Linear Circuits Data Book

TEXAS INSTRUMENTS

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INTRODUCTION

The rapid advance in high-tech digital processing creates new demands for microprocessor-compatible circuits that can sense, amplify, and convert analog signals or provide regulated power to a system. In this volume, Texas Instruments presents specifications and technical information on our broad line of integrated circuits designed for applications that involve analogue signal conditioning. That product line includes:

- Operational amplifiers
- Voltage comparators
- Regulators
- Power supply monitors
- Switching-mode power supply circuits
- Current mirrors
- Floppy-disk circuits for control, reading, or writing
- Timers
- A/D converters
- Video amplifiers
- Analog switches
- D/A converters

These circuits span the recent rapid development of integrated circuit technology from classical bipolar through BIFET™ and BIDFET™ to TI's new LinCMOS™ processing that provides a step-function improvement in input impedance, power dissipation, and threshold stability. New surface-mount packages include both plastic and ceramic chip carriers and the small-outline packages that increase board density with little impact on power handling capability.

Ordering information and mechanical data are in the Appendix. Section 1 contains an alphanumeric index that lists page numbers for all the device types included, and each data sheet section provides a functional selection guide to the devices in that section.

While this volume offers design and specification data only for Linear components, complete technical data for any TI semiconductor product is available from your nearest TI sales office.
A listing can be found at the back of this data book.

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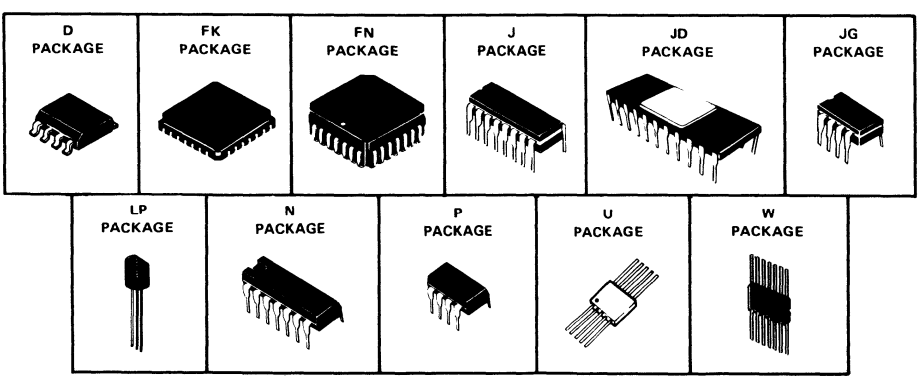
Appendix A

THERMAL RESISTANCE

PACKAGE	PINS	JUNCTION-TO-CASE THERMAL RESISTANCE $R_{\theta JC}$(°C/W)	JUNCTION-TO-AMBIENT THERMAL RESISTANCE $R_{\theta JA}$(°C/W)
D plastic dual-in-line	8	51	172
	14, 16	33	131
FK ceramic chip carrier	20	35	91
FN plastic chip carrier	20	37	114
J ceramic dual-in-line (glass-mounted chips)	14 thru 20	60	122
J ceramic dual-in-line† (alloy-mounted chips)	14 thru 20	29†	91†
JG ceramic dual-in-line (glass-mounted chips)	8	58	151
JG ceramic dual-in-line† (alloy-mounted chips)	8	26†	119†
KC Standard lead frame	3	6	62.5
LP plastic plug-in	3	40	160
N plastic dual-in-line	14 thru 20	72	143
	28	45	100
	40	40	100
P plastic dual-in-line	8	79	172
U ceramic flat	10, 14	55	185
W ceramic flat	14, 16	60	125

† In addition to those products so designated on their data sheets, all devices having a type number prefix of "SNC" or "SNM," or a suffix of "/883B" have alloy-mounted chips.

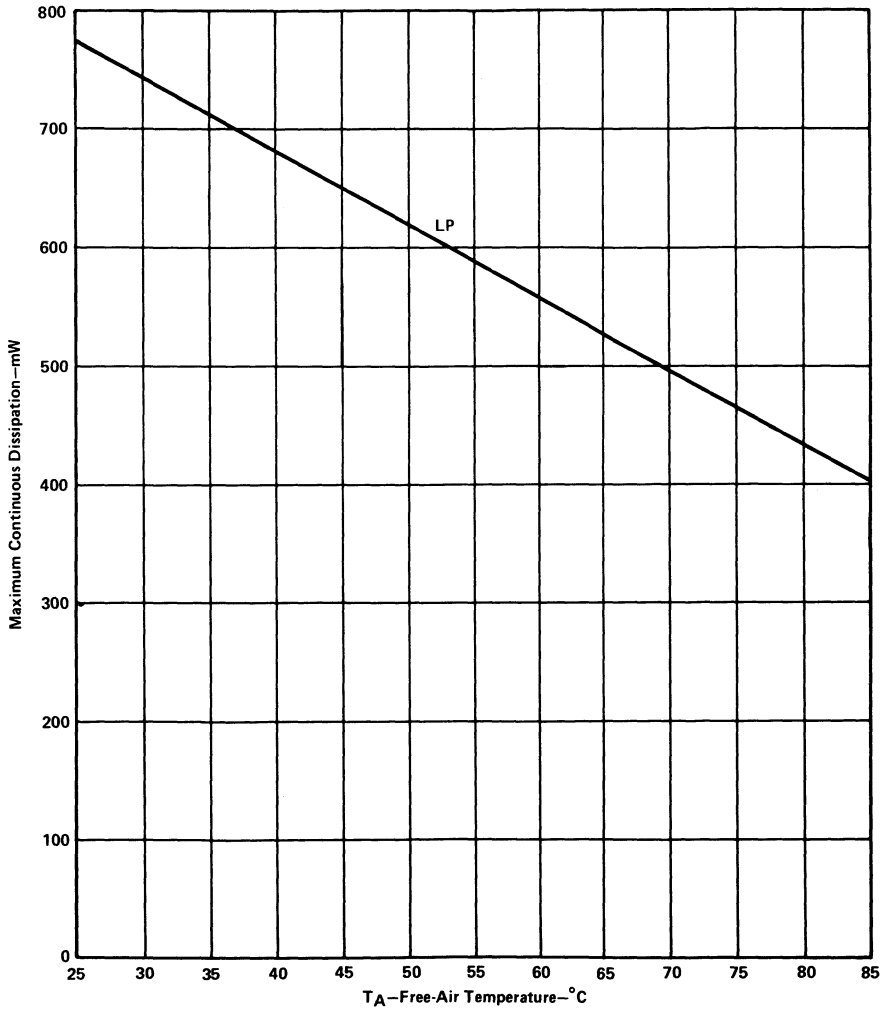
† This package no longer available.



PLASTIC PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

DISSIPATION DERATING CURVE



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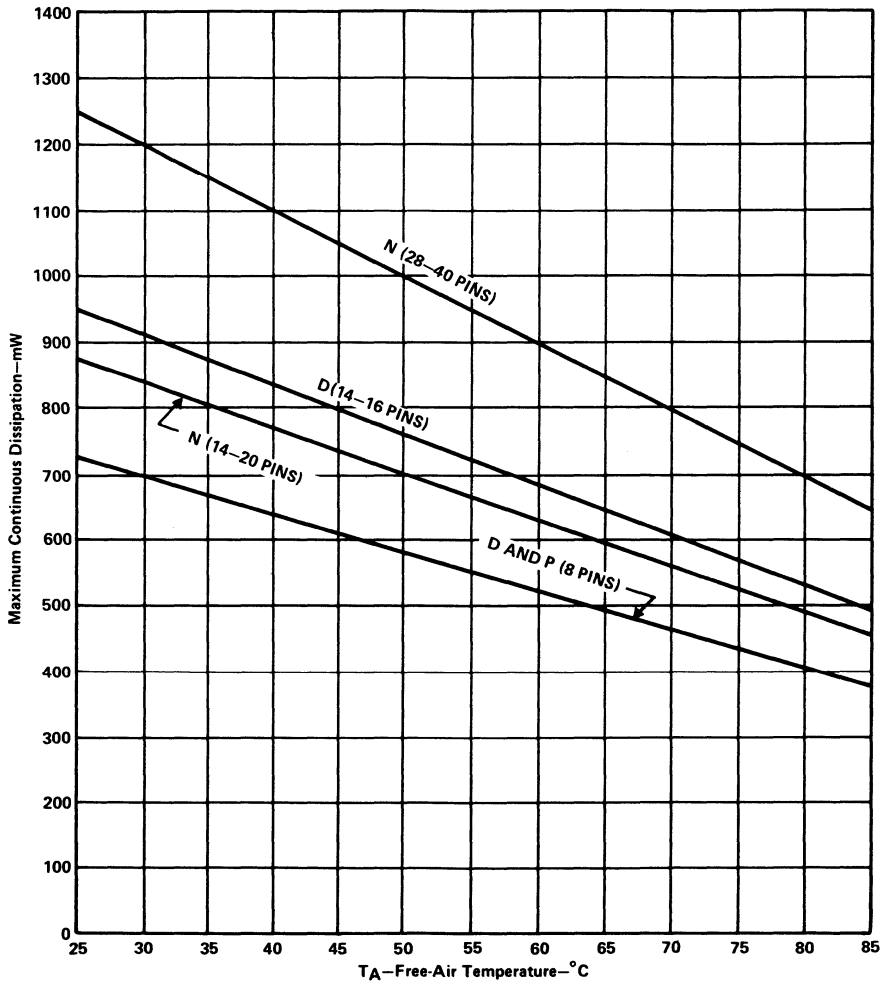
PLASTIC PACKAGES (CONTINUED)

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

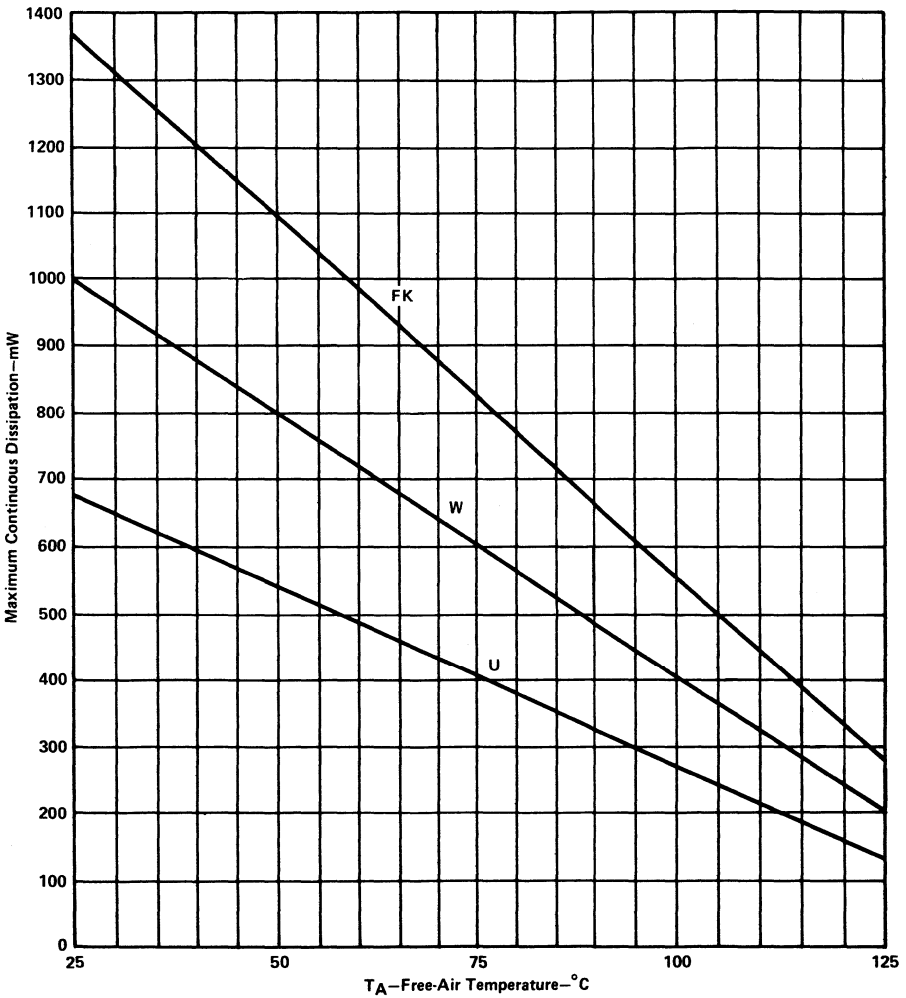
DISSIPATION DERATING CURVE



FLAT PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

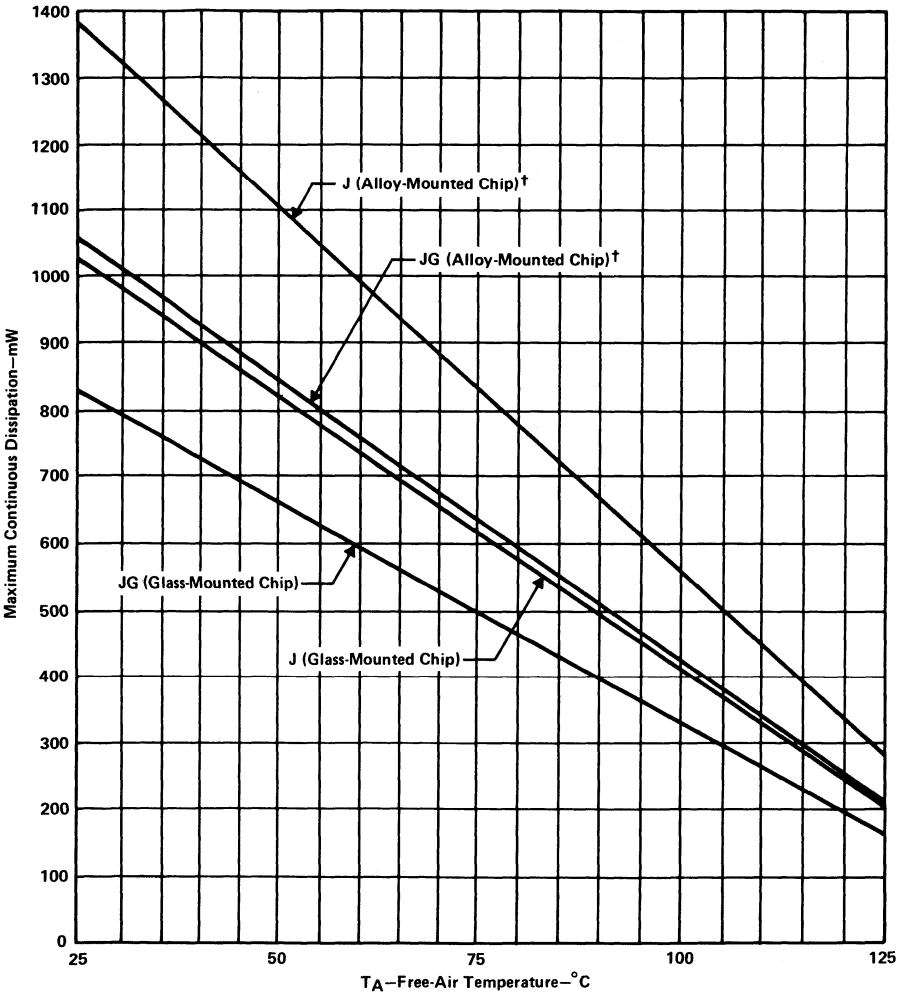
DISSIPATION DERATING CURVE



CERAMIC DUAL-IN-LINE PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

DISSIPATION DERATING CURVE



†In addition to those products so designated on their data sheets, all devices having a type number prefix of "SNC" or "SNM", or a suffix of "/883B" have alloy-mounted chips.

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Thermal Information 2

Special Functions 5

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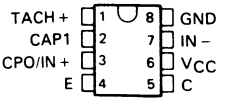
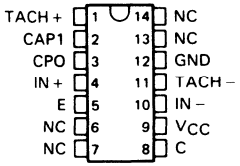
D3003, MARCH 1986

- **Output Swings to Ground for Zero-Frequency Input**
- **Only One RC Network Provides Frequency Doubling for Low Ripple**
- **8-Pin Versions Interface Directly to Variable-Reluctance Magnetic Pickups**
- **Uncommitted Collector and Emitter Outputs Provide 40-mA Sink or Source Current to Operate Relays, Solenoids, Meters, or LEDs**
- **Built-In Hysteresis for Noise Immunity**
- **Linearity Typically ±0.3%**
- **8-Pin Versions are Fully Protected from Damage Due to TACH Input Swing Above V_{CC} and Below Ground**

LM2907, LM2917 . . . D OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



LM2907, LM2917 . . . D OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

applications

Over/under speed sensing
Frequency-to-voltage conversion
Speedometers
Breaker-point dwell meters
Hand-held tachometers
Speed governors
Cruise control
Automotive door-lock control
Clutch control
Horn control
Touch or sound switches

description

The LM2907 and LM2917 are monolithic frequency-to-voltage converters with an output circuit designed to operate a relay, lamp, or other load when the input frequency reaches or exceeds a selected rate. The converter (tachometer) section consists of a comparator driving a charge pump and offers frequency doubling for low ripple, full input protection in 8-pin versions, and an output swing to ground for a zero-frequency input. The output section consists of an operational amplifier, normally operating as a comparator, that drives an output transistor with both the collector and emitter floating. The circuit can either sink or source 40 milliamperes of load current.

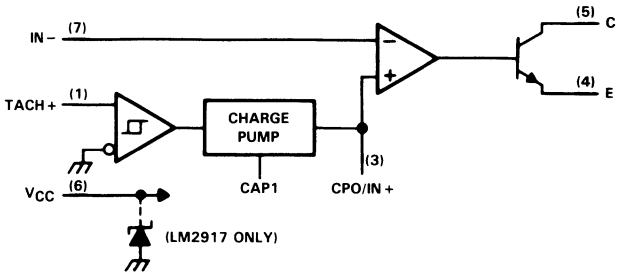
Two basic configurations of the devices are offered; an 8-pin version and a 14-pin version. The 8-pin versions have a ground-referenced tachometer input and an internal connection between the tachometer output and the operational amplifier input. The 8-pin version is well suited to single-speed or single-frequency switching or fully buffered frequency-to-voltage conversion applications. The more versatile 14-pin versions provide differential tachometer inputs and uncommitted operational amplifier inputs. In the 14-pin versions, the tachometer input can be floated and the operational amplifier becomes suitable for active filter conditioning of the tachometer output.

The LM2917 has an active shunt regulator connected across the power leads. The regulator clamps the supply voltage so that stable frequency-to-voltage and frequency-to-current conversions are possible with any supply voltage and a suitable resistor.

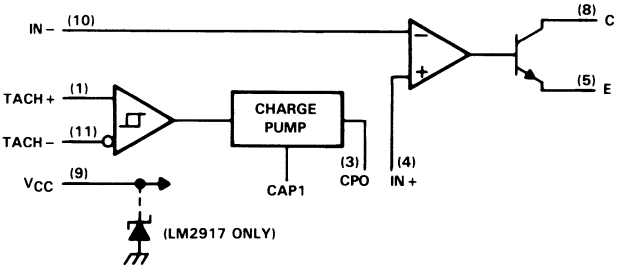
The LM2907 and LM2917 are designed for operation from −40°C to 85°C.

functional block diagrams

8-PIN VERSIONS



14-PIN VERSIONS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}: LM2907 . . . . . 28 V
Supply current, I_{CC}: LM2917 . . . . . 25 mA
Collector-to-emitter voltage . . . . . 28 V
Operational amplifier input voltage, IN+ and IN– . . . . . 0 V to V_{CC}
Tachometer input voltage: 8-pin version TACH+ . . . . . 0 V to 28 V
14-pin version TACH+ and TACH– . . . . . 0 V to V_{CC}
Continuous total dissipation at (or below) 25°C (see Note 1) . . . . . 500 mW
Operating free-air temperature range . . . . . –40°C to 85°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature range 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: For operation above 25°C free-air temperature, see Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D (8 pins)	500 mW	5.8 mW/°C	64°C
D (14 pins)	500 mW	7.6 mW/°C	84°C
N	500 mW	7.0 mW/°C	79°C
P	500 mW	5.8 mW/°C	64°C

electrical characteristics, V_{CC} = 12 V (LM2907), V+ = 12 V through 470 Ω (LM2917), T_A = 25°C

converter (tachometer) section

PARAMETER			TEST CONDITIONS	LM2907			LM2917			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage		V_I = 250 mV, f = 1 kHz	±10	±15	±40	±10	±15	±40	mV
V_{hys}	Input hysteresis (see Note 2)		V_I = 250 mV, f = 1 kHz		30			30		mV
V_{IO}	Input offset voltage (see Note 2)	8-pin versions	V_I = 250 mV, f = 1 kHz		5	15		5	15	mV
		14-pin versions	V_{ID} = 250 mV, f = 1 kHz		3.5	10		3.5	10	
I_{IB}	Input bias current		V_I = ±50 mV		0.1	1		0.1	1	μA
V_{OH}	High-level output voltage, CAP1		V_I or V_{ID} = 125 mV		8.3			5.0		V
V_{OL}	Low-level output voltage, CAP1		V_I or V_{ID} = −125 mV		2.3			1.2		V
I_O	Output current, CAP1, CPO		CAP1 and CPO at 6 V	140	180	240				μA
			CAP1 and CPO at 3.8 V				140	180	240	
	Leakage current, CPO		CAP1 open, CPO at 0 V, See Note 4			0.1			0.1	μA
	Gain constant			0.9	1	1.1	0.9	1	1.1	
	Nonlinearity (see Note 3)		f = 1 kHz, 5 kHz, or 10 kHz		0.3	±1		0.3	±1	%

output section

PARAMETER		TEST CONDITIONS	LM2907			LM2917			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_I = 6 V, See Note 4		3	10				mV
		V_I = 3.8 V, See Note 4					3	10	
I_{IB}	Bias current	V_I = 6 V		50	500				nA
		V_I = 3.8 V					50	500	
A_V	Voltage amplification			200			200		V/mV
I_C	Collector output (sink) current	V_C = 1 V, V_E = 0	40	50		40	50		mA
I_E	Emitter output (source) current	V_C = V_{CC}, V_E = V_{CC} − 2		−10			−10		mA
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 5 mA		0.1	0.5		0.1	0.5	V
		I_C = 20 mA			1			1	
		I_C = 50 mA		1	1.5		1	1.5	

NOTES: 2. Hysteresis is the algebraic difference $V_{T+} - V_{T-}$; offset voltage is the difference in magnitudes $V_{T+} - V_{T-}$. See parameter measurement information test circuits.

3. Nonlinearity is defined as the deviation of V_O at CPO for f = 5 kHz from a straight line defined by the V_O at 1 kHz and V_O at 10 kHz, with C1 = 1000 pF, R1 = 68 kΩ, C2 = 0.22 μF.

4. Pin 2 must be bypassed with a 0.001-μF capacitor to prevent oscillation for these tests.

electrical characteristics

zener regulator (LM2917 only) V+ = 12 V through 470 Ω, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Regulated supply voltage		7.56		V
r_s	Series resistance		10.5	15	Ω
αV_{CC}	Temperature coefficient of regulated supply voltage		1		mV/°C

total device (LM2907 only) V_{CC} = 12 V, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
I_{CC}	Supply current		3.8	6	mA

PARAMETER MEASUREMENT INFORMATION

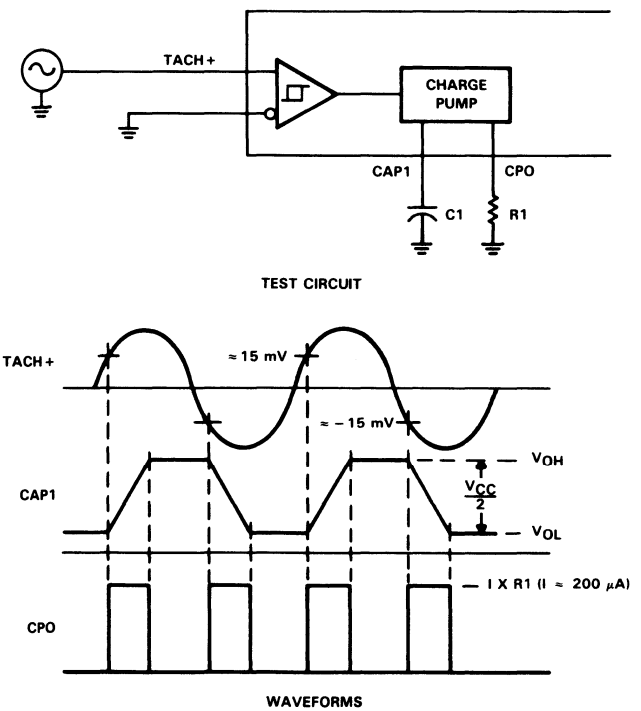


FIGURE 1. TEST CIRCUIT AND WAVEFORMS

TYPICAL APPLICATION DATA

The LM2907 and LM2917 frequency-to-voltage converter circuits are designed for maximum versatility with a minimum of external parts. The first stage of these devices is a differential comparator. The single-input 8-pin versions have one input grounded so that an input signal must swing above and below ground and exceed the input thresholds to produce an output. This version is specifically for magnetic variable-reluctance pickups, which typically provide a single-ended ac output. These single-ended inputs are fully protected against voltage swings to ±28 volts, which are easily attained by these types of pickups.

The differential-input 14-pin versions provide the option of setting the input reference level and still having hysteresis around that level to provide excellent noise rejection in any application. The input protection is removed in the 14-pin versions. Therefore, neither of the differential inputs should exceed the limits of the supply voltage. An input must not go below ground without a resistance in the lead to limit the current that will flow in the epi-substrate diode. The charge pump circuit that follows the input stage produces a dc output voltage proportional to the input frequency. The charge pump circuit (see Figure 2) consists of a timing capacitor (C1), an output resistor (R1), and an integrating or filter capacitor (C2). When the input changes state (due to a suitable zero crossing or differential voltage on the input), the timing capacitor is either charged or discharged linearly with a constant current of 200 μA through CAP1 between two voltages whose difference is $V_{CC}/2$. Within one-half cycle of the input frequency or a time equal to 1/2f, the change in charge on C1 is equal to (VCC/2)C1. The average amount of current pumped into or out of the capacitor is:

$$\text{CAP1 current (average)} = \frac{Q}{T} = C1 \cdot \frac{V_{CC}}{2} \cdot 2f = V_{CC} \cdot f \cdot C1$$

The output of the charge pump accurately mirrors the CAP1 current into the load resistor (R1) connected to CPO. If the pulses of current are integrated with a filter capacitor, the output voltage is the average CAP1 current times R1, and the total equation becomes:

$$V_O = V_{CC} \cdot f \cdot C1 \cdot R1 \cdot K$$

where K is the gain factor, which is typically 1.

The size of C2 is dependent only on the amount of ripple allowable and the required response time.

selection of R1, C1, and C2

To achieve optimum performance, there are some limitations to be considered in the selection of R1 and C1. The timing capacitor controls the RC time and provides internal compensation for the charge pump circuit. For very accurate operation it should be 100 picofarads or greater. Smaller values, especially at lower temperatures, can cause an error current through R1. $V_O/R1$ must be less than or equal to the output current at CPO, which is fixed typically at 180 microamperes. If R1 is too large it becomes a significant fraction of the output impedance at CPO, which degrades the linearity. In addition, ripple voltage must be considered when selecting R1. The size of C2 is directly affected by the size of R1. An expression that describes the ripple content at CPO is:

$$V_{ripple} = \frac{V_{CC}}{2} \cdot \frac{C1}{C2} \cdot \left(1 - V_{CC} \cdot f \cdot \frac{C1}{200}\right) \quad \text{volts peak-to-peak}$$

where

C1 and C2 are in farads
V_{CC} is in volts
f is in hertz.

TYPICAL APPLICATION DATA

R1 cannot be chosen independently of ripple because response time or the time it takes V_O to stabilize at a new level increases as the size of C2 increases. A compromise between ripple, response time, and linearity must be chosen carefully. As a final consideration, the maximum attainable input frequency is determined by V_{CC}, C1, and I_{cap} (current through CAP1).

$$f_{max} = \frac{I_{cap}}{C1 \cdot V_{CC}} \quad \text{hertz}$$

where

I_{cap} is typically 200 μA
C1 is in farads
V_{CC} is in volts.

zener regulator options (LM2917)

For those applications in which an output voltage or current must be obtained independently of supply voltage variations, the LM2917 can be used. The most important factor in selecting a dropping resistor for the unregulated supply is that the frequency-to-voltage converter circuit and the operational amplifier alone require approximately 3 mA at the voltage level set by the zener diode. At low supply voltages there must be some current flowing in the resistor above the 3 mA circuit current to operate the regulator. As an example, if the supply voltage varies between 9 and 16 volts, a resistance of 470 Ω will minimize the zener voltage variation to typically 160 mV. If the resistance goes under 400 Ω or above 600 Ω, the zener variation quickly rises above 200 mV for the same input variation.

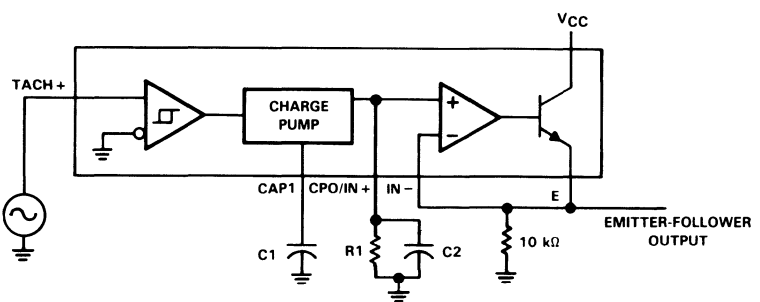


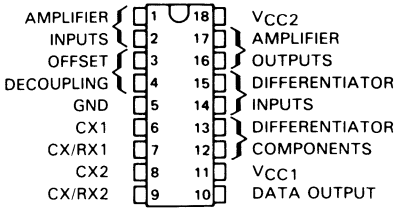
FIGURE 2. MINIMUM-COMPONENT TACHOMETER

TYPE MC3470
FLOPPY DISK READ-AMPLIFIER SYSTEM

D2759, NOVEMBER 1983

- **Combines All Read-Amplifier Active Circuitry into One Monolithic Circuit**
- **Guaranteed Maximum Peak Shift of 5%**
- **Designed to be Interchangeable with Motorola MC3470**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)

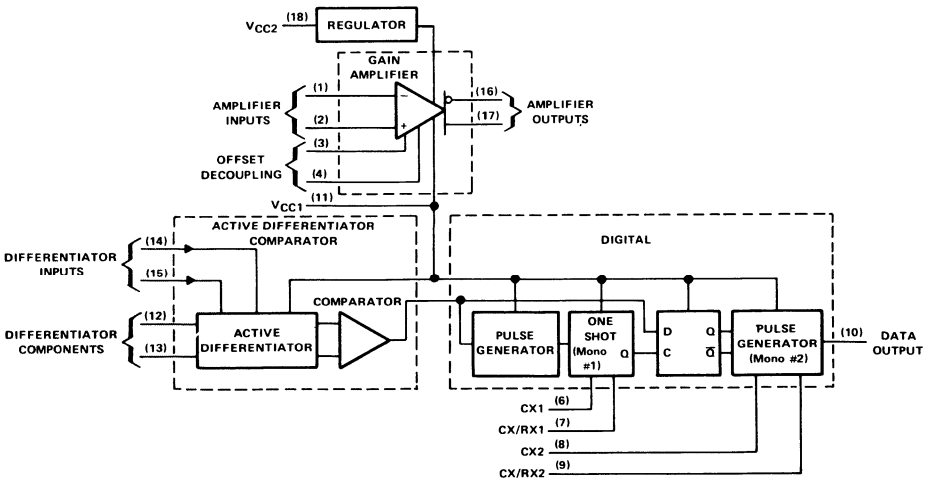


description

The MC3470 is a monolithic read-amplifier system containing all the active circuitry necessary for obtaining digital information from floppy disk storage. It is designed to accept the ac differential signal from the magnetic head and produce a digital output pulse corresponding to each peak of the input signal. The gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output.

The MC3470 is characterized for operation from 0°C to 70°C.

functional block diagram



ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 7 V
Supply voltage, V_{CC2} . . . . . 16 V
Input voltage range (amplifier inputs) . . . . . −0.2 V to 7 V
Output voltage, V_O (data output) . . . . . −0.2 V to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage V_{CC1}		4.75	5	5.25	V
Supply voltage V_{CC2}		10	12	14	V
Timing capacitor CX1 (see Note 2)		150		680	pF
Timing capacitor CX2		100		800	pF
Timing resistors RX1 and RX2		1.5		10	kΩ
Timing of digital section	Monostable no. 1	500		4000	ns
	Monostable no. 2	150		1000	
Operating free-air temperature, T_A		0		70	°C

NOTE 2: To minimize current transients, CX1 should be kept as small as convenient.

electrical characteristics over recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

gain amplifier section

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
A_{VD}	Differential voltage amplification	V_{id} = 5 mV rms,	f = 200 kHz	80	100	120	V/V
I_{IB}	Input bias current				−10	−25	μA
V_{ICR}	Common-mode input voltage range	THD ≤ 5%		−0.1 to 1.5			V
V_{IDR}	Differential input voltage range	THD ≤ 5%		±25			mV
V_{OPP}	Peak-to-peak differential output voltage			3	4		V
V_{OC}	Common-mode output voltage	V_I = 0 V,	V_{ID} = 0 V		3		V
V_{OD}	Differential output offset voltage	V_I = 0 V, T_A = 25°C	V_{ID} = 0 V,			0.4	V
I_O	Output current (each amplifier output)	To ground			−8		mA
		From V_{CC1}		2.8	4		
r_i	Input resistance	T_A = 25°C		100	250		kΩ
r_o	Output resistance (single-ended)	V_{CC1} = 5 V, T_A = 25°C	V_{CC2} = 12 V,		15		Ω
BW	Bandwidth (3 dB)	V_{id} = 2 mV rms, V_{CC2} = 12 V,	V_{CC1} = 5 V, T_A = 25°C	5			MHz
CMRR	Common-mode rejection ratio	V_{CC1} = 5 V, f = 100 kHz, T_A = 25°C	V_{IPP} = 200 mV, A_{VD} = 40 dB,	50			dB
k_{SVR}	Supply voltage rejection ratio	A_{VD} = 40 dB, T_A = 25°C	V_{CC1} = 5 ± 0.25 V, V_{CC2} = 12 V	50			dB
			V_{CC1} = 5 V, V_{CC2} = 12 ±2 V	60			
V_n	Equivalent input noise voltage	BW = 10 Hz to 1 MHz, T_A = 25°C			15		μV

active-differentiator section

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{sink}	Sink current at pins 12 and 13	V_{OD} = V_{CC1}		1	1.4		mA
	Peak shift	V_{CC1} = 5 V, V_{IDPP} = 1 V, I_{cap} = 500 μA,	V_{CC2} = 12 V, f = 250 kHz, See Figure 1			5%	
r_{id}	Differential input resistance				30		kΩ
r_{od}	Differential output resistance				40		Ω

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 12 V, T_A = 25°C.

digital section

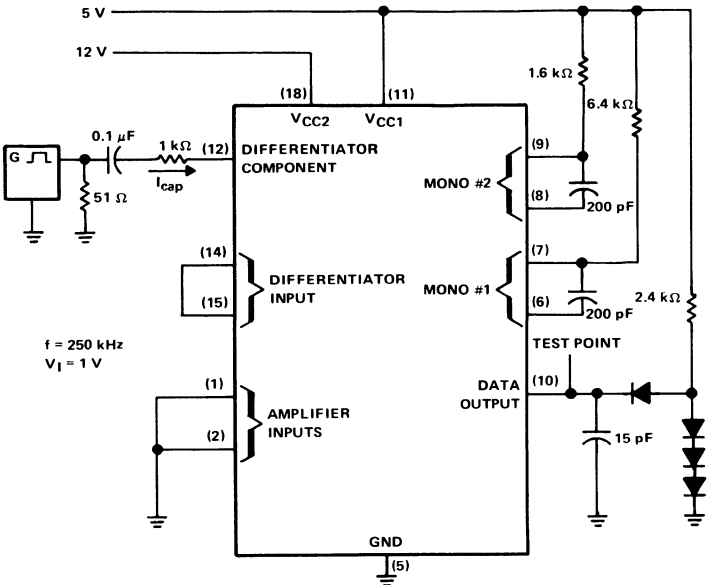
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 10)	V_{CC1} = 4.75 V, V_{CC2} = 12 V, I_{OH} = −0.4 mA	2.7			V
V_{OL}	Low-level output voltage (pin 10)	V_{CC1} = 4.75 V, V_{CC2} = 12 V, I_{OL} = 8 mA			0.5	V
I_{CC1}	Supply current from V_{CC1}	V_{CC1} = 5.25 V		35	50	mA
I_{CC2}	Supply current from V_{CC2}	V_{CC2} = 14 V		4.5	10	mA

timing characteristics over recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted) (see Figure 2)

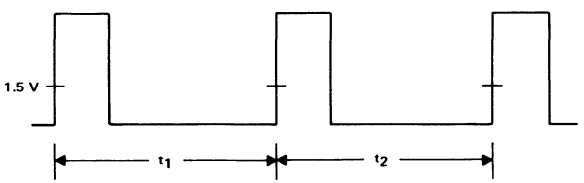
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_r	Rise time (pin 10)				20	ns
t_f	Fall time (pin 10)				25	ns
	Timing accuracy of monostable no. 1 compared to 0.625 RX1 • CX1 + 200 ns	RX1 = 1.5 kΩ to 10 kΩ, CX1 = 150 pF to 680 pF	85%		115%	
	Timing accuracy of monostable no. 2 compared to 0.625 RX2 • CX2	RX2 = 1.5 kΩ to 10 kΩ, CX2 = 100 pF to 800 pF	85%		115%	

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 12 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

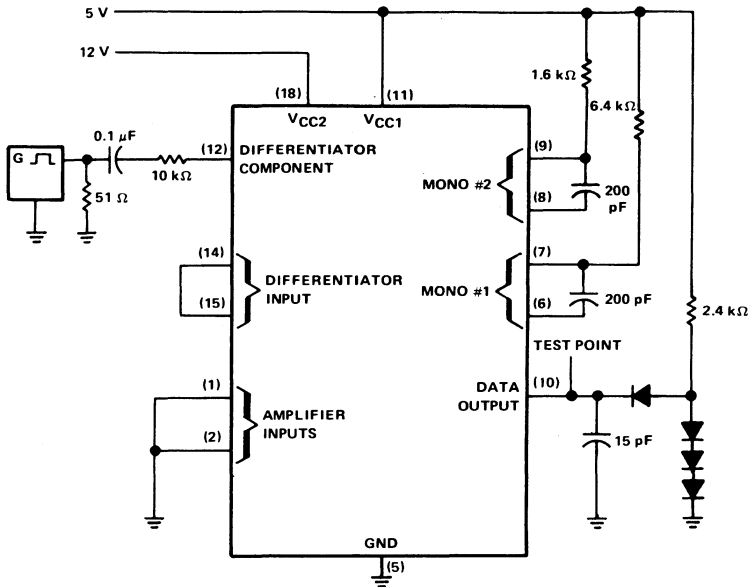


$$\text{Peak shift} = \frac{(t_1 - t_2)}{2\,(t_1 + t_2)} \; 100\%$$

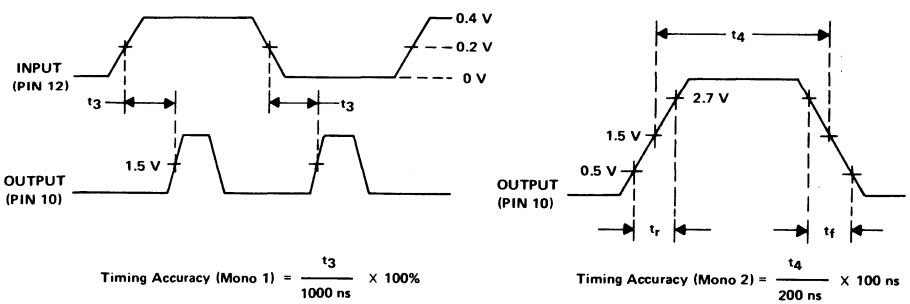
VOLTAGE WAVEFORMS

FIGURE 1–PEAK SHIFT

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2–TIMING ACCURACY

TYPICAL CHARACTERISTICS

NORMALIZED POWER SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

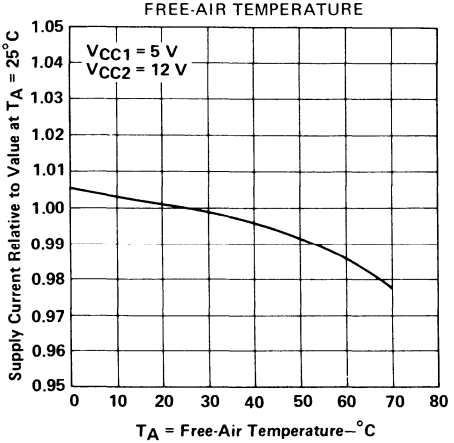


FIGURE 3

NORMALIZED VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

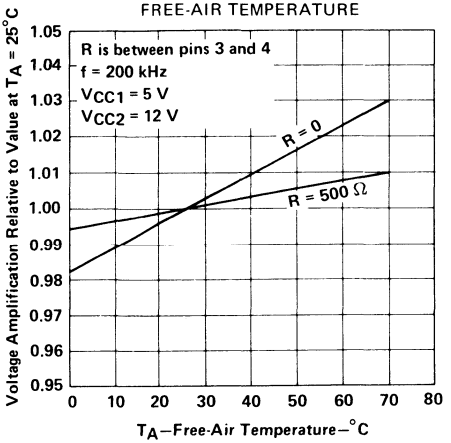


FIGURE 4

NORMALIZED TIME DELAY (PIN 12 TO PIN 10)
vs
FREE-AIR TEMPERATURE

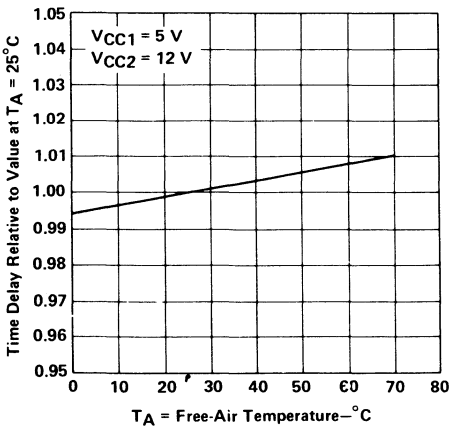


FIGURE 5

VOLTAGE AMPLIFICATION (NORMALIZED)
and PHASE SHIFT
vs
FREQUENCY

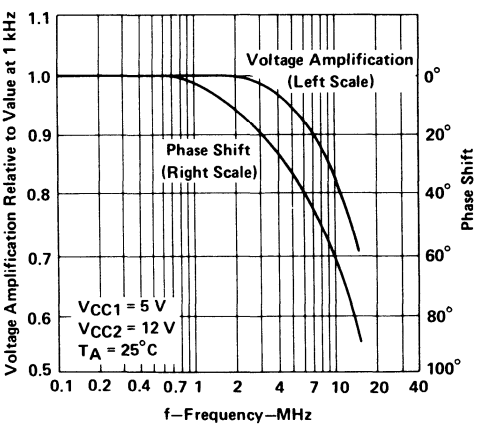


FIGURE 6

TYPICAL APPLICATION INFORMATION

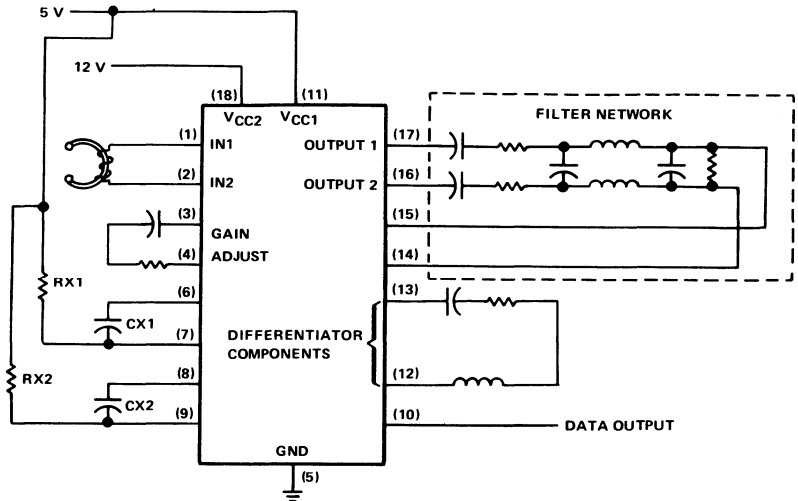


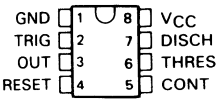
FIGURE 7

TYPES SE555, SE555C, SA555, NE555 PRECISION TIMERS

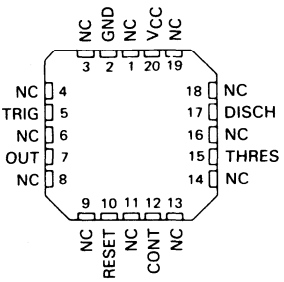
D1669, SEPTEMBER 1973—REVISED OCTOBER 1983

- **Timing from Microseconds to Hours**
- **Astable or Monostable Operation**
- **Adjustable Duty Cycle**
- **TTL-Compatible Output Can Sink or Source up to 200 mA**
- **Functionally Interchangeable with the Signetics SE555, SE555C, SA555, NE555; Have Same Pinout**

NE555, SE555, SE555C . . . JG DUAL-IN-LINE PACKAGE
SA555, NE555 . . . D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



SE555, SE555C . . . FH OR FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC—No internal connection

description

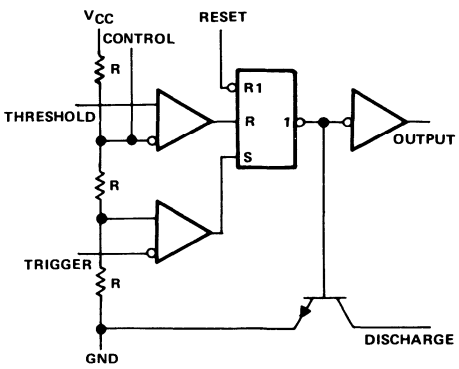
These devices are monolithic timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle may be independently controlled with two external resistors and a single external capacitor.

The threshold and trigger levels are normally two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

The output circuit is capable of sinking or sourcing current up to 200 milliamperes. Operation is specified for supplies of 5 to 15 volts. With a 5-volt supply, output levels are compatible with TTL inputs.

The SE555 and SE555C are characterized for operation over the full military range of −55°C to 125°C. The SA555 is characterized for operation from −40°C to 85°C, and the NE555 is characterized for operation from 0°C to 70°C.

functional block diagram



Reset can override Trigger, which can override Threshold.

FUNCTION TABLE

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	< 1/3 V_{DD}	Irrelevant	High	Off
High	> 1/3 V_{DD}	> 2/3 V_{DD}	Low	On
High	> 1/3 V_{DD}	< 2/3 V_{DD}	As previously established	

†Voltage levels shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Input voltage (control voltage, reset, threshold, trigger) . . . . . V_{CC}
Output current . . . . . ±225 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 600 mW
Operating free-air temperature range: SE555, SE555C . . . . . −55°C to 125°C
SA555 . . . . . −40°C to 85°C
NE555 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: FH, FK, or JG package . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the JG package, SE555 and SE555C chips are alloy mounted, SA555 and NE555 chips are glass mounted.

recommended operating conditions

	SE555		SE555C		SA555		NE555		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	4.5	18	4.5	16	4.5	16	4.5	16	V
Input voltage (control voltage, reset, threshold, trigger)		V_{CC}		V_{CC}		V_{CC}		V_{CC}	V
Output current		±200		±200		±200		±200	mA
Operating free-air temperature, T_A	−55	125	−55	125	−40	85	0	70	°C

electrical characteristics at 25°C free-air temperature, V_{CC} = 5 V to 15 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE555			SE555C, SA555 NE555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level	V_{CC} = 15 V		9.4	10	10.6	8.8	10	11.2	V
	V_{CC} = 5 V		2.7	3.3	4	2.4	3.3	4.2	
Threshold current (see Note 3)				30	250		30	250	nA
Trigger voltage level	V_{CC} = 15 V		4.8	5	5.2	4.5	5	5.6	V
	V_{CC} = 5 V		1.45	1.67	1.9	1.1	1.67	2.2	
Trigger current	Trigger at 0 V			0.5	0.9		0.5	2	μA
Reset voltage level			0.4	0.7	1	0.4	0.7	1	V
Reset current	Reset at V_{CC}			0.1	0.4		0.1	0.4	mA
	Reset at 0 V			−0.4	−1		−0.4	−1	
Discharge switch off-state current				20	100		20	100	nA
Control voltage (open circuit)	V_{CC} = 15 V		9.6	10	10.4	9	10	11	V
	V_{CC} = 5 V		2.9	3.3	3.8	2.6	3.3	4	
Low-level output voltage	V_{CC} = 15 V	I_{OL} = 10 mA		0.1	0.15		0.1	0.25	V
		I_{OL} = 50 mA		0.4	0.5		0.4	0.75	
		I_{OL} = 100 mA		2	2.2		2	2.5	
		I_{OL} = 200 mA		2.5			2.5		
	V_{CC} = 5 V	I_{OL} = 5 mA		0.05	0.15		0.05	0.25	
		I_{OL} = 8 mA		0.1	0.2		0.25	0.3	
High-level output voltage	V_{CC} = 15 V	I_{OH} = −100 mA	13	13.3		12.75	13.3		V
		I_{OH} = −200 mA		12.5			12.5		
	V_{CC} = 5 V	I_{OH} = −100 mA	3	3.3		2.75	3.3		
Supply current	Output low, No load	V_{CC} = 15 V		10	12		10	15	mA
		V_{CC} = 5 V		3	5		3	6	
	Output high, No load	V_{CC} = 15 V		9	10		9	13	
		V_{CC} = 5 V		2	4		2	5	

NOTE 3: This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 13. For example, when V_{CC} = 5 V the maximum value is $R = R_A + R_B \approx 3.4$ MΩ and for V_{CC} = 15 V the maximum value is 10 MΩ.

operating characteristics, V_{CC} = 5 V and 15 V

PARAMETER		TEST CONDITIONS†	SE555			SE555C, SA555 NE555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval‡	Each timer, monostable§	T_A = 25°C		0.5	1.5		1	3	%
	Each timer, astable¶			1.5			2.25		
Temperature coefficient of timing interval	Each timer, monostable§	T_A = MIN to MAX		30	100		50		ppm/°C
	Each timer, astable¶			90			150		
Supply voltage sensitivity of timing interval	Each timer, monostable§	T_A = 25°C		0.05	0.2		0.1	0.5	%/V
	Each timer, astable¶			0.15			0.3		
Output pulse rise time		C_L = 15 pF, T_A = 25°C		100	200		100	300	ns
Output pulse fall time				100	200		100	300	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡Timing interval error is defined as the difference between the measured value and the nominal value computed by the formula: $t_w = 1.1\ R_A C$.
§Values specified are for a device in a monostable circuit similar to Figure 10, with component values as follow: R_A = 2 kΩ to 100 kΩ, C = 0.1 μF.
¶Vallues specified are for a device in an astable circuit similar to Figure 1, with component values as follow: R_A = 1 kΩ to 100 kΩ, C = 0.1 μF.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

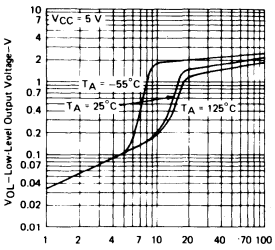


FIGURE 1

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

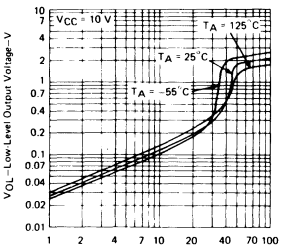


FIGURE 2

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

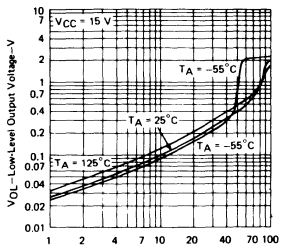


FIGURE 3

DROP BETWEEN SUPPLY VOLTAGE AND OUTPUT vs HIGH-LEVEL OUTPUT CURRENT

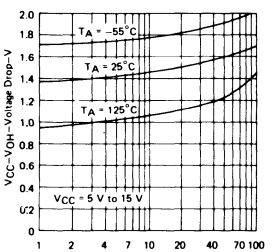


FIGURE 4

SUPPLY CURRENT vs SUPPLY VOLTAGE

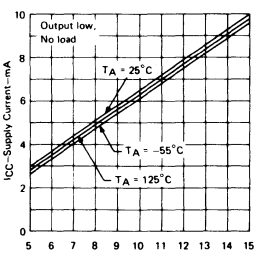


FIGURE 5

MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING vs LOWEST VOLTAGE LEVEL OF TRIGGER PULSE

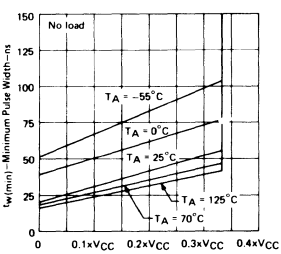


FIGURE 6

NORMALIZED OUTPUT PULSE WIDTH (MONOSTABLE OPERATION) vs SUPPLY VOLTAGE

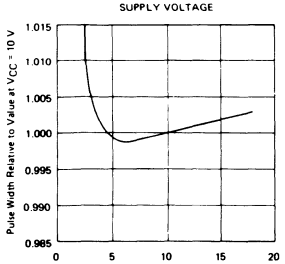


FIGURE 7

NORMALIZED OUTPUT PULSE WIDTH (MONOSTABLE OPERATION) vs FREE-AIR TEMPERATURE

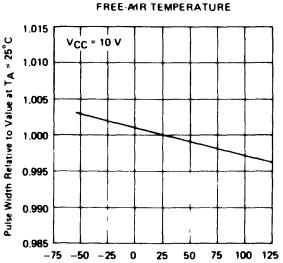


FIGURE 8

PROPAGATION DELAY TIME vs LOWEST VOLTAGE LEVEL OF TRIGGER PULSE

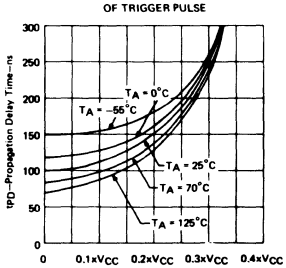


FIGURE 9

†Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

TYPICAL APPLICATION DATA

monostable operation

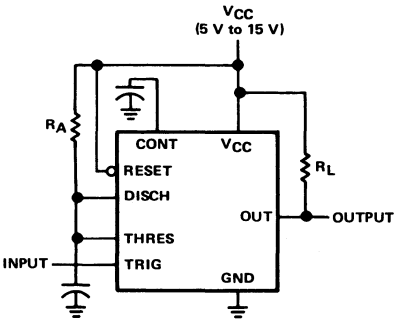


FIGURE 10–CIRCUIT FOR MONOSTABLE OPERATION

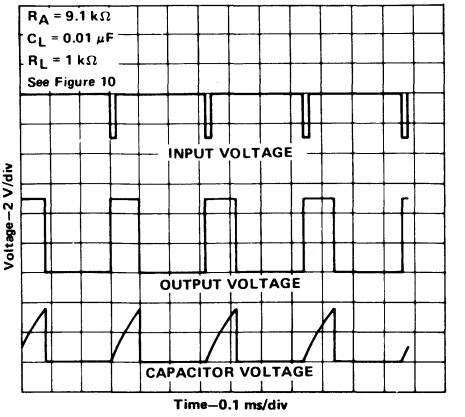


FIGURE 11–TYPICAL MONOSTABLE WAVEFORMS

For monostable operation, any of these timers may be connected as shown in Figure 10. If the output is low, application of a negative-going pulse to the trigger input sets the flip-flop ($\overline{Q}$ goes low), drives the output high, and turns off Q1. Capacitor C is then charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold input. If the trigger input has returned to a high level, the output of the threshold comparator will reset the flip-flop ($\overline{Q}$ goes high), drive the output low, and discharge C through Q1.

Monostable operation is initiated when the trigger input voltage falls below the trigger threshold. Once initiated, the sequence will complete only if the trigger input is high at the end of the timing interval. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_W = 1.1\ R_AC$. Figure 12 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates are both directly proportional to the supply voltage, V_{CC}. The timing interval is therefore independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to the reset and trigger terminals during the timing interval will discharge C and re-initiate the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. When the reset pulse is low. When the reset input is not used, it should be connected to V_{CC} to prevent false triggering.

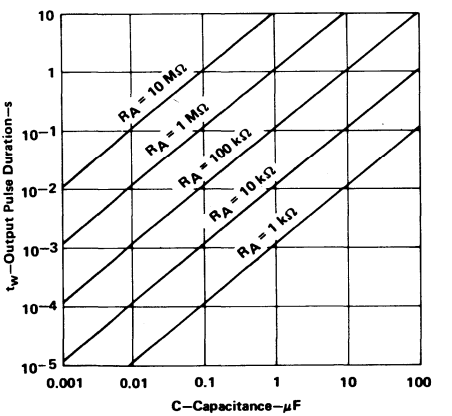
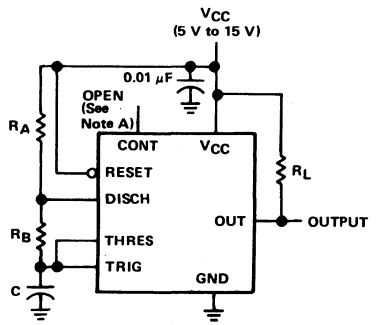


FIGURE 12–OUTPUT PULSE DURATION vs CAPACITANCE

TYPICAL APPLICATION DATA

astable operation



NOTE A: Decoupling the control voltage input to ground with a capacitor may improve operation. This should be evaluated for individual applications.

FIGURE 13–CIRCUIT FOR ASTABLE OPERATION

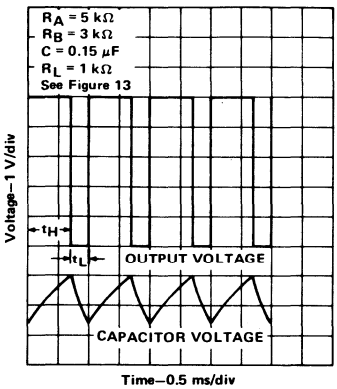


FIGURE 14–TYPICAL ASTABLE WAVEFORMS

Addition of a second resistor, R_B, to the circuit of Figure 10, as shown in Figure 13, and connection of the trigger input to the threshold input will cause the timer to self-trigger and run as a multivibrator. The capacitor C will charge through R_A and R_B then discharge through R_B only. The duty cycle may be controlled, therefore, by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \cdot V_{CC}$) and the trigger-voltage level ($\approx 0.33 \cdot V_{CC}$). As in the monostable circuit, charge and discharge times (and therefore the frequency and duty cycle) are independent of the supply voltage.

Figure 14 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L may be found by:

$$t_H = 0.693\ (R_A + R_B)\ C$$

$$t_L = 0.693\ (R_B)\ C$$

Other useful relationships are shown below.

$$\text{period} = t_H + t_L = 0.693\ (R_A + 2R_B)\ C$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)\ C}$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B}$$

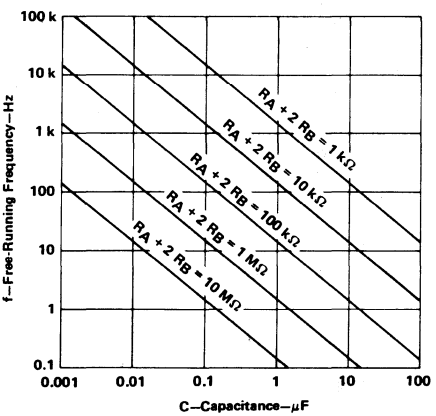


FIGURE 15–FREE-RUNNING FREQUENCY

TYPICAL APPLICATION DATA

missing-pulse detector

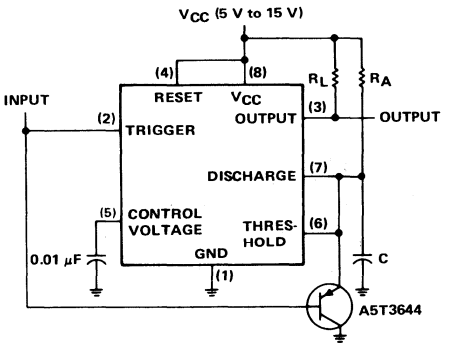


FIGURE 16–CIRCUIT FOR MISSING-PULSE DETECTOR

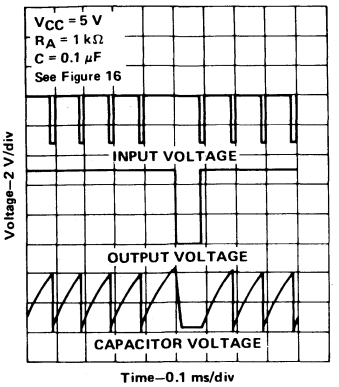


FIGURE 17–MISSING-PULSE DETECTOR WAVEFORMS

The circuit shown in Figure 16 may be utilized to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is continuously retriggered by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train will permit the timing interval to be completed, thereby generating an output pulse as illustrated in Figure 17.

frequency divider

By adjusting the length of the timing cycle, the basic circuit of Figure 10 can be made to operate as a frequency divider. Figure 18 illustrates a divide-by-3 circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

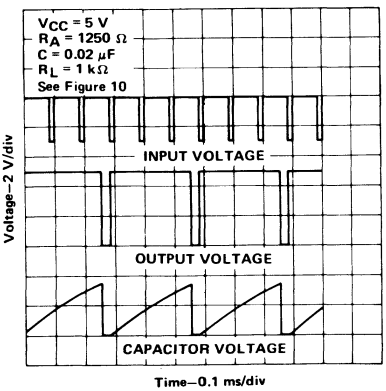
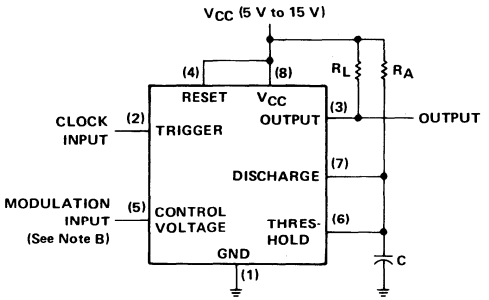


FIGURE 18–DIVIDE-BY-THREE CIRCUIT WAVEFORMS

TYPICAL APPLICATION DATA

pulse-width modulation



NOTE B: The modulating signal may be direct or capacitively coupled to the control voltage terminal. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

FIGURE 19–CIRCUIT FOR PULSE-WIDTH MODULATION

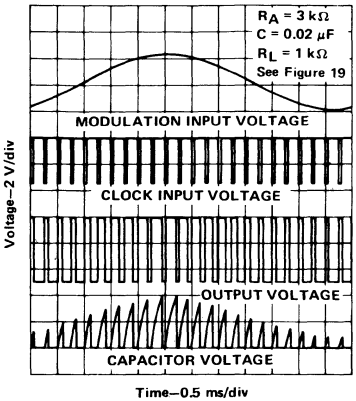
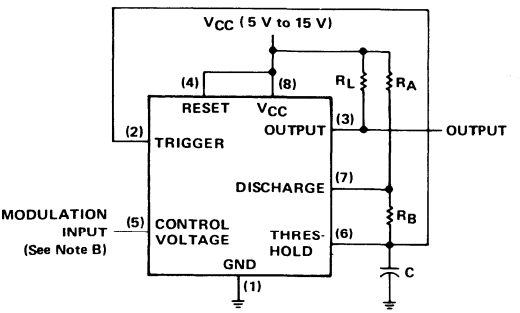


FIGURE 20–PULSE-WIDTH MODULATION WAVEFORMS

The operation of the timer may be modified by modulating the internal threshold and trigger voltages. This is accomplished by applying an external voltage (or current) to the control voltage pin. Figure 19 is a circuit for pulse-width modulation. The monostable circuit is triggered by a continuous input pulse train and the threshold voltage is modulated by a control signal. The resultant effect is a modulation of the output pulse width, as shown in Figure 20. A sine-wave modulation signal is illustrated, but any wave-shape could be used.

TYPICAL APPLICATION DATA

pulse-position modulation



NOTE B: The modulating signal may be direct or capacitively coupled to the control voltage terminal. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

FIGURE 21–CIRCUIT FOR PULSE-POSITION MODULATION

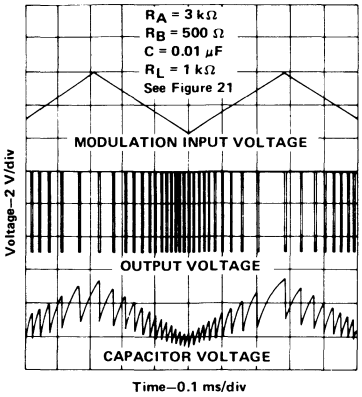
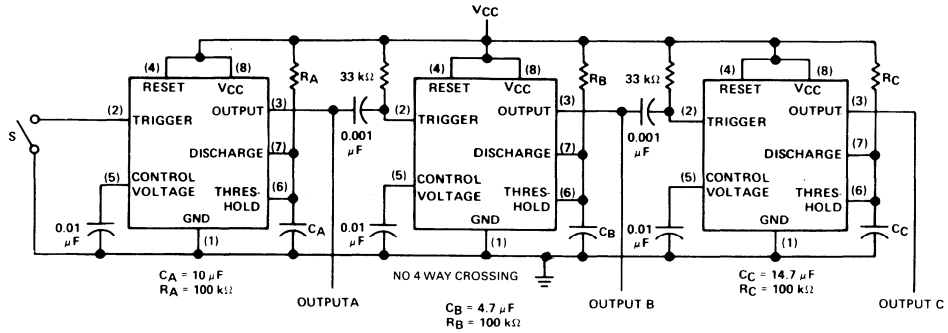


FIGURE 22–PULSE POSITION-MODULATION WAVEFORMS

Any of these timers may be used as a pulse-position modulator as shown in Figure 21. In this application, the threshold voltage, and thereby the time delay, of a free-running oscillator is modulated. Figure 22 shows such a circuit, with a triangular-wave modulation signal, however, any modulating wave-shape could be used.

TYPICAL APPLICATION DATA

sequential timer



S closes momentarily at t = 0.

FIGURE 23–SEQUENTIAL TIMER CIRCUIT

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications such as test equipment require activation of test signals in sequence. These timing circuits may be connected to provide such sequential control. The timers may be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 23 illustrates a sequencer circuit with possible applications in many systems and Figure 24 shows the output waveforms.

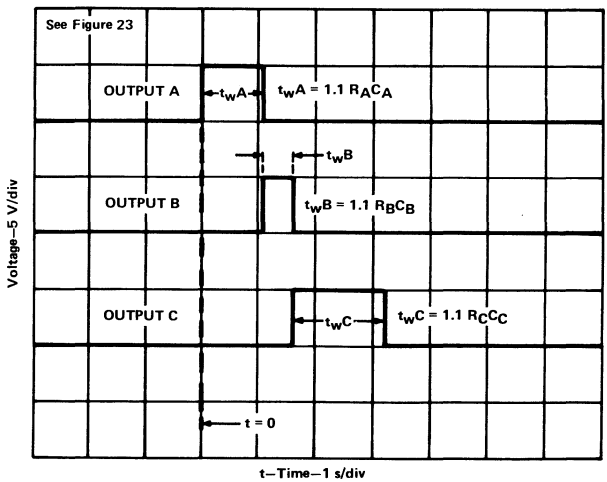


FIGURE 24–SEQUENTIAL TIMER WAVEFORMS

TYPES SE556, SE556C, SA556, NE556
DUAL PRECISION TIMERS

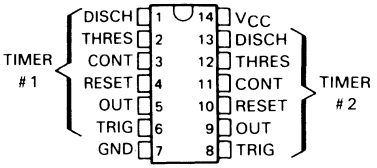
D2440, APRIL 1978–REVISED OCTOBER 1983

- Two Precision Timing Circuits per Package
- Astable or Monstable Operation
- TTL-Compatible Output can Sink or Source up to 150 mA
- Active Pull-Up or Pull-Down
- Designed to be Interchangeable with Signetics SE556, SE556C, SA556, NE556

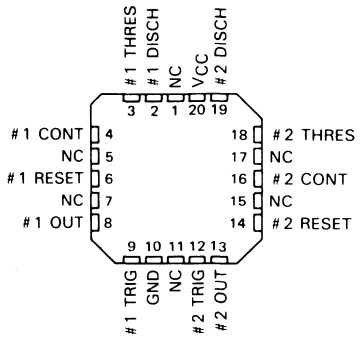
APPLICATIONS

Precision Timer from Microseconds to Hours
Sequential Timer
Pulse-Shaping Circuit
Pulse Generator
Missing-Pulse Detector
Tone-Burst Generator
Pulse-Width Modulator
Time-Delay Circuit
Frequency Divider
Pulse-Position Modulator
Appliance Timer
Touch-Tone Encoder
Industrial Controls

SE556 . . . J
SE556C, SA556, NE556 . . . D, J, OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



SE556 . . . FK PACKAGE
(TOP VIEW)



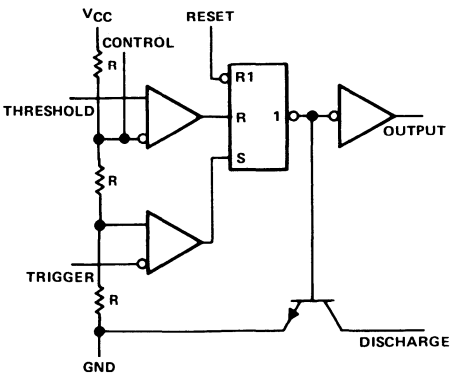
NC – No internal correction

description

These devices provide two monolithic, independent timing circuits of the SE555, SE555C, SA555, or NE555 type in each package. These circuits can be operated in the astable or the monostable mode with external resistor-capacitor timing control. The basic timing provided by the RC time constant may be actively controlled by modulating the bias of the control voltage input.

The threshold and trigger levels are normally two-thirds and one-third respectively of V_{CC}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

functional block diagram (each timer)



Reset can override Trigger, which can override Threshold.

The SE556 and SE556C are characterized for operation over the full military range of −55°C to 125°C. The SA556 is characterized for operation from −40°C to 85°C, and the NE556 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	< 1/3 V_{DD}	Irrelevant	High	Off
High	> 1/3 V_{DD}	> 2/3 V_{DD}	Low	On
High	> 1/3 V_{DD}	< 2/3 V_{DD}	As previously established	

†Voltage levels shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Input voltage (control voltage, reset, threshold, trigger) . . . . . V_{CC}
Output current . . . . . ±225 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 600 mW
Operating free-air temperature range: SE556, SE556C . . . . . −55°C to 125°C
SA556 . . . . . −40°C to 85°C
NE556 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: FK, or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J package, SE556 and SE556C chips are alloy mounted, SA556 and NE556 chips are glass mounted.

recommended operating conditions

	SE556		SE556C		SA556		NE556		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	4.5	18	4.5	16	4.5	16	4.5	16	V
Input voltage (control voltage, reset, threshold, trigger)		V_{CC}		V_{CC}		V_{CC}		V_{CC}	V
Output current		±200		±200		±200		±200	mA
Operating free-air temperature, T_A	−55	125	−55	125	−40	85	0	70	°C

electrical characteristics at 25°C free-air temperature, V_{CC} = 5 V to 15 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE556			SE556C, SA556 NE556			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level	V_{CC} = 15 V		9.4	10	10.6	8.8	10	11.2	V
	V_{CC} = 5 V		2.7	3.3	4	2.4	3.3	4.2	
Threshold current (see Note 1)				30	250		30	250	nA
Trigger voltage level	V_{CC} = 15 V		4.8	5	5.2	4.5	5	5.6	V
	V_{CC} = 5 V		1.45	1.67	1.9	1.1	1.67	2.2	
Trigger current	Trigger at 0 V			0.5	0.9		0.5	2	μA
Reset voltage level			0.4	0.7	1	0.4	0.7	1	V
Reset current	Reset at V_{CC}			0.1	0.4		0.1	0.4	mA
	Reset at 0 V			−0.4	−1		−0.4	−1	
Discharge switch off-state current				20	100		20	100	nA
Control voltage (open-circuit)	V_{CC} = 15 V		9.6	10	10.4	9	10	11	V
	V_{CC} = 5 V		2.9	3.3	3.8	2.6	3.3	4	
Low-level output voltage	V_{CC} = 15 V	I_{OL} = 10 mA		0.1	0.15		0.1	0.25	V
		I_{OL} = 50 mA		0.4	0.5		0.4	0.75	
		I_{OL} = 100 mA		2	2.2		2	2.5	
		I_{OL} = 200 mA		2.5			2.5		
	V_{CC} = 5 V	I_{OL} = 5 mA		0.05	0.15		0.05	0.25	
		I_{OL} = 8 mA		0.1	0.2		0.25	0.3	
High-level output voltage	V_{CC} = 15 V	I_{OH} = −100 mA	13	13.3		12.75	13.3		V
		I_{OH} = −200 mA		12.5			12.5		
	V_{CC} = 5 V	I_{OH} = −100 mA	3	3.3		2.75	3.3		
Supply current	Output low, No load	V_{CC} = 15 V		20	24		20	30	mA
		V_{CC} = 5 V		6	10		6	12	
	Output high, No load	V_{CC} = 15 V		18	20		18	26	
		V_{CC} = 5 V		4	8		4	10	

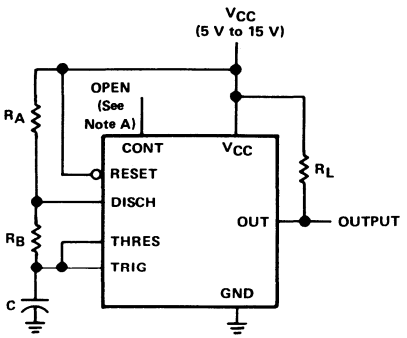
NOTE 1: This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 1. For example, when V_{CC} = 5 V the maximum value is R = R_A + R_B = 3.4 MΩ and for V_{CC} = 15 V the maximum value for R_A + R_B = 10 MΩ.

operating characteristics, V_{CC} = 5 V and 15 V

PARAMETER		TEST CONDITIONS†	SE556			SE556C, SA556 NE556			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval‡ *	Each timer, monostable§	T_A = 25°C		0.5	1.5		1	3	%
	Each timer, astable¶			1.5			2.25		
	Timer 1 — Timer 2			±0.5			±1		
Temperature coefficient of timing interval *	Each timer, monostable§	T_A = MIN to MAX		30	100		50		ppm/°C
	Each timer, astable¶			90			150		
	Timer 1 — Timer 2			±10			±10		
Supply voltage sensitivity of timing interval *	Each timer, monostab;e§	T_A = 25°C		0.05	0.2		0.1	0.5	%/V
	Each timer, astable¶			0.15			0.3		
	Timer 1— Timer 2			±0.1			±0.2		
Output pulse rise time *		C_L = 15 pF, T_A = 25°C		100	200		100	300	ns
Output pulse fall time *				100	200		100	300	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡Timing interval error is defined as the difference between the measured value and the nominal value computed by the formula: t_w = 1.1 R_AC.
§Values specified are for a device in a monostable circuit similar to Figure 2, with component values as follow: R_A = 2 kΩ to 100 kΩ, C = 0.1 μF.
¶Values specified are for a device in an astable circuit similar to Figure 1, with component values as follow: R_A = 1 kΩ to 100 kΩ, C = 0.1 μF.
*For SE556 and SE556C these parameters are guaranteed but not tested.

TYPICAL APPLICATION DATA



NOTE A: Bypassing the control voltage input to ground with a capacitor may improve operation. This should be evaluated for individual applications.

FIGURE 1–CIRCUIT FOR ASTABLE OPERATION

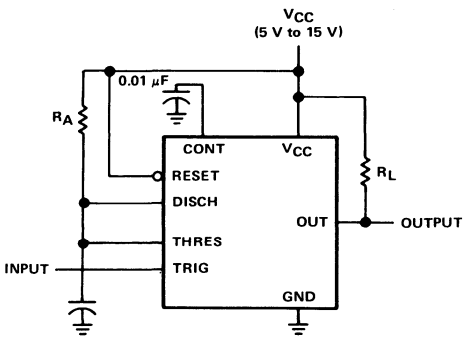


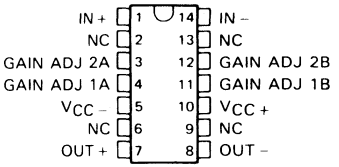
FIGURE 2–CIRCUIT FOR MONOSTABLE OPERATION

TYPES SE592, NE592, NE592A DIFFERENTIAL VIDEO AMPLIFIERS

D2667, FEBRUARY 1984

- **90-MHz Bandwidth**
- **Adjustable Gain to 400**
- **No Frequency Compensation Required**
- **Adjustable Passband**
- **Designed to be Interchangeable with Signetics SE592 and NE592**
- **Pin compatible with Signetics SE592 and NE592**

D–14, J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices are monolithic two-stage amplifiers with differential inputs and differential outputs.

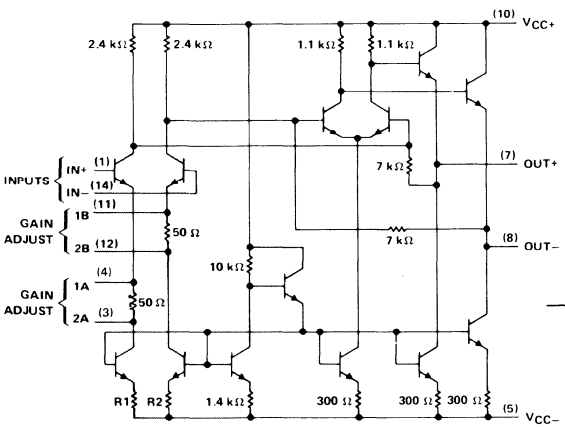
Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the devices to drive capacitive loads, and all stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

Fixed differential amplification of 100 or 400 may be selected without external components; or amplification may be adjusted from 0 to 400 by the use of a single external resistor connected between the gain-adjustment pins 1A and 1B. External frequency-compensating components are not required for any gain option.

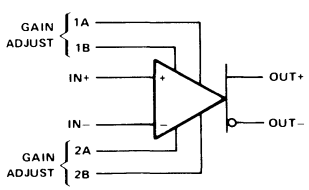
The devices are particularly useful in magnetic-tape or disc-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

The SE592 is characterized for operation over the full military temperature range of −55°C to 125°C. The NE592 and NE592A are characterized for operation from 0°C to 70°C.

schematic



symbol



Device	Temp. Range	AVD Range
SE592	−55 to 125 °C	300-500
NE592	0 to 70 °C	250-600
NE592	0 to 70 °C	400-600

All resistor values shown are in ohms and nominal.
In NE592 or SE592, R1 = 500 Ω, R2 = 500 Ω.
In NE592A, R1 = 600 Ω, R2 = 600 Ω.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage V_{CC-} (see Note 1) . . . . . −8 V
Differential input voltage . . . . . ±5 V
Common-mode input voltage . . . . . ±6 V
Output current . . . . . 10 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values except differential input voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in Section 2. In the J package, SE592 chips are alloy mounted, NE592 and NE592A chips are glass mounted.

recommended operating conditions

	SE592			NE592 NE592A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}	3	6	8	3	6	8	V
Supply voltage, V_{CC-}	−3	−6	−8	−3	−6	−8	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics at 25°C operating free-air temperature, V_{CC+} = 6 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	SE592			UNIT
					MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_L = 2 kΩ	1	300	400	500	V/V
				2	90	100	110	
BW	Bandwidth (−3 dB)	2	V_{OPP} = 1 V	1		40		MHz
				2		90		
I_{IO}	Input offset current			1, 2, or 3		0.4	3	μA
I_{IB}	Input bias current			1, 2, or 3		9	20	μA
V_{ICR}	Common-mode input voltage range	3		1, 2, or 3	±1			V
V_{OC}	Common-mode output voltage	1	R_L = ∞	1, 2, or 3	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1	V_{IO} = 0, R_L = ∞	1			1.5	V
				2			1	
				3		0.35	0.75	
V_{OPP}	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	1, 2, or 3	3	4		V
r_i	Input resistance			1		4		kΩ
				2	20	30		
r_o	Output resistance					20		Ω
C_i	Input capacitance					2		pF
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	60	86		dB
		3	V_{IC} = ±1 V, f = 5 MHz	2		60		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50	70		dB
V_n	Broadband equivalent noise voltage	4	BW = 1 kHz to 10 MHz	1, 2, or 3		12		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V	1		7.5		ns
				2		6	10	
t_r	Rise time	2	ΔV_O = 1 V	1		10.5		ns
				2		4.5	10	
$I_{sink(max)}$	Maximum output sink current‡			1, 2, or 3	3	4		mA
I_{CC}	Supply current		No load, No signal	1, 2, or 3		18	24	mA

† The gain option is selected as follows:
Gain Option 1 . . Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2 . . Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.
Gain Option 3 . . All Gain Adjust pins are open.

‡ For interchangeability considerations it should be kept in mind that this parameter is not guaranteed by all major manufacturers of SE592 as of the publication of this data sheet.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 6 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	SE592 MIN	SE592 TYP	SE592 MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V	1	200		600	V/V
				2	80		120	
I_{IO}	Input offset current			1 or 2			5	μA
I_{IB}	Input bias current			1 or 2			40	μA
V_{ICR}	Common-mode input voltage range	3		1 or 2	±1			V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1			1.5	V
				2			1.2	
				3			1	
V_{OPP}	Maximum output voltage peak-to-peak swing	1	R_L = 2 kΩ	1 or 2	2.5			V
r_i	Input resistance			2	8			kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	50			dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50			dB
$I_{sink(max)}$	Maximum output sink current			1, 2, or 3	2.5			mA
I_{CC}	Supply current	1	No load, No signal	1, 2, or 3			27	mA

† The gain option is selected as follows:
Gain Option 1 . . Gain Adjust pin 1A is connected to pin 1B; pins 2A and 2B are open.
Gain Option 2 . . Gain Adjust pin 2A is connected to pin 2B; pins 1A and 1B are open.
Gain Option 3 . . All Gain Adjust pins are open.

electrical characteristics at 25°C operating free-air temperature, V_{CC+} = 6 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	NE592			NE592A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
A_{VD}	Large signal differential voltage amplification	1	V_{OPP} = 3 V, R_L = 2 kΩ	1	250	400	600	400	440	600	V/V
				2	80	100	120	80	100	120	
BW	Bandwidth (−3 dB)	2	V_{OPP} = 1 V	1		40			40		MHz
				2		90			90		
I_{IO}	Input offset current			1, 2, or 3		0.4	5		0.4	5	μA
I_{IB}	Input bias current			1, 2, or 3		9	30		10	30	μA
V_{ICR}	Common-mode input voltage range	3		1, 2, or 3	±1			±1			V
V_{OC}	Common-mode output voltage	1	R_L = ∞	1, 2, or 3	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1 or 2			1.5			1.5	V
				3		0.35	0.75		0.35	0.75	
V_{OPP}	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	1, 2, or 3	3	4		3	4		V
r_i	Input resistance			1		4			4		kΩ
				2	10	30		10	30		
r_o	Output resistance					20			20		Ω
C_i	Input capacitance					2			2		pF
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	60	86		60	86		dB
		3	V_{IC} = ±1 V, f = 5 MHz	2		60			60		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50	70		50	70		dB
V_n	Broadband equivalent noise voltage	4	BW = 1 kHz to 10 MHz	1, 2, or 3		12			12		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V	1		7.5			7.5		ns
				2		6	10		6	10	
t_r	Rise time	2	ΔV_O = 1 V	1		10.5			10.5		ns
				2		4.5	12		4.5	12	
$I_{sink(max)}$	Maximum output sink current‡			1, 2, or 3	3	4		3	4		mA
I_{CC}	Supply current		No load, No signal	1, 2, or 3		18	24		19	24	mA

† The gain option is selected as follows:
Gain Option 1 . . . Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2 . . . Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.
Gain Option 3 . . . All Gain Adjust pins are open.

‡ For interchangeability considerations it should be kept in mind that this parameter is not guaranteed by all major manufacturers of NE592 as of the publication of this data sheet.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 6 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	NE592			NE592A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V	1	250		600	400		600	V/V
				2	80		120	80		120	
I_{IO}	Input offset current			1 or 2			6			6	μA
I_{IB}	Input bias current			1 or 2			40			40	μA
V_{ICR}	Common-mode input voltage range	3		1 or 2	±1			±1			V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1 or 2			1.5			1.5	V
				3			1			1	
V_{OPP}	Maximum output voltage peak-to-peak swing	1	R_L = 2 kΩ	1 or 2	2.8			2.8			V
r_i	Input resistance			2	8			8			kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	50			50			dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50			50			dB
$I_{sink(max)}$	Maximum output sink current			1, 2, or 3				2.8	4		mA
I_{CC}	Supply current	1	No load, No signal	1, 2, or 3			27			27	mA

† The gain option is selected as follows:
Gain Option 1 . . Gain Adjust pin 1A is connected to pin 1B; pins 2A and 2B are open.
Gain Option 2 . . Gain Adjust pin 2A is connected to pin 2B; pins 1A and 1B are open.
Gain Option 3 . . All Gain Adjust pins are open.

PARAMETER MEASUREMENT INFORMATION

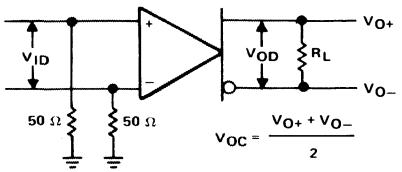


FIGURE 1

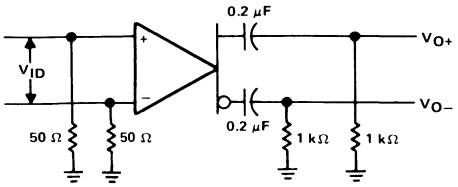


FIGURE 2

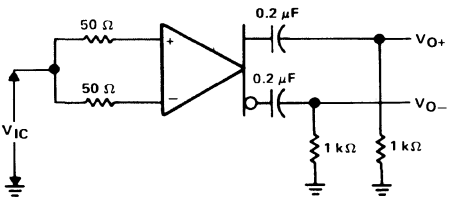


FIGURE 3

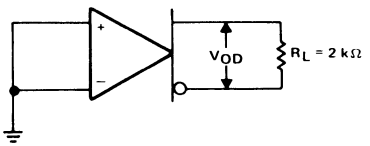


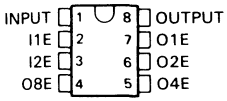
FIGURE 4

TYPES TL010I, TL010C
ADJUSTABLE-RATIO CURRENT MIRRORS

D2738, SEPTEMBER 1983

- **33 Distinct Input-to-Output Emitter Ratios from 3:1 to 1:15**
- **Wide Input Current Range: 1 μA to 3 mA**
- **35-Volt Output Capability**
- **High Output Impedance**

P DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TL010 is a Wilson current mirror that provides output current in a selectable fixed ratio to the input current. The ratio is substantially independent of changes in load, voltages, and temperature. Selecting the ratio consists of connecting appropriate input emitter pins and output emitter pins to ground as shown in Figure 1.

The TL010 is designed to operate with up to 3 milliamperes input current if all three input emitter pins are used. It will also operate at voltages up to 35 volts.

The TL010I is characterized for operation from −40°C to 85°C. The TL010C is characterized for operation from 0°C to 70°C.

typical values of current ratio at T_A = 25°C

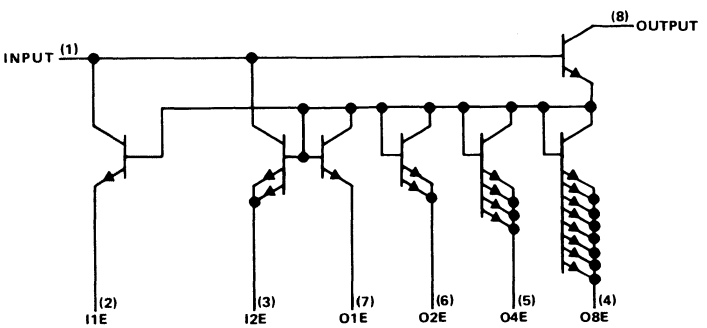
EMITTER RATIO m:n†	CURRENT RATIO $h_F = I_O/I_I$
1:15	14.1
1:14	13.2
1:13	12.3
1:12	11.4
1:11	10.5
1:10	9.55
1:9	8.62
1:8	7.72
2:15	7.23
1:7	6:71
2:13	6.29

EMITTER RATIO m:n†	CURRENT RATIO $h_F = I_O/I_I$
1:6	5.78
2:11	5.34
1:5	4.82
3:14	4.53
2:9	4.38
3:13	4.21
1:4	3.89
3:11	3.57
2:7	3:40
3:10	3:25
1:3	2.90

EMITTER RATIO m:n†	CURRENT RATIO $h_F = I_O/I_I$
3:8	2.61
2:5	2.43
3:7	2.26
1:2	1.98
3:5	1.64
2:3	1.45
3:4	1.32
1:1	0.99
3:2	0.663
2:1	0.50
3:1	0.332

†m is the number of input emitters used, n is the number of output emitters used.

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Output voltage (see Note 1) . . . . . 45 V
Input current . . . . . 5 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 725 mW
Operating free-air temperature range: TL010I . . . . . −40°C to 85°C
TL010C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Input and output voltages are with respect to the common terminal. Neither voltage should be more negative than −0.3 V.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 5.8 mW/°C.

recommended operating conditions

	TL010I		TL010C		UNIT
	MIN	MAX	MIN	MAX	
Output voltage, V_O	5	35	5	35	V
Input voltage, V_I	0.6	1.7	0.65	1.6	V
Input current per input emitter, I_I	0.001	1	0.001	1	mA
Operating free-air temperature, T_A	−40	85	0	70	°C

electrical characteristics over recommended ranges of operating free-air temperature and output voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL010I			TL010C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_I	Input voltage	I_I = m × 1 μA			1			1		V
		I_I = m × 10 μA			1.1			1.1		
		I_I = m × 100 μA			1.25			1.25		
		I_I = m × 1 mA			1.4			1.4		
h_F	Current ratio (I_O/I_I)	I_I = MIN to MAX	m:n = 1:8	6.97	7.72	8.13	7.05	7.72	8.13	
			m:n = 1:4	3.61	3.89	4.05	3.64	3.89	4.05	
			m:n = 1:2	1.84	1.98	2.07	1.88	1.98	2.07	
			m:n = 1:1	0.89	0.99	1.08	0.94	0.99	1.04	
			m:n = 2:1	0.46	0.50	0.56	0.475	0.50	0.525	
α_{hF}	Temperature coefficient of current ratio	I_I = MIN to MAX				300			300	ppm/°C
	Output-to-input isolation	I_I = MIN to MAX,	f = 1 kHz	60			60			dB
$V_{O(th)}$	Output threshold voltage§	I_I = MIN to MAX	T_A = MIN		1.1			1.05		V
			T_A = 25°C		1			1		
r_o	Output resistance¶	F = 1 kHz	I_I = m × 10 μA		200 m/n			200 m/n		MΩ
			I_I = m × 100 μA		20 m/n			20 m/n		
			I_I = m × 1 mA		2 m/n			2 m/n		
f_{max}	Maximum operating frequency#	I_I = m × 1 mA, R_L = 500 Ω		10			10			MHz

† m is the number of input emitters, n is the number of output emitters. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C.
§ Output threshold voltage is the voltage at which the current ratio is equal to 90% of its value at V_O = 15 V.
¶ The output resistance is directly proportional to the number of input emitters divided by the number of output emitters (m/n).
# Maximum operating frequency is the frequency at which the output current is down 3 dB from its low-frequency value.

TYPICAL APPLICATION INFORMATION

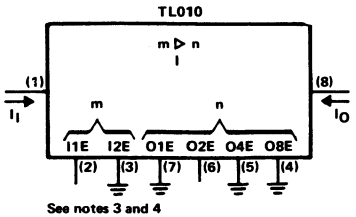


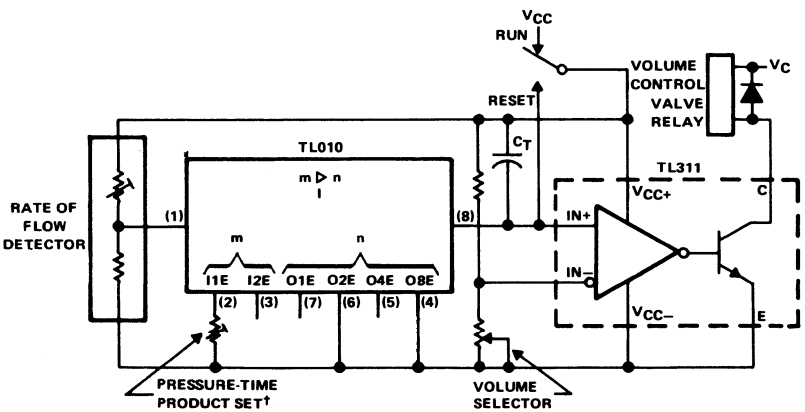
FIGURE 1–CURRENT MIRROR SET FOR A CURRENT RATIO OF 2:13

NOTES: 3. Selected emitters must be grounded as close as possible to the package to avoid unstable device behavior.
Using the fixed-Beta model, the current ratio for a current mirror of m input emitters and n output emitters may be calculated as

$$\frac{I_O}{I_I} = \frac{\beta^2 n + \beta(n+m)}{\beta^2 m + (\beta+1)(m+n)}$$

Second-order effects, such as on-chip self-heating, may slightly perturb the observed ratio from the calculated value.

4. At high current levels a small capacitor (270 pF) may be required between the input and output terminals to improve stability.



†Adjust for a mirror of 11.9

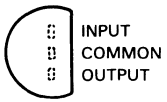
In this application of the TL010, the problem is to measure a precise volume of liquid flowing through a line and shut off the flow with a relay when the limit is reached. For the particular volume to be measured and the pressure detector used, a current gain of 11.9 is required. By setting the TL010 for a gain of 10 with the emitter selection, the exact gain of 11.9 may be obtained by adjusting the pressure-time product control.

SERIES TL011, TL012, TL014, TL021
FIXED-RATIO N-P-N CURRENT MIRRORS

D2614, NOVEMBER 1983

- **Wide Input Current Range:**
  1 μA to 1 mA
- **35-Volt Output Capability**
- **High Output Impedance**
- **Guaranteed Current-Ratio Tolerances over Full Temperature Range;**
  ±8% for I Suffix
  ±7% for C Suffix
- **Typically Less Than ±1% Error at 25°C**

LP PACKAGE
(TOP VIEW)



TEMPERATURE RANGE	INPUT-TO-OUTPUT CURRENT RATIO			
	1:1	1:2	1:4	2:1
−40°C to 85°C	TL011I	TL012I	TL014I	TL021I
0°C to 70°C	TL011C	TL012C	TL014C	TL021C

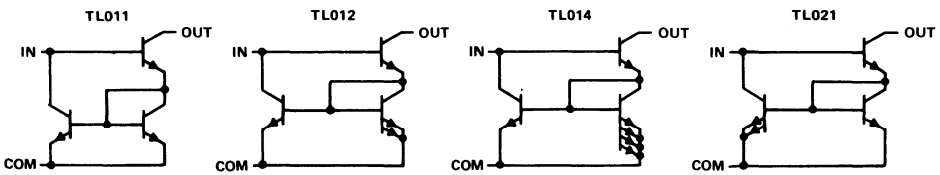
description

The TL011, TL012, TL014, and TL021 are Wilson current mirrors with output currents in fixed proportion to the input currents and substantially independent of changes in voltage, load, and temperature. These devices make use of the tight matching properties of identical bipolar transistors on a monolithic integrated circuit chip to achieve current-ratio accuracy typically better than 98%.

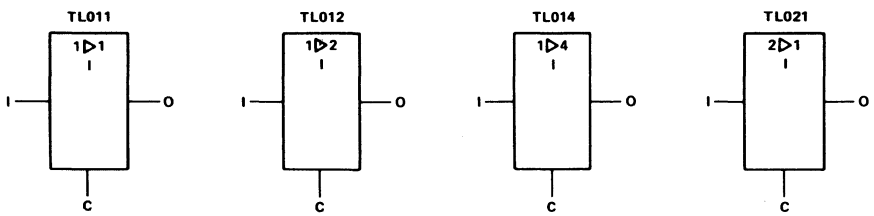
Current mirrors are used extensively in linear integrated circuit designs as active loads for operational-amplifier stages and as current sources for other stages. The TL011 family gives the designer this same capability with no sacrifice in accuracy or stability.

The TL011, TL012, and TL014 are designed to operate with input currents up to 1 milliampere and output voltage up to 35 volts. The TL021 is designed for 2 milliamperes and 35 volts.

schematics



symbols



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Output voltage (see Note 1) . . . . . 45 V
Input current . . . . . 5 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 775 mW
Operating free-air temperature range: TL011I, TL012I, TL014I, TL021I . . . . . −40°C to 85°C
TL011C, TL012C, TL014C, TL021C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Input and output voltages are with respect to the common terminal. Neither voltage should be more negative than −0.3 V.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 6.2 mW/°C.

recommended operating conditions

		TL0__I		TL0__C		UNIT
		MIN	MAX	MIN	MAX	
Output voltage, V_O		5	35	5	35	V
Input current, I_O	TL021	0.002	2	0.002	2	mA
	All others	0.001	1	0.001	1	
Operating free-air temperature, T_A		−40	85	0	70	°C

electrical characteristics over recommended ranges of operating free-air temperature and output voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TL011			TL012			TL014			TL021			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
V_I	Input voltage		I_I = 1 μA			1			1			1					V
			I_I = 2 μA												1		
			I_I = 10 μA			1.1			1.1			1.1					
			I_I = 20 μA												1.1		
			I_I = 100 μA			1.25			1.25			1.25					
			I_I = 200 μA												1.25		
			I_I = 1 mA			1.4			1.4			1.4					
			I_I = 2 mA												1.4		
h_F	Current ratio (I_O/I_I)	TLO_I	I_I = MIN to MAX‡		0.92	1	1.08	1.84	2	2.16	3.68	4	4.32	0.46	0.5	0.54	
		TLO_C			0.93	1	1.07	1.86	2	2.14	3.72	4	4.28	0.465	0.5	0.535	
α_{hF}	Temperature coefficient of current ratio		I_I = MIN to MAX			50			100			200			200		ppm/°C
	Output-to-input isolation		I_I = MIN to MAX,	f = 1 kHz	80			80			80			80			dB
$V_{O(th)}$	Output threshold voltage§	TLO_I	I_I = MIN to MAX	T_A = −40°C			1.35			1.35			1.35			1.35	V
		TLO_C		T_A = 0°C			1.25			1.25			1.25			1.25	
		All		T_A = 25°C			1.2			1.2			1.2			1.2	
r_o	Output resistance		f = 1 kHz	I_I = 10 μA		200			100			50					MΩ
				I_I = 20 μA											200		
				I_I = 100 μA		20			10			5					
				I_I = 200 μA											20		
				I_I = 1 mA		2			1			0.5					
				I_I = 2 mA											2		
f_{max}	Maximum operating frequency¶		I_I = MAX,	R_L = 500 Ω		10			10			10			10		MHz

†All typical values are at T_A = 25°C.
‡For test conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§Output threshold voltage is the voltage at which the current ratio is equal to 90% of its value at V_O = 15 V.
¶Maximum operating frequency is the frequency at which the output current is down 3 dB from its low frequency value.

TYPICAL CHARACTERISTICS

TL011
CURRENT RATIO
vs
FREE-AIR TEMPERATURE

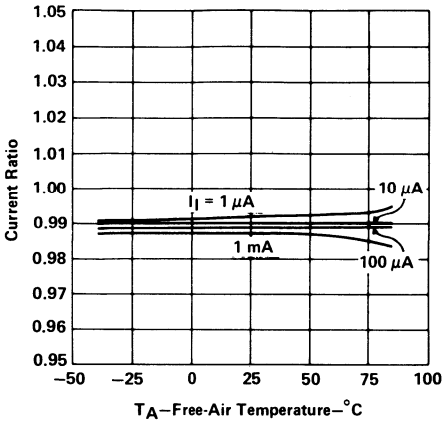


FIGURE 1

TL012
CURRENT RATIO
vs
FREE-AIR TEMPERATURE

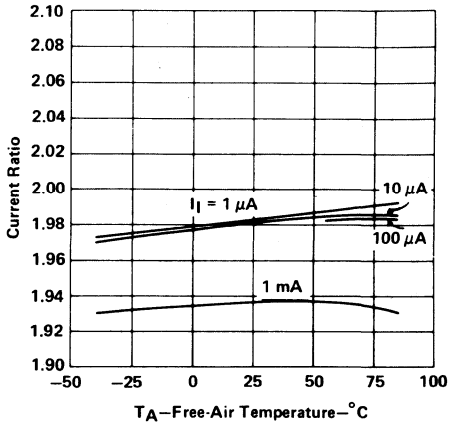


FIGURE 2

TL014
CURRENT RATIO
vs
FREE-AIR TEMPERATURE

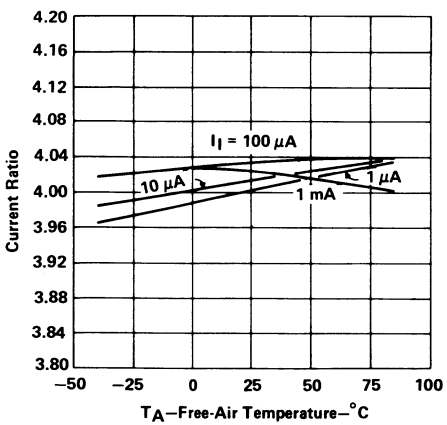


FIGURE 3

TL021
CURRENT RATIO
vs
FREE-AIR TEMPERATURE

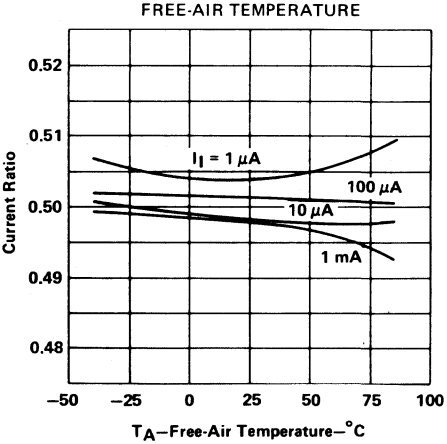
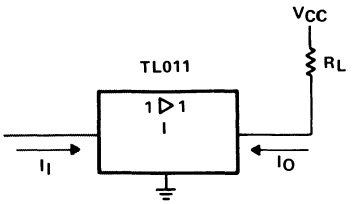


FIGURE 4

TYPICAL APPLICATIONS INFORMATION

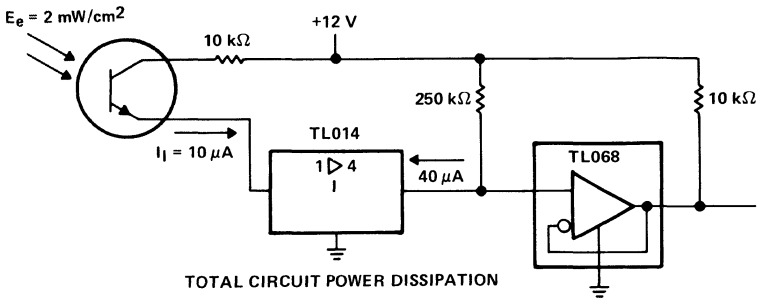


$I_O = I_I$

VARIATIONS IN R_L DO NOT AFFECT I_I OR I_O WHEN:

$$I_I = I_O < \frac{V_{CC} - V_{O(th)}}{R_L}$$

FIGURE 5–BASIC CURRENT BUFFER



TOTAL CIRCUIT POWER DISSIPATION

Idle condition: P_D = 1.5 mW typical
On condition: P_D = 12.5 mW typical
10 μA from phototransistor provides a V_O swing of 10 V at 1 mA.

FIGURE 6–PHOTOTRANSISTOR PREAMPLIFIER

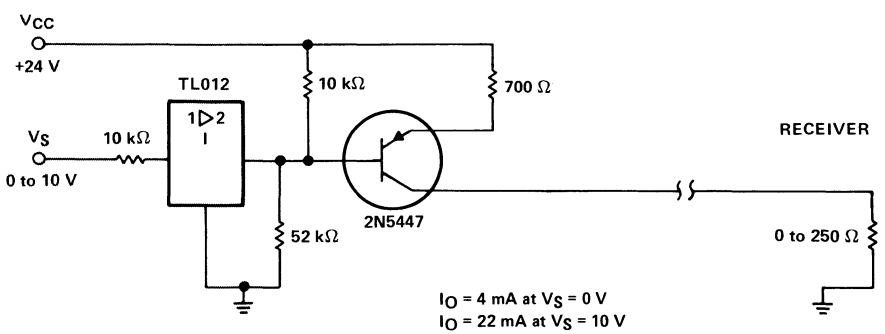


FIGURE 7–TWO-WIRE LINEAR CURRENT-MODE TRANSMITTER

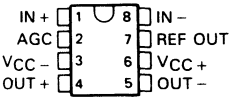
1183

TL026C
DIFFERENTIAL VIDEO AMPLIFIER WITH AGC

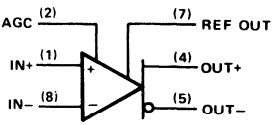
D2790, JUNE 1985

- Low Output Common-Mode Sensitivity to AGC Voltages
- Input and Output Impedances Independent of AGC Voltage
- Peak Gain . . . 38 dB Typ
- Wide AGC Range . . . 50 dB Typ
- 3-dB Bandwidth . . . 50 MHz
- Other Characteristics Similar to NE592 and uA733

JG, P, OR D
DUAL-IN-LINE PACKAGE
(TOP VIEW)



symbol



description

This device is a monolithic two-stage video amplifier with differential inputs and outputs.

Internal feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Variable gain based on signal summation provides large AGC control over a wide bandwidth with low harmonic distortion. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios. The gain may be electronically attenuated by applying a control voltage to the AGC pin. No external frequency compensation components are required.

This device is particularly useful in TV and radio IF and RF AGC circuits, as well as magnetic-tape and disk-file systems where AGC is needed. Other applications include video and pulse amplifiers where a large AGC range, wide bandwidth, low phase shift, and excellent gain stability are required.

The TL026C is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	8 V
Supply voltage, V_{CC-} (see Note 1)	−8 V
Differential input voltage	±5 V
Common-mode input voltage	±6 V
Output current	10 mA
Continuous total power dissipation at (or below) 25°C free-air temperature	500 mW
Operating free-air temperature	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P, D package	260°C

NOTE 1: All voltages are with respect to the midpoint between V_{CC+} and V_{CC-} except differential input and output voltages.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	3	6	8	V
Supply voltage, V_{CC-}	3	6	8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at 25 °C operating free-air temperature, $V_{CC\pm}$ = ±6 V, V_{AGC} = 0, REF OUT pin open (unless otherwise specified)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} 3 V, R_L 2 kΩ	65	85	105	V/V
ΔA_{VD}	Change in voltage amplification	1	V_{IPP} 28.5 mV, R_L 2 kΩ, V_{AGC} V_{ref} ±180 mV		50		dB
V_{ref}	Open-circuit voltage at REF OUT			1.3		1.5	V
BW	Bandwidth (3 dB)	2	V_{OPP} 1 V		50		MHz
I_{IO}	Input offset current				0.4	5	μA
I_{IB}	Input bias current				10	30	μA
V_{ICR}	Common-mode input voltage range	3		±1			V
V_{OC}	Common-mode output voltage	1	R_L ∞	3.25	3.75	4.25	V
ΔV_{OC}	Change in common-mode output voltage	1	V_{AGC} 0 to 2 V, R_L ∞			300	mV
V_{OO}	Output offset voltage	1	V_{ID} 0, R_L ∞			0.75	V
V_{OPP}	Maximum peak-to-peak output voltage swing	1	R_L 2 kΩ	3	4		V
r_i	Input resistance at AGC, IN+, or IN−			10	30		kΩ
r_o	Output resistance				20		Ω
CMRR	Common-mode rejection ratio	3	V_{IC} ±1 V, f 100 kHz	60	86		dB
		3	V_{IC} ±1 V, f 5 mHz		60		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} ±0.5 V, ΔV_{CC-} ±0.5 V	50	70		dB
V_n	Broadband equivalent noise voltage	4	BW 1 kHz to 10 MHz		12		μV
t_{pd}	Propagation delay time	2	ΔV_O 1 V		6	10	ns
t_r	Rise time	2	ΔV_O 1 V		4.5	12	ns
$I_{sink(max)}$	Maximum output sink current		V_{ID} 1 V, V_O 3 V	3	4		mA
I_{CC}	Supply current		No load, No signal		22	27	mA

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±6 V, V_{AGC} = 0, REF OUT pin open (unless otherwise specified)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_L = 2 kΩ	55		115	V/V
I_{IO}	Input offset current					6	μA
I_{IB}	Input bias current					40	μA
V_{ICR}	Common-mode input voltage range	3		±1			V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞			1.5	V
V_{OPP}	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	2.8			V
r_i	Input resistance at AGC, IN+, or IN−			8			kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	50			dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	50			dB
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V, V_O = 3 V	2.8	4		mA
I_{CC}	Supply current	1	No load, No signal			30	mA

PARAMETER MEASUREMENT INFORMATION

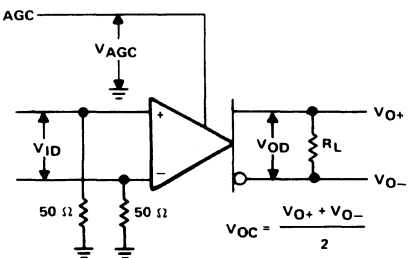


FIGURE 1

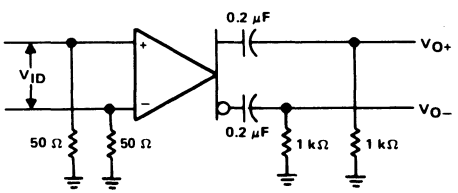


FIGURE 2

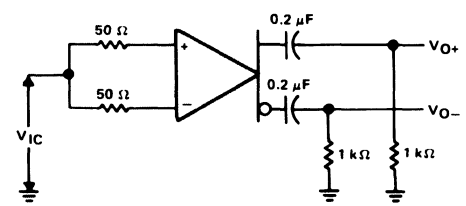


FIGURE 3

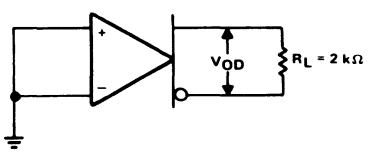


FIGURE 4

TYPICAL CHARACTERISTICS

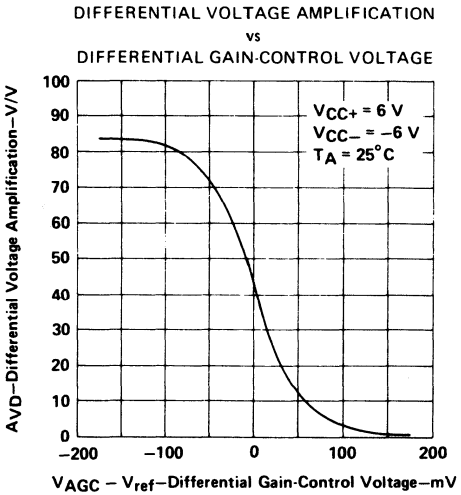


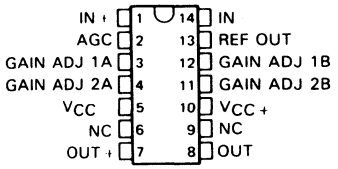
FIGURE 5

TL027C
DIFFERENTIAL VIDEO AMPLIFIER WITH AGC

D2888, JUNE 1985

- **Low Output Common-Mode Sensitivity to AGC Voltages**
- **Input and Output Impedances Independent of AGC Voltage**
- **Wide AGC Range . . . 50 dB Typ**
- **3-dB Bandwidth . . . 50 MHz**
- **Other Characteristics Similar to NE592 and uA733**

D, J, OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

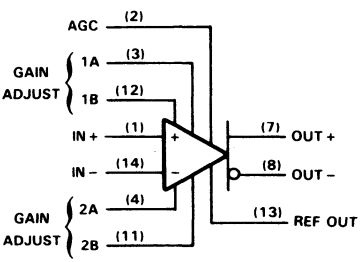


NC No internal connection

DEVICE FEATURES

	GAIN	AGC
Gain Option 1	50 dB	50 dB
Gain Option 2	38 dB	50 dB

symbol



description

This device is a monolithic two-stage video amplifier with differential inputs and outputs.

Internal feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Variable gain based on signal summation provides large AGC control over a wide bandwidth with low harmonic distortion. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios. The gain may be electronically attenuated by applying a control voltage to the AGC pins. No external frequency compensation components are required.

This device is particularly useful in TV and radio IF and RF AGC circuits, as well as magnetic-tape and disk-file systems where AGC is needed. Other applications include video and pulse amplifiers for which a large AGC range, wide bandwidth, low phase shift, and excellent gain stability are required.

The TL027C is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −8 V
Differential input voltage . . . . . ±5 V
Common-mode input voltage . . . . . ±6 V
Output current . . . . . 10 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (unless otherwise noted) . . . . . 500 mW
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to the midpoint between V_{CC+} and V_{CC-} except differential input and output voltages.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	3	6	8	V
Supply voltage, V_{CC-}	3	6	8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at 25°C operating free-air temperature, $V_{CC\pm}$ = ±6 V, V_{AGC} = 0, REF OUT pin open (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_L = 2 kΩ	1	200	300	400	V/V
				2	65	85	105	
ΔA_{VD1}	Change in voltage amplification	1	V_{IPP} = 7.5 mV, R_L = 2 kΩ, V_{AGC} = V_{ref} + 180 mV	1		−50		dB
ΔA_{VD2}	Change in voltage amplification	1	V_{IPP} = 28.5 mV, R_L = 2 kΩ, V_{AGC} = V_{ref} ± 180 mV	2		−50		dB
V_{ref}	Open-circuit voltage at REF OUT			1	1.3		1.5	V
BW	Bandwidth (−3 dB)	2	V_{OPP} = 1 V	1		20		MHz
				2		50		
I_{IO}	Input offset current			1 or 2		0.4	5	μA
I_{IB}	Input bias current			1 or 2		10	30	μA
V_{ICR}	Common-mode input voltage range	3		1 or 2	±1			V
V_{OC}	Common-mode output voltage	1	R_L = ∞	1 or 2	3.25	3.75	4.25	V
ΔV_{OC}	Change in common-mode output voltage	1	V_{AGC} = 0 to 2 V, R_L = ∞	1 or 2			300	mV
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1 or 2			0.75	V
V_{OPP}	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	1 or 2	3	4		V
r_i	Input resistance at AGC, IN+, or IN−			1		4		kΩ
				2	10	30		
r_o	Output resistance					20		Ω
C_i	Input capacitance					2		pF
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	60	86		dB
		3	V_{IC} = ±1 V, f = 5 MHz	2		60		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50	70		dB
V_n	Broadband equivalent input noise voltage	4	BW = 1 kHz to 10 MHz	1 or 2		12		μV
t_{pd}	Propagation delay time	2	ΔV_O = ±1 V	1		7.5		ns
				2		6	10	
t_r	Rise time	2	ΔV_O = ±1 V	1		10.5		ns
				2		4.5	12	
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V, V_O = 3 V	1 or 2	3	4		mA
I_{CC}	Supply current		No load, No signal	1 or 2		22	27	mA

† The gain option is selected as follows:
Gain Option 1. . .Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2. . .Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±6 V, V_{AGC} = 0, REF OUT pin open (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_L = 2 kΩ	1	150		450	V/V
				2	55		115	
I_{IO}	Input offset current			1 or 2			6	μA
I_{IB}	Input bias current			1 or 2			40	μA
V_{ICR}	Common-mode input voltage range	3		1 or 2	±1			V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1 or 2			1.5	V
V_{OPP}	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	1 or 2	2.8			V
r_i	Input resistance			2	8			kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	50			dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50			dB
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V, V_O = 3 V	1 or 2	2.8	4		mA
I_{CC}	Supply current	1	No load, No signal	1 or 2			30	mA

† The gain option is selected as follows:
Gain Option 1. . .Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2. . .Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.

PARAMETER MEASUREMENT INFORMATION

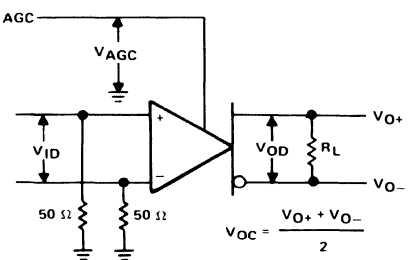


FIGURE 1

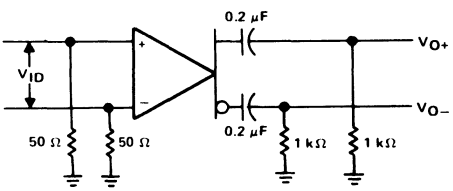


FIGURE 2

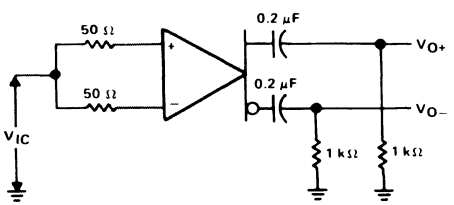


FIGURE 3

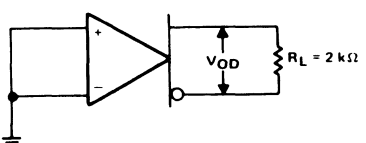


FIGURE 4

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
DIFFERENTIAL GAIN-CONTROL VOLTAGE

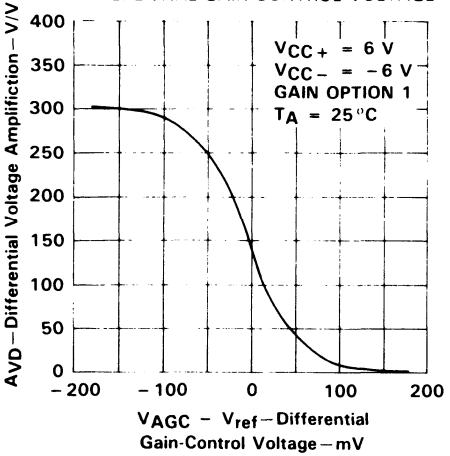


FIGURE 5

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
DIFFERENTIAL GAIN-CONTROL VOLTAGE

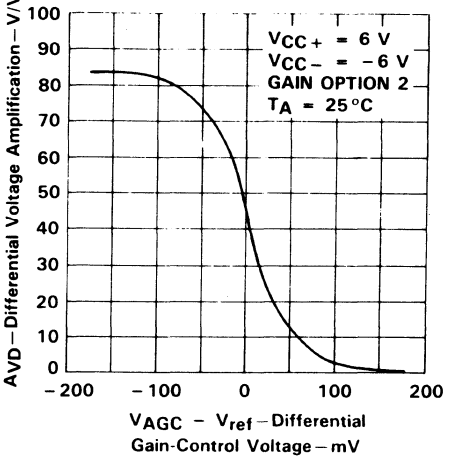


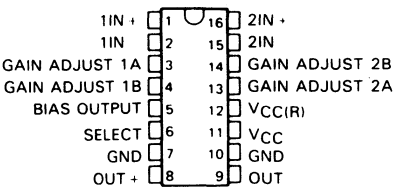
FIGURE 6

TL040C
2-CHANNEL MULTIPLEXED VIDEO AMPLIFIER

D3002, MARCH 1986

- **Designed for Use with the TL041 Magnetic Field Pulse Detector**
- **Wide Bandwidth . . . 20 MHz Typ**
- **Low Noise . . . Less than 5 μV Typ**
- **Independently Adjustable Channel Gains . . . Up to 450 Typ**
- **No Frequency Compensation Required**
- **Internal Voltage Source Eliminates External Components**
- **Input Channel Select Pin is Compatible with TTL and CMOS**
- **Low Power Dissipation . . . 150 mW Typ**

D OR N PACKAGE
(TOP VIEW)



CHANNEL SELECT TABLE

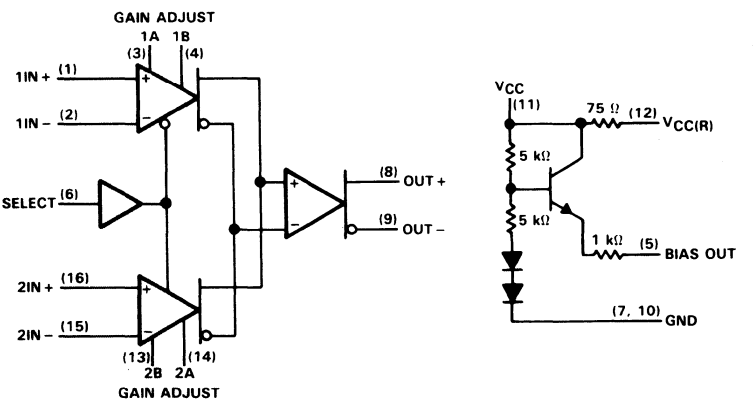
SELECT	CHANNEL
L	1
H	2

description

The TL040 is a two-channel multiplexed video amplifier designed for use with magnetic pulse detectors in streaming tape drives. The circuit design eliminates many external components, and the D package allows substantial reduction in circuit board area. The gain of each channel is a function of the resistance across its gain-adjust pins (A-B) with maximum gain occurring when the terminals are shorted.

The $V_{CC(R)}$ pin provides supply voltage decoupling required by some designs. The BIAS OUT pin provides a voltage source for other circuits that is approximately equal to 1/2 V_{CC}.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1) . . . . . 14 V
Input voltage range . . . . . −0.2 V to V_{CC} + 0.2 V
Continuous total power dissipation . . . . . 600 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltages except differential voltages are with respect to the ground terminals.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}	10.8	12	13.2	V
Common-mode input voltage (diff inputs), V_{IC}	5	6	7	V
High-level input voltage, SELECT input, V_{IH}	2			V
Low-level input voltage, SELECT input, V_{IL}			0.8	V
Output sink current (diff outputs), I_{sink}			1.5	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics of selected channel at T_A = 25°C, V_{CC} = 12 V, R_{AB} = 0, R_L = 2 kΩ (unless otherwise noted)

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1		300	450	600	V/V
	Channel amplification mismatch	1			1%		
	Large-signal differential voltage attenuation	1	ΔV_I = 50 mV on unselected input		60		dB
V_{OC}	Common-mode output voltage	1	$R_L = \infty$		8		V
V_{OPP}	Maximum peak-to-peak output voltage swing	1			4		V
BW	Bandwidth (−3 dB)	2			20		MHz
I_{IO}	Input offset current	1			0.2	3	μA
I_{IB}	Input bias current	1			5	17	μA
V_{OD}	Differential output voltage	1	$R_L = \infty$, V_{ID} = 0		0.75		V
r_i	Input resistance (differential inputs)				4		kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = 5 V to 7 V	60	80		dB
k_{SVR}	Supply-voltage rejection ratio (ΔV_{CC} ΔV_{IO})	4	V_{CC} = 10.8 V to 13.2 V	50	70		dB
V_n	Broadband equivalent input noise voltage	4			< 5		μV
I_{IH}	High-level input current, Select input		V_{IH} = 2.7 V			−0.4	mA
I_{IL}	Low-level input current, Select input		V_{IL} = 0.4 V			20	μA
t_{pd}	Propagation delay time (differential inputs)	2	ΔV_O = 1 V		15		ns
t_r	Output rise time	2	ΔV_O = 1 V		20		ns
I_{CC}	Supply current	1			10	15	mA
	Bias output voltage	1		5	6	7	V

PARAMETER MEASUREMENT INFORMATION

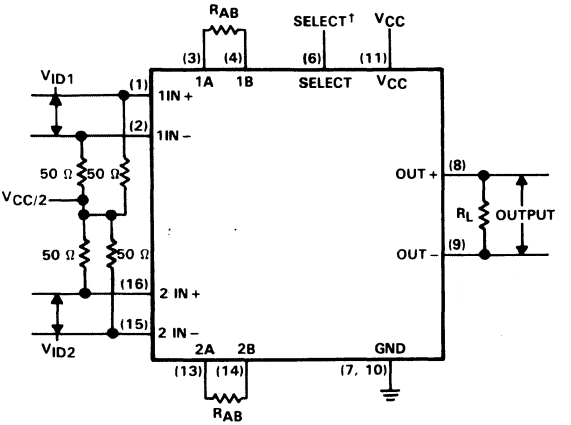


FIGURE 1

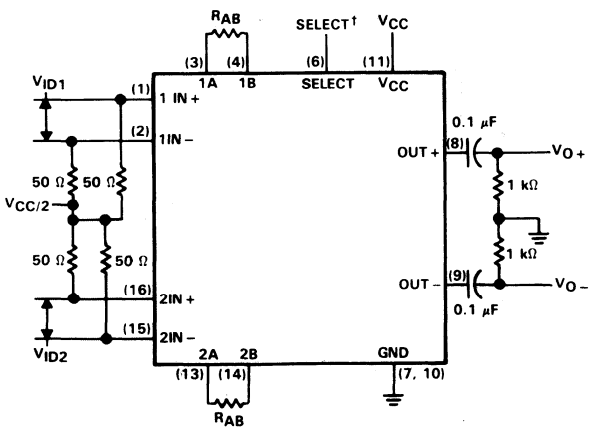


FIGURE 2

†Select input must be at proper logic level to select desired input channel.

PARAMETER MEASUREMENT INFORMATION (continued)

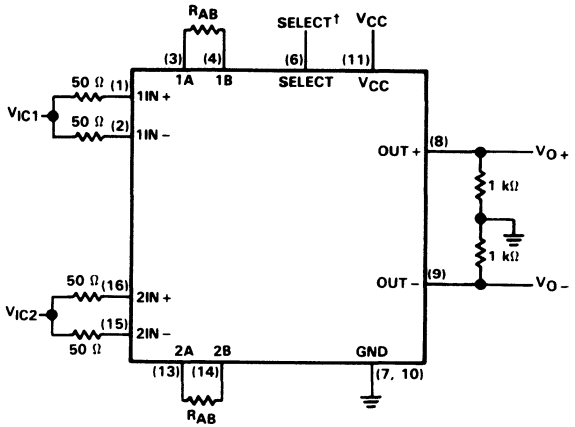


FIGURE 3

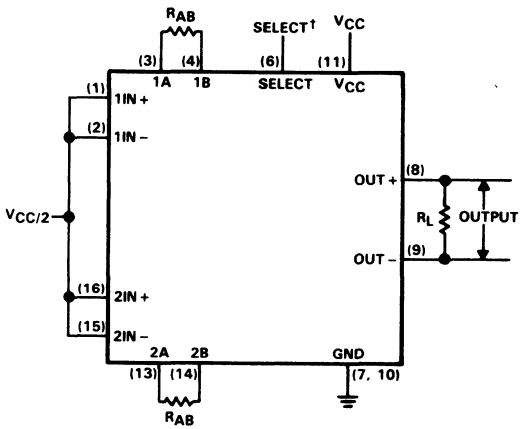


FIGURE 4

†Select input must be at proper logic level to select desired input channel.

TYPICAL CHARACTERISTICS

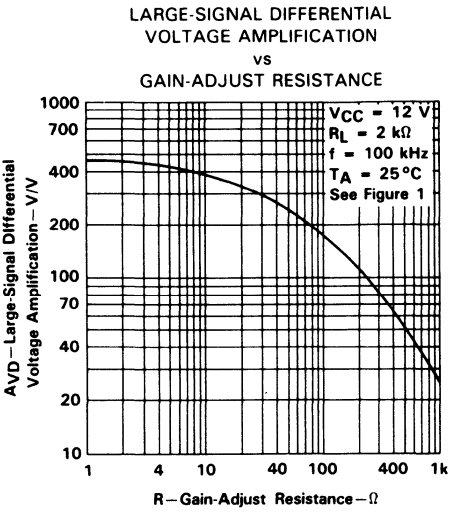


FIGURE 5

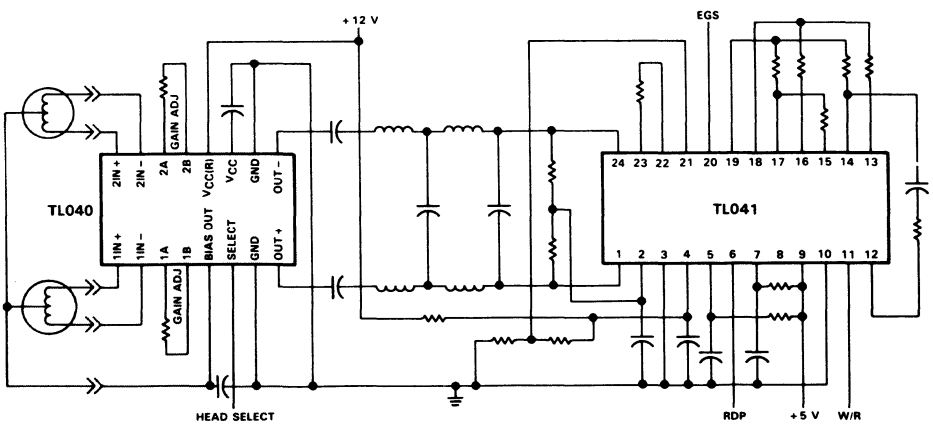
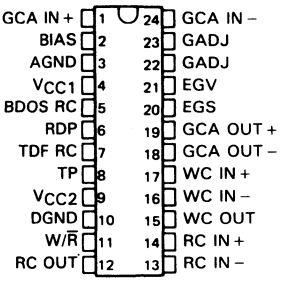


FIGURE 6. READ SIGNAL CIRCUIT FOR A STREAMING TAPE DRIVE

D3024, AUGUST 1987

- **Designed for Signal Processing in Streaming-Tape Memory Units in Combination with TL040 Two-Channel Video Amplifier**
- **Space-Saving LSI Circuits Include:**
  - **Two High-Speed Differential Comparators**
  - **Time-Domain Filter**
  - **Bidirectional One-Shot Multivibrator**
  - **Gain-Controlled Video Amplifier with Differential Inputs and Outputs**
- **Amplifier and Comparator Bandwidth . . . 20 MHz Typical**
- **Maximum Data Rate at Read Data Pulse (RDP) . . . 1.4 Mb/s Typical**
- **Available in 300-mil Dual-In-Line and "Small Outline" Plastic Packages**

DW OR NT . . . PACKAGE
(TOP VIEW)



description

The TL041 is a magnetic tape read signal conditioner designed for use with the TL040 video amplifier. When combined, these devices amplify the low-signal output from a streaming-tape playback head and reconstruct the data as originally written on the tape. The TL041C includes a gain-controlled amplifier, two comparators, read/write select logic, a time-domain filter, and a bidirectional one-shot multivibrator.

The amplifier has differential inputs, differential outputs, and electronic gain control. A special feature of the electronic gain control is the Electronic Gain Select (EGS). When the EGS input is high, the Electronic Gain Voltage (EGV) input is driven low and amplifier gain is determined by the value of the resistor connected between the Gain Adjust (GADJ) pins. When the EGS input is low, the gain set by the resistor is increased by an amount determined by the voltage applied to the EGV pin.

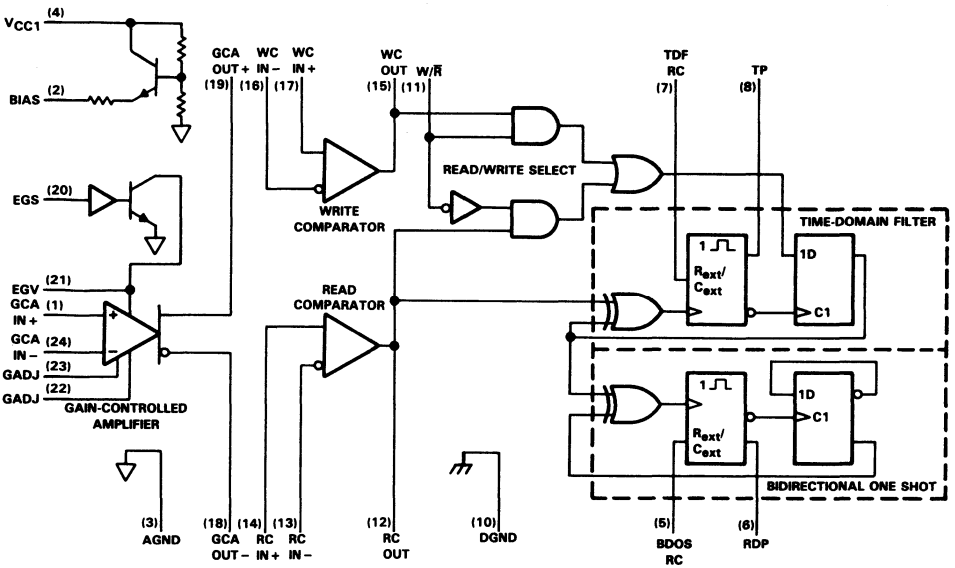
To accommodate different magnetic tape output signal levels, the amplifier gain may be switched by logic at the EGS input, controlled manually with an adjustable voltage at the EGV input, or automatically adjusted with an automatic gain control (AGC) circuit applying a control voltage to the EGV input.

The comparator functions are controlled by a logic input to the Write/Read (W/$\overline{R}$) select input. With the W/$\overline{R}$ input low, the read comparator output (usually connected as a zero-crossing detector) is sent to the time-domain filter. When W/$\overline{R}$ is high, the write comparator output is used to provide write amplitude verification in a typical read-after-write function.

The time-domain filter helps to ensure the input data is valid. A capacitor in series with a resistor, connected to the time-domain filter pin (TDF RC), begins charging at the leading edge of an input pulse from the read comparator. If the input pulse does not remain high for one RC time constant, the pulse is considered invalid and no signal is passed to the bidirectional one-shot multivibrator (BDOS). However, if the input pulse remains high for longer than one RC time constant, the pulse is considered valid and the signal is passed through the time-domain filter to trigger the BDOS. When triggered, the BDOS provides a pulse to the Read Data Pulse (RDP) output. The RDP output pulse duration is determined by a resistor-capacitor network connected to the BDOS RC pin.

The TL041C is characterized for operation from 0°C to 70°C.

functional block diagram



FUNCTION TABLE

INPUT CONDITONS			I/O NAME	I/O CONDITION
EGS	W/$\overline{R}$	DIFFERENTIAL INPUTS WRITE OR READ COMPARATOR		
	X	RC IN+ > RC IN−	RC OUT	H
	X	RC IN− > RC IN+	RC OUT	L
	L	X	RC OUT	Input to time-domain filter
	X	WC IN+ > WC IN−	WC OUT	H
	X	WC IN− > WC IN+	WC OUT	L
	H	X	WC OUT	Input to time-domain filter
H		X	EGV	L
L		X	EGV	Input

PIN NAME	PIN NO.	DESCRIPTION
AGND	3	Analog ground
BDOS RC	5	Bidirectional one-shot resistor and capacitor
BIAS	2	Output bias voltage
DGND	10	Digital ground
EGS	20	Electronic gain select
EGV	21	Electronic gain voltage
GCA IN−	24	Gain-controlled amplifier, inverting input
GCA IN+	1	Gain-controlled amplifier, noninverting input
GADJ	22	Gain adjust
GADJ	23	Gain adjust
GCA OUT−	18	Gain-controlled amplifier, inverting output
GCA OUT+	19	Gain-controlled amplifier, noninverting output
RC IN−	13	Read comparator, inverting input
RC IN+	14	Read comparator, noninverting input
RC OUT	12	Read comparator out
RDP	6	Read data pulse
TDF RC	7	Time-domain filter resistor and capacitor
TP	8	Test point
V_{CC1}	4	Analog collector supply voltage
V_{CC2}	9	Digital collector supply voltage
WC IN−	16	Write comparator, inverting input
WC IN+	17	Write comparator, noninverting input
WC OUT	15	Write comparator out
W/$\overline{R}$	11	Write/read

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage: V_{CC1} (see Note 1) . . . . . 14 V
V_{CC2} . . . . . 7 V
Input voltage range: Amplifier and comparators . . . . . AGND − 0.2 V to V_{CC1} + 0.2 V
Multivibrators and logic . . . . . AGND − 0.2 V to V_{CC2} + 0.2 V
Input current: EGV (see Note 2) . . . . . ±2 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds . . . . . 260°C

NOTES: 1. All voltages except differential voltages are with respect to network ground terminals (AGND and DGND tied together).
2. Driving EGV high from a low-impedance source (> ±2 mA capability) with EGS high can result in damage to the device.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1350 mW	10.8 mW/°C	864 mW/°C
NT	1700 mW	13.6 mW/°C	1088 mW/°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	13.2	V
Supply voltage, V_{CC2}		4.5	5	5.5	V
High-level input voltage, V_{IH}	EGS or W/$\overline{R}$	2			V
Low-level input voltage, V_{IL}	EGS or W/$\overline{R}$			0.8	V
Input voltage, V_I	EGS	0		10	V
	EGV	0		$0.8V_{CC1}$	
Common-mode input voltage to gain-control amplifier, V_{IC}			4		V
High-level output current, I_{OH}	WC OUT, RC OUT, TP, or RDP			−400	μA
Low-level output current, I_{OL}	WC OUT, RC OUT, TP, or RDP			8	mA
Pulse duration, t_w	TP or RDP	40			ns
External timing resistance, (see Note 3)	TDF or BDOS RC	5		25	kΩ
External timing capacitance	TDF or BDOS RC)	0.01	0.1	1000	nF
Operating free-air temperature, T_A		0		70	°C

NOTE 3: Some high resistance and capacitance combinations may produce abnormal output waveforms.

electrical characteristics at V_{CC1} = 12 V, V_{CC2} = 5 V, $V_{IC(GIC)}$ = V_{bias}, R_{ADJ} = 5 kΩ, EGS at high level, EGV at 0 V, r_i = 50 Ω, R_L = 2 kΩ, T_A = 25°C (unless otherwise noted)

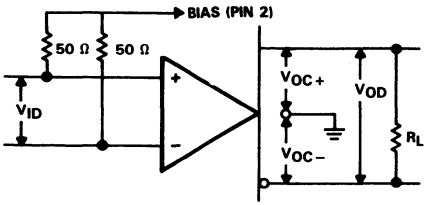
gain-controlled amplifier

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage	1	V_{ID} = 0,	V_{OD} = V_O		0.35	0.75	V
V_{OPP}	Maximum differential output voltage	1	V_{ID} = 1 V,	V_{OPP} = V_O	3	4		V
A_{VD}	Large-signal differential voltage amplification	1	V_{ID} = 20 mV,	EGS high	8	14	20	V/V
			V_{id} = 20 mV, EGS low, f = 455 kHz	EGV at 4 V		19		V/V
				EGV at 9.6 V		90		
CMRR	Common-mode rejection ratio	2	V_{IC} = 2 V to 5 V		60	80		dB
V_{IC}	Common-mode input voltage	2			2		5	V
V_{OC}	Common-mode output voltage	1	V_{ID} = 0		4	5	6	V
I_{IO}	Input offset current	1	I_{IB+} − I_{IB-}			0.2	3	μA
I_O	Output current, sink				1.5	2		mA
I_{IB}	Input bias current	1	(I_{IB+} + I_{IB-})/2			5	17	μA
$V_{O(BIAS)}$	Bias output voltage	1			3	4	5	V
$z_{o(BIAS)}$	Bias output impedance					1		kΩ
z_i	Input impedance					30		kΩ
BW	Bandwidth (−3 dB)	3				20		MHz
k_{SVR}	Supply voltage rejection ratio	4	V_{CC1} = 10.8 V to 13.2 V		50	70		dB
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 13.2 V,	No signal		32	45	mA

logic section

PARAMETER			TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage			V_{CC2} = 4.5 V, I_{OH} = −400 μA	V_{ID} = 0.1 V,	2.7	3.5		V
V_{OL}	Low-level output voltage			V_{CC2} = 4.5 V, I_{OL} = 8 mA	V_{ID} = 0.1 V,		260	500	mV
V_{ICR}	Common-mode input voltage, comparators					2		7	V
I_{IH}	High-level input current	EGS		$V_{I(EGS)}$ = 2.7 V			120	200	μA
		W/$\overline{R}$		$V_{I(W/\overline{R})}$ = 2.7 V				20	
I_{IL}	Low-level input current	EGS		$V_{I(EGS)}$ = 0.4 V				−20	μA
		W/$\overline{R}$		$V_{I(W/\overline{R})}$ = 0.4 V				−400	
I_{CC2}	Supply current from V_{CC2}			V_{CC2} = 5.5 V,	No signal		22	31	mA
	Response time			100-mV step,	5-mV overdrive		50		ns
t_w	Pulse duration of one-shots (TP, RDP)			R_{ext} = 5 kΩ,	C_{ext} = 100 pF		360		ns
				R_{ext} = 20 kΩ,	C_{ext} = 33 pF		460		

PARAMETER MEASUREMENT INFORMATION



$V_{OO} = V_{OD}$ with $V_{ID} = 0$

$V_{OPP} = V_{OD}$ with $V_{ID} = 1$ V

$A_{VD} = \frac{V_{OD}}{V_{ID}}$ with $V_{ID} = 20$ mV

$V_{OC} = \frac{V_{OC+} + V_{OC-}}{2}$ with $V_{ID} = 0$

FIGURE 1

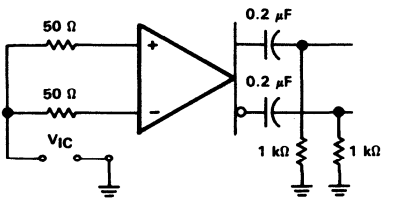


FIGURE 2

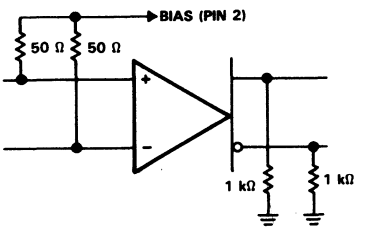


FIGURE 3

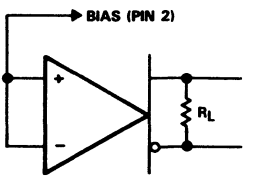


FIGURE 4

TYPICAL CHARACTERISTICS

READ DATA PULSE DURATION
vs
CAPACITANCE

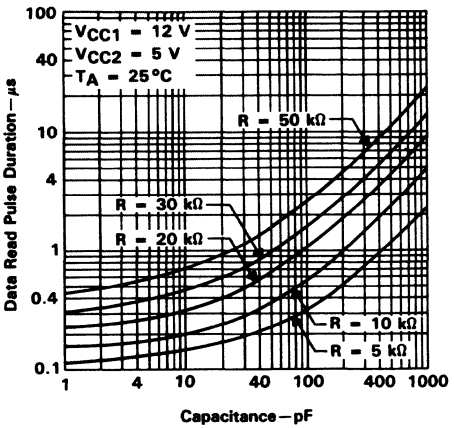


FIGURE 5

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
ELECTRONIC GAIN VOLTAGE

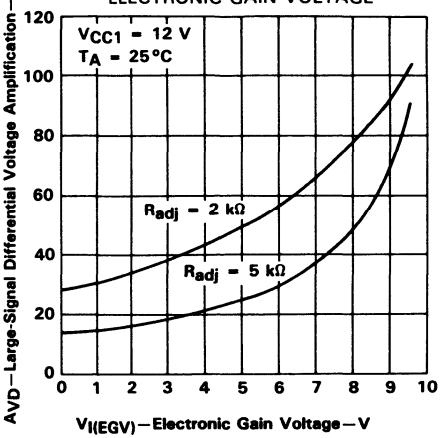


FIGURE 6

TYPICAL APPLICATION DATA

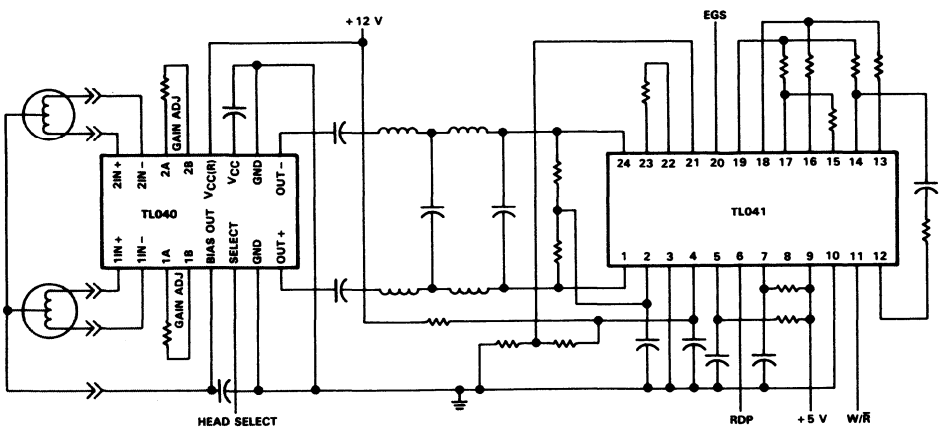


FIGURE 7. READ SIGNAL CIRCUIT FOR A STREAMING TAPE DRIVE

TL592B
DIFFERENTIAL VIDEO AMPLIFIER

D2668, AUGUST 1985

- **Adjustable Gain to 400 Typ**
- **No Frequency Compensation Required**
- **Low Noise . . . 3 μV Typ V_n**

description

This device is a monolithic two-stage video amplifier with differential inputs and differential outputs. It features internal series-shunt feedback that provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

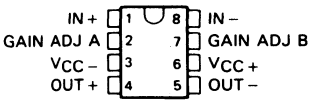
The differential gain is typically 400 when the gain adjust pins are connected together, or amplification may be adjusted from near 0 to 400 by the use of a single external resistor connected between the gain adjustment pins A and B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disk-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general-purpose video and pulse amplifiers.

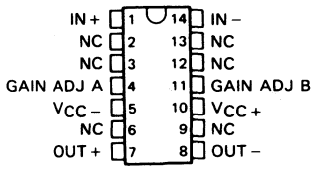
The device achieves low equivalent noise voltage through special processing and a new circuit layout incorporating input transistors with low base resistance.

The TL592B is characterized for operation from 0°C to 70°C.

D8† OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



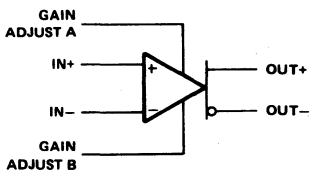
D14† OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



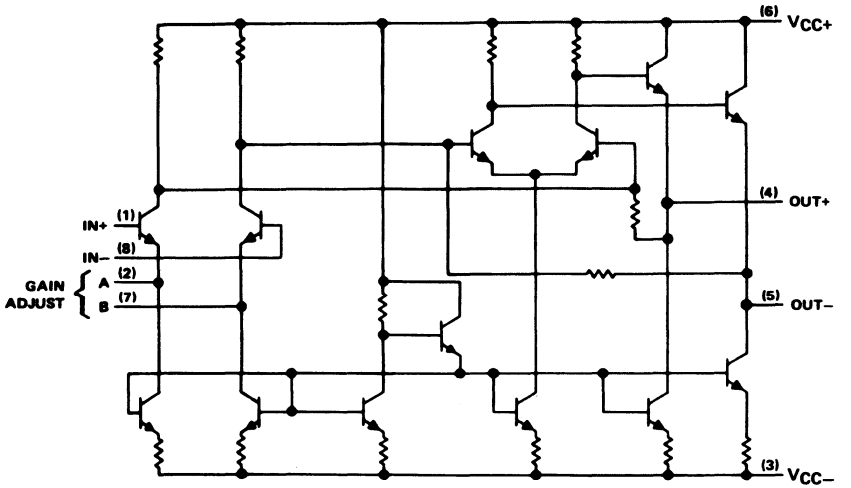
NC – No internal connection

†D8 and D14 are the codes used to differentiate the 8-pin and 14-pin versions, respectively, of the D package, if the device is available in both versions.

symbol



schematic



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage, V_{CC-} . . . . . −8 V
Differential input voltage . . . . . ±5 V
Voltage range, any input . . . . . V_{CC+} to V_{CC-}
Output current . . . . . 10 mA
Continuous total power dissipation (see Note 2) . . . . . 530 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values except differential input voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. For operation in the D8 or P package above 59°C free-air temperature, derate linearly to 464 mW at 70°C at the rate of 5.8 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	3	6	8	V
Supply voltage, V_{CC-}	−3	−6	−8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified free-air temperature, V_{CC+} = 6 V, V_{CC-} = −6 V, R_L = 2 kΩ (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_L = 2 kΩ, R_{AB} = 0		25°C	300	400	500	V/V
					0°C to 70°C	250		600	
A_{VD2}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_L = 2 kΩ, R_{AB} = 1 kΩ		25°C		13		V/V
BW	Bandwidth (└ 3 dB)	2	V_{OPP} = 1 V, R_{AB} = 0		25°C		50		MHz
I_{IO}	Input offset current				25°C		0.4	F	μA
					0°C to 70°C			(	
I_{IB}	Input bias current				25°C		9	3(	μA
					0°C to 70°C			4(	
V_{ICR}	Common-mode input voltage range	3			25°C	±1			V
					0°C to 70°C	±1			
V_{OC}	Common-mode output voltage	1	R_L = ∞		25°C	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞		25°C		0.35	0.75	V
					0°C to 70°C			1.5	
V_{OPP}	Peak-to-peak output voltage swing	1	R_L = 2 kΩ, R_{AB} = 0		25°C	3	4		V
					0°C to 70°C	2.8			
r_i	Input resistance		V_{OD} = 1 V, R_{AB} = 0		25°C		4		kΩ
					0°C to 70°C		3.6		
r_o	Output resistance				0°C to 70°C			30	Ω
C_i	Input capacitance				25°C		5		pF
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, R_{AB} = 0	f = 100 kHz	25°C	60	86		dB
				f = 5 MHz			60		
				f = 100 kHz	0°C to 70°C	50			
				f = 5 MHz			60		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V, R_{AB} = 0		25°C	50	70		dB
					0°C to 70°C	50			
V_n	Broadband equivalent input noise voltage	4	BW = 1 kHz to 10 MHz		25°C		3		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V		25°C		7.5		ns
t_r	Rise time	2	ΔV_O = 1 V		25°C		10.5		ns
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V, V_O = 3 V			3	4		mA
I_{CC}	Supply current		No load, No signal		25°C		18	24	mA
					0°C to 70°C			27	

†R_{AB} is the gain-adjustment resistor connected between gain-adjust pins A and B. If not specified for a particular parameter, its value is irrelevant.

PARAMETER MEASUREMENT INFORMATION

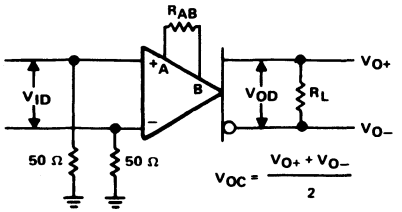


FIGURE 1

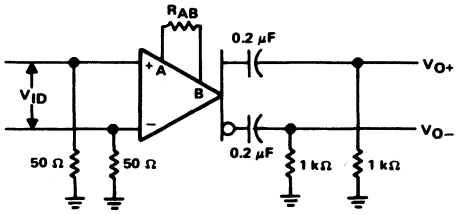


FIGURE 2

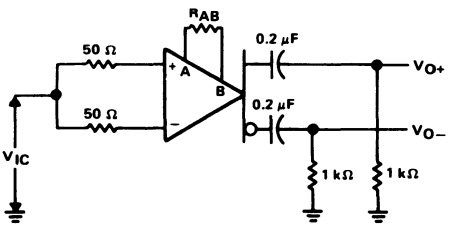


FIGURE 3

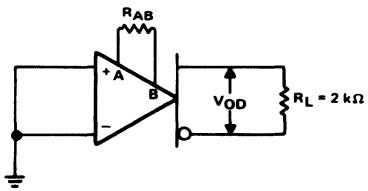


FIGURE 4

TYPICAL CHARACTERISTICS

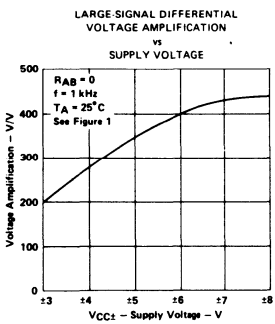


FIGURE 5

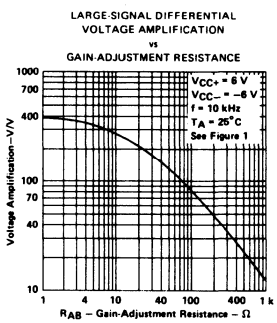


FIGURE 6

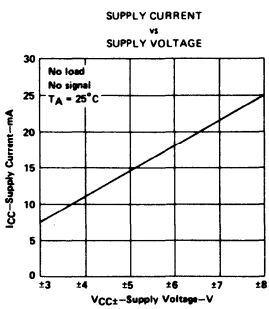
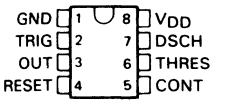


FIGURE 7

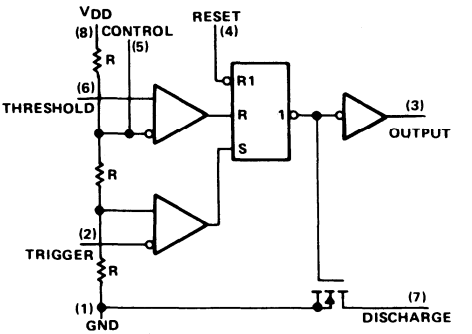
D2791, FEBRUARY 1984—REVISED OCTOBER 1985

- **Very Low Power Consumption . . . 1 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **High-Impedance Inputs . . . 10^{12} Ω Typ**
- **Single-Supply Operation from 1 V to 18 V**
- **Functionally Interchangeable with the NE555; Has Same Pinout**

D OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



functional block diagram



Reset can override Trigger, which can override Threshold.

description

The TLC551 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE555 because of the high input impedance. Power consumption is low across the full range of power supply voltages.

Like the NE555, the TLC551 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the complementary CMOS output is capable of sinking over 100 milliamperes and sourcing over 10 milliamperes, the TLC551 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883C, Method 3015.2. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC551C is characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments.

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range (any input) . . . . . −0.3 V to V_{DD}
Sink current, discharge or output . . . . . 150 mA
Source current, output . . . . . 15 mA
Continuous total dissipation at (or below) 25°C free-air temperature . . . . . 460 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1	18	V
Operating free-air temperature, T_A	0	70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0.475	0.67	0.85	V
		Full range	0.45		0.875	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.15	0.33	0.425	V
		Full range	0.1		0.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	0.7	1	V
		Full range	0.3		1	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 μA	25°C		0.02	0.15	V
		Full range			0.2	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 μA	25°C		0.03	0.2	V
		Full range			0.25	
High-level output voltage	I_{OH} = −10 μA	25°C	0.6	0.98		V
		Full range	0.6			
Supply current		25°C		15	100	μA
		Full range			150	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0.95	1.33	1.65	V
		Full range	0.85		1.75	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.4	0.67	0.95	V
		Full range	0.3		1.05	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.03	0.2	V
		Full range			0.25	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		V
		Full range	1.5			
Supply current		25°C		65	250	μA
		Full range			400	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	2.8	3.3	3.8	V
		Full range	2.7		3.9	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	1.36	1.66	1.96	V
		Full range	1.26		2.06	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.14	0.5	V
		Full range			0.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4	V
		Full range			0.5	
	I_{OL} = 5 mA	25°C		0.13	0.3	
		Full range			0.4	
	I_{OL} = 3.2 mA	25°C		0.08	0.3	
		Full range			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		V
		Full range	4.1			
Supply current		25°C		170	350	μA
		Full range			500	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	9.45	10	10.55	V
		Full range	9.35		10.65	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	4.65	5	5.35	V
		Full range	4.55		5.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.77	1.7	V
		Full range			1.8	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2	V
		Full range			3.6	
	I_{OL} = 50 mA	25°C		0.63	1	
		Full range			1.3	
	I_{OL} = 10 mA	25°C		0.12	0.3	
		Full range			0.4	
High-level output voltage	I_{OH} = −10 mA	25°C	12.5	14.2		V
		Full range	12.5			
	I_{OH} = −5 mA	25°C	13.5	14.6		
		Full range	13.5			
	I_{OH} = −1 mA	25°C	14.2	14.9		
		Full range	14.2			
Supply current		25°C		360	600	μA
		Full range			800	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	11.4	12	12.6	V
		Full range	10.9		12.7	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	5.6	6	6.4	V
		Full range	5.5		6.5	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.72	1.5	V
		Full range			1.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 3.2 mA	25°C		0.04	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	17.3	17.9		V
		Full range	17.3			
Supply current		25°C		420	600	μA
		Full range			800	

†Full range (MIN to MAX) is 0°C to 70°C.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval	V_{DD} = 5 V to 15 V,		1%	3%	
Supply voltage sensitivity of timing interval	$R_A = R_B$ = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Note 2		0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
Output pulse fall time			15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF, See Note 2	1.2	1.8		MHz

NOTE 2: R_A, R_B, and C_T are as defined in Figure 1.

TYPICAL APPLICATION DATA

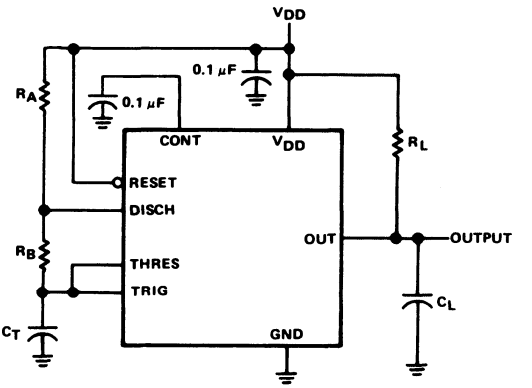
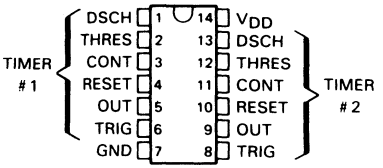


FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

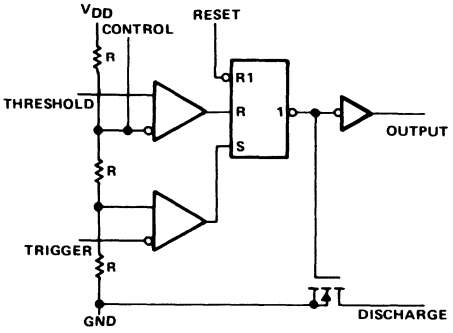
D2796, FEBRUARY 1984 – REVISED OCTOBER 1985

- **Very Low Power Consumption . . . 2 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **High-Impedance Inputs . . . 10^{12} Ω Typ**
- **Single-Supply Operation from 1 V to 18 V**
- **Functionally Interchangeable with the NE556; Has Same Pinout**

D OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



functional block diagram (each timer)



Reset can override Trigger and Threshold.
Trigger can override Threshold.

description

The TLC552 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE555 because of the high input impedance. Power consumption is low across the full range of power supply voltages.

Like the NE556, the TLC552 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the complementary CMOS output is capable of sinking over 100 milliamperes and sourcing over 10 milliamperes, the TLC552 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE556.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883C, Method 3015.2. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC552C is characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments.

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range (any input) . . . . . −0.3 V to V_{DD}
Sink current, discharge or output . . . . . 150 mA
Source current, output . . . . . 15 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)
D package . . . . . 950 mW
N package . . . . . 875 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation of the above 25°C free-air temperature, see Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	950 mW	7.6 mW/°C	25°C
N	875 mW	7.0 mW/°C	25°C

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1	18	V
Operating free-air temperature, T_A	0	70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0.475	0.67	0.85	V
		Full range	0.45		0.875	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.15	0.33	0.425	V
		Full range	0.1		1.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	0.7	1	V
		Full range	0.3		1	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 μA	25°C		0.02	0.15	V
		Full range			0.2	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 μA	25°C		0.03	0.2	V
		Full range			0.25	
High-level output voltage	I_{OH} = −10 μA	25°C	0.6	0.98		V
		Full range	0.6			
Supply current		25°C		30	200	μA
		Full range			300	

† Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0.95	1.33	1.65	V
		Full range	0.85		1.75	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.4	0.67	0.95	V
		Full range	0.3		1.05	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.03	0.2	V
		Full range			0.25	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		V
		Full range	1.5			
Supply current		25°C		130	500	μA
		Full range			800	

† Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	2.8	3.3	3.8	V
		Full range	2.7		3.9	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	1.36	1.66	1.96	V
		Full range	1.26		2.06	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.14	0.5	V
		Full range			0.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4	V
		Full range			0.5	
	I_{OL} = 5 mA	25°C		0.13	0.3	
		Full range			0.4	
	I_{OL} = 3.2 mA	25°C		0.08	0.3	
		Full range			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		V
		Full range	4.1			
Supply current		25°C		340	700	μA
		Full range			1000	

† Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	9.45	10	10.55	V
		Full range	9.35		10.65	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	4.65	5	5.35	V
		Full range	4.55		5.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.77	1.7	V
		Full range			1.8	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2	V
		Full range			3.6	
	I_{OL} = 50 mA	25°C		0.63	1	
		Full range			1.3	
	I_{OL} = 10 mA	25°C		0.12	0.3	
		Full range			0.4	
High-level output voltage	I_{OH} = −10 mA	25°C	12.5	14.2		V
		Full range	12.5			
	I_{OH} = −5 mA	25°C	13.5	14.6		
		Full range	13.5			
	I_{OH} = −1 mA	25°C	14.2	14.9		
		Full range	14.2			
Supply current		25°C		0.72	1.2	mA
		Full range			1.6	

† Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	11.4	12	12.6	V
		Full range	10.9		12.7	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	5.6	6	6.4	V
		Full range	5.5		6.5	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.72	1.5	V
		Full range			1.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 3.2 mA	25°C		0.04	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	17.3	17.9		V
		Full range	17.3			
Supply current		25°C		0.84	1.2	mA
		Full range			1.6	

† Full range (MIN to MAX) is 0°C to 70°C.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval	V_{DD} = 5 V to 15 V,		1%	3%	
Supply voltage sensitivity of timing interval	$R_A = R_B$ = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Note 3		0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
Output pulse fall time			15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF, See Note 3	1.2	2.8		MHz

NOTE 3: R_A, R_B, and C_T are as defined in Figure 1.

TYPICAL APPLICATION DATA

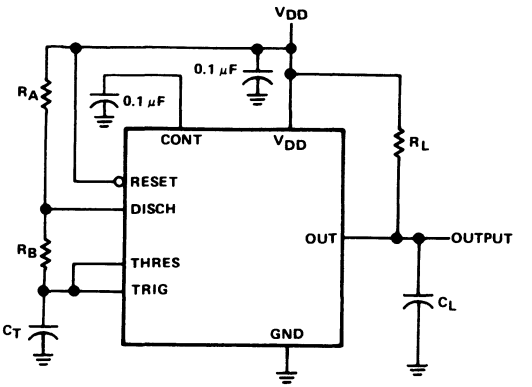
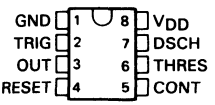


FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

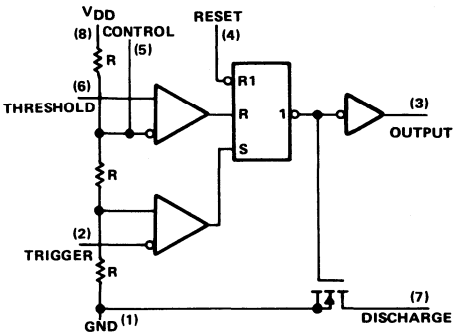
D2784, SEPTEMBER 1983 – REVISED MAY 1988

- **Very Low Power Consumption . . . 1 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **High-Impedance Inputs . . . 10^{12} Ω Typ**
- **Single-Supply Operation from 2 V to 18 V** *(unless specified)*
- **Functionally Interchangeable with the NE555; Has Same Pinout**

TLC555M . . . JG PACKAGE
TLC555I, TLC555C . . . D or P PACKAGE
(TOP VIEW)



functional block diagram



Reset can override Trigger, which can override Threshold.

description

The TLC555 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE555 because of the high input impedance. Power consumption is low across the full range of power supply voltage.

Like the NE555, the TLC555 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the complementary CMOS output is capable of sinking over 100 milliamperes and sourcing over 10 milliamperes, the TLC555 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.
The TLC555M is characterized for operation over the full military temperature range of –55°C to 125°C. The TLC555C is characterized for operation from 0°C to 70°C. The TLC555I is characterized for operation from –40°C to 85°C.

LinCMOS is a trademark of Texas Instruments.

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range (any input) . . . . . −0.3 V to V_{DD}
Sink current, discharge or output . . . . . 150 mA
Source current, output . . . . . 15 mA
Continuous total dissipation (see Note 2) . . . . . 460 mW
Operating free-air temperature range: TLC555M . . . . . −55°C to 125°C
TLC555C . . . . . 0°C to 70°C
TLC555I . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation of the TLC555M above 95°C free-air temperature, derate linearly at the rate of 8.4 mW/°C to 210 mW at 125°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Operating free-air temperature, T_A	TLC555M	−55		125	°C
	TLC555I	−40		85	
	TLC555C	0		70	
Supply voltage, V_{DD}	TLC555M	5		18	
	TLC555I	3		18	
	TLC555C	2		18	

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER	TEST CONDITIONS†		TLC555C			UNIT
			MIN	TYP	MAX	
Threshold voltage level		25°C	0.95	1.33	1.65	V
		Full range	0.85		1.75	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.4	0.67	0.95	V
		Full range	0.3		1.05	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		2	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.03	0.2	V
		Full range			0.25	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		V
		Full range	1.5			
Supply current		25°C			250	μA

† Full range (MIN to MAX) is 0° to 70°C for TLC555C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		TLC555M			TLC555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	2.8	3.3	3.8	2.8	3.3	3.8	V
		Full range	2.7		3.9	2.7		3.9	
Threshold current		25°C		10			10		pA
		MAX		5000			75		
Trigger voltage level		25°C	1.36	1.66	1.96	1.36	1.66	1.96	V
		Full range	1.26		2.06	1.26		2.06	
Trigger current		25°C		10			10		pA
		MAX		5000			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		2	0.3		2	
Reset current		25°C		10			10		pA
		MAX		5000			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.14	0.5		0.14	0.5	V
		Full range			0.6			0.6	
Discharge switch off-state current		25°C		0.1			0.1		nA
		MAX		120			0.5		
Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4		0.21	0.4	V
		Full range			0.6			0.5	
	I_{OL} = 5 mA	25°C		0.13	0.3		0.13	0.3	
		Full range			0.45			0.4	
	I_{OL} = 3.2 mA	25°C		0.08	0.3		0.08	0.3	
		Full range			0.4			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		4.1	4.8		V
		Full range	4.1			4.1			
Supply current		25°C		170	350		170	350	μA

† Full range (MIN to MAX) is −55°C to 125°C for TLC555M, 0°C to 70°C for TLC555C, and −40°C to 85°C for TLC555I

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		TLC555M			TLC555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	9.45	10	10.55	9.45	10	10.55	V
		Full range	9.35		10.65	9.35		10.65	
Threshold current		25°C		10			10		pA
		MAX		5000			75		
Trigger voltage level		25°C	4.65	5	5.35	4.65	5	5.35	V
		Full range	4.55		5.45	4.55		5.45	
Trigger current		25°C		10			10		pA
		MAX		5000			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		2	0.3		2	
Reset current		25°C		10			10		pA
		MAX		5000			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.77	1.7		0.77	1.7	V
		Full range			1.8			1.8	
Discharge switch off-state current		25°C		0.1			0.1		nA
		MAX		120			0.5		
Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2		1.28	3.2	V
		Full range			3.8			3.6	
	I_{OL} = 50 mA	25°C		0.63	1		0.63	1	
		Full range			1.5			1.3	
	I_{OL} = 10 mA	25°C		0.12	0.3		0.12	0.3	
		Full range			0.45			0.4	
High-level output voltage	I_{OH} = −10 mA	25°C	12.5	14.2		12.5	14.2		V
		Full range	12.5			12.5			
	I_{OH} = −5 mA	25°C	13.5	14.6		13.5	14.6		
		Full range	13.5			13.5			
	I_{OH} = −1 mA	25°C	14.2	14.9		14.2	14.9		
		Full range	14.2			14.2			
Supply current		25°C		360	600		360	600	μA

†Full range (MIN to MAX) is −55°C to 125°C for TLC555M, 0°C to 70°C for TLC555C, and −40°C to +85°C for TLC555I

electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		TLC555M			TLC555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	11.4	12	12.6	11.4	12	12.6	V
		Full range	10.9		12.7	10.9		12.7	
Threshold current		25°C		10			10		pA
		MAX		5000			75		
Trigger voltage level		25°C	5.6	6	6.4	5.6	6	6.4	V
		Full range	5.5		6.5	5.5		6.5	
Trigger current		25°C		10			10		pA
		MAX		5000			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		2	0.3		2	
Reset current		25°C		10			10		pA
		MAX		5000			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.72	1.5		0.72	1.5	V
		Full range			1.6			1.6	
Discharge switch off-state current		25°C		0.1			0.1		nA
		MAX		120			0.5		
Low-level output voltage	I_{OL} = 3.2 mA	25°C		0.04	0.3		0.04	0.3	V
		Full range			0.4			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	17.3	17.9		17.3	17.9		V
		Full range	17.3			17.3			
Supply current		25°C			600			600	μA

†Full range (MIN to MAX) is −55°C to 125°C for TLC555M, 0°C to 70°C for TLC555C, and −40°C to +85°C for TLC555I

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval	V_{DD} = 5 V to 15 V,		1%	3%	
Supply voltage sensitivity of timing interval	$R_A = R_B$ = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Note 3		0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
Output pulse fall time			15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF, See Note 3	1.2	2.1		MHz

NOTE 3: R_A, R_B, and C_T are as defined in Figure 1.

TYPICAL APPLICATION DATA

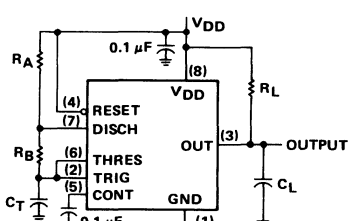


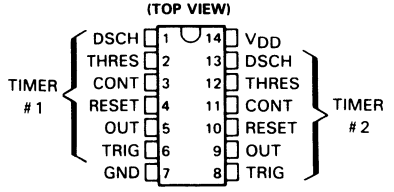
FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

TLC556M, TLC556I, TLC556C
DUAL LinCMOS™ TIMERS

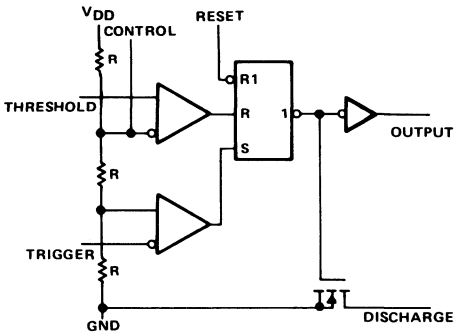
D2796, FEBRUARY 1984 – REVISED MAY 1988

- **Very Low Power Consumption . . . 2 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  Sink 100 mA Typ
  Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **High-Impedance Inputs . . . 10^{12} Ω Typ**
- **Single-Supply Operation from 2 V to 18 V (unless specified)**
- **Functionally Interchangeable with the NE556; Has Same Pinout**

TLC556M . . . J DUAL-IN-LINE PACKAGE
TLC556I, TLC556C . . . D OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



functional block diagram (each timer)



Reset can override Trigger and Threshold.
Trigger can override Threshold.

description

The TLC556 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE556 because of the high input impedance. Power consumption is low across the full range of power supply voltages.

Like the NE556, the TLC556 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the CMOS output is capable of sinking over 100 milliamperes and sourcing over 10 milliamperes, the TLC556 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE556.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883C, Method 3015.2. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC556M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC556I is characterized for operation from −40°C to 85°C. The TLC556C is characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments.

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

† For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TLC556M	TLC556I	TLC556C	UNIT
Supply voltage (see Note 1)		18	18	18	V
Input voltage		−0.3 to V_{DD}	−0.3 to V_{DD}	−0.3 to V_{DD}	V
Sink current, discharge or output		150	150	150	mA
Source current, output		15	15	15	mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2)	D package		950	950	mW
	J package	1375			
	N package		875	875	
Operating free-air temperature		−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300			

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C, see the Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	950 mW	7.6 mW/°C	25°C
J (alloy mount)	1375 mW	11.0 mW/°C	25°C
N	875 mW	7.0 mW/°C	25°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Operating free-air temperature, T_A	TLC556M	−55		125	°C
	TLC556I	−40		85	
	TLC556C	0		70	
Supply voltage, V_{DD}	TLC556M	5		18	
	TLC556I	3		18	
	TLC556C	2		18	

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER	TEST CONDITIONS†		TLC556C			UNIT
			MIN	TYP	MAX	
Threshold voltage level		25°C	0.95	1.33	1.65	V
		Full range	0.85		1.75	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.4	0.67	0.95	V
		Full range	0.3		1.05	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.04	0.2	V
		Full range			0.25	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		V
		Full range	1.5			
Supply current	See Note 3	25°C		130	500	μA
		Full range			800	

†Full range (MIN to MAX) is 0°C to 70°C for TLC556C.

NOTE 3: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	2.8	3.3	3.8	2.8	3.3	3.8	2.8	3.3	3.8	V
		Full range	2.7		3.9	2.7		3.9	2.7		3.9	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	1.36	1.66	1.96	1.36	1.66	1.96	1.36	1.66	1.96	V
		Full range	1.26		2.06	1.26		2.06	1.26		2.06	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.15	0.5		0.15	0.5		0.15	0.5	V
		Full range			0.6			0.6			0.6	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4		0.21	0.4		0.21	0.4	
		Full range			0.6			0.5			0.5	
	I_{OL} = 5 mA	25°C		0.13	0.3		0.13	0.3		0.13	0.3	V
		Full range			0.45			0.4			0.4	
	I_{OL} = 3.2 mA	25°C		0.08	0.3		0.08	0.3		0.08	0.3	
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		4.1	4.8		4.1	4.8		V
		Full range	4.1			4.1			4.1			
Supply current	See Note 3	25°C		340	700		340	700		340	700	μA
		Full range			1400			1200			1000	

† Full range (MIN to MAX) is −55°C to 125°C for TLC556M, −40°C to 85°C for TLC556I, and 0°C to 70°C for TLC556C.

NOTE 3: These values apply for the expected operating configuration in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	9.45	10	10.55	9.45	10	10.55	9.45	10	10.55	V
		Full range	9.35		10.65	9.35		10.65	9.35		10.65	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	4.65	5	5.35	4.65	5	5.35	4.65	5	5.35	V
		Full range	4.55		5.45	4.55		5.45	4.55		5.45	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.8	1.7		0.8	1.7		0.8	1.7	V
		Full range			1.8			1.8			1.8	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2		1.28	3.2		1.28	3.2	V
		Full range			3.8			3.7			3.6	
	I_{OL} = 50 mA	25°C		0.63	1		0.63	1		0.63	1	
		Full range			1.5			1.4			1.3	
	I_{OL} = 10 mA	25°C		0.12	0.3		0.12	0.3		0.12	0.3	
		Full range			0.45			0.4			0.4	
High-level output voltage	I_{OH} = −10 mA	25°C	12.5	14.2		12.5	14.2		12.5	14.2		V
		Full range	12.5			12.5			12.5			
	I_{OH} = −5 mA	25°C	13.5	14.6		13.5	14.6		13.5	14.6		
		Full range	13.5			13.5			13.5			
	I_{OH} = −1 mA	25°C	14.2	14.9		14.2	14.9	14.2	14.9			
		Full range	14.2			14.2			14.2			
Supply current	See Note 3	25°C		0.72	1.2		0.72	1.2		0.72	1.2	mA
		Full range			2			1.8			1.6	

† Full range (MIN to MAX) is −55°C to 125°C for TLC556M, −40°C to 85°C for TLC556I, and 0°C to 70°C for TLC556C.

NOTE 3: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	11.4	12	12.6	11.4	12	12.6	11.4	12	12.6	V
		Full range	10.9		12.7	10.9		12.7	10.9		12.7	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	5.6	6	6.4	5.6	6	6.4	5.6	6	6.4	V
		Full range	5.5		6.5	5.5		6.5	5.5		6.5	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.73	1.5		0.73	1.5		0.73	1.5	V
		Full range			1.6			1.6			1.6	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL} = 3.2 mA	25°C		0.04	0.3		0.04	0.3		0.04	0.3	V
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	17.3	17.9		17.3	17.9		17.3	17.9		V
		Full range	17.3			17.3			17.3			
Supply current	See Note 3	25°C			1.2			1.2			1.2	mA
		Full range			2			1.8			1.6	

† Full range (MIN to MAX) is −55°C to 125°C for TLC556M, −40°C to 85°C for TLC556I, and 0°C to 70°C for TLC556C.

NOTE 3: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval	V_{DD} = 5 V to 15 V, R_A = R_B = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Note 4		1%	3%	
Supply voltage sensitivity of timing interval			0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
Output pulse fall time			15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF, See Note 3	1.2	2.1		MHz

NOTE 4: R_A, R_B, and C_T are as defined in Figure 3.

TYPICAL CHARACTERISTICS

DISCHARGE SWITCH ON-STATE RESISTANCE
vs
FREE-AIR TEMPERATURE

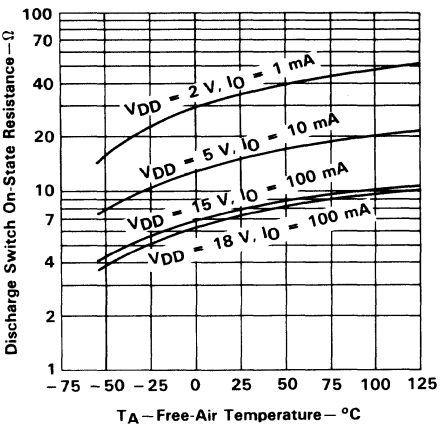
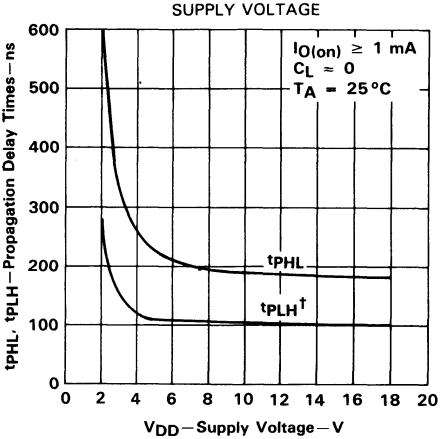


FIGURE 1

PROPAGATION DELAY TIMES TO DISCHARGE OUTPUT
FROM TRIGGER AND THRESHOLD SHORTED TOGETHER
vs
SUPPLY VOLTAGE



†The effects of the load resistance on these values must be taken into account separately.

FIGURE 2

TYPICAL APPLICATION DATA

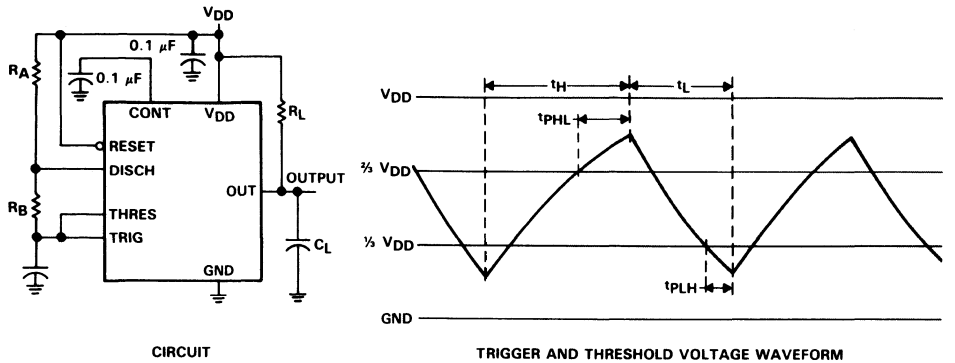


FIGURE 3. ASTABLE OPERATION

Connecting the trigger input to the threshold input as shown in Figure 3 causes the timer to run as a multivibrator. The capacitor C_T charges through R_A and R_B to the trigger voltage level (approximately $0.67V_{DD}$) and then discharges through R_B only to the value of the threshold voltage level (approximately $0.33V_{DD}$). The output is high during the charging cycle (t_H) and low during the discharge cycle (t_L). The duty cycle is controlled by the values of R_A, R_B, and C_T as shown in the equations below.

$$t_H \approx C_T (R_A + R_B) \ln 2 \qquad (\ln 2 = 0.693)$$

$$t_L \approx C_T R_B \ln 2$$

$$\text{Period} = t_H + t_L \approx C_T (R_A + 2R_B) \ln 2$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} \approx 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} \approx \frac{R_B}{R_A + 2R_B}$$

The 0.1-μF capacitor at the control pin in Figure 3 decreases the period by about 10%.

The formulas shown above do not allow for any propagation delay from the trigger and threshold inputs to the discharge output. These delay times add directly to the period and create differences between calculated and actual values that increase with frequency. In addition, the discharge output resistance r_{on} adds to R_B to provide another source of error in the calculation when R_B is very low or r_{on} is very high.

The equations below provide much better agreement with measured values.

$$t_H = C_T (R_A + R_B) \ln \left[3 - \exp\left(\frac{-t_{PLH}}{C_T (R_B + r_{on})} \right) \right] + t_{PHL}$$

$$t_L = C_T (R_B + r_{on}) \ln \left[3 - \exp\left(\frac{-t_{PHL}}{C_T (R_A + R_B)} \right) \right] + t_{PLH}$$

The similarity between the equations above and those given earlier in that a time constant is multiplied by the logarithm of a number or function can be seen. The effect of the propagation times on the timing can also be seen. The limit values of the logarithmic terms must be between ln 2 at low frequencies and ln 3 at extremely high frequencies. For a duty cycle close to 50%, an appropriate constant for the logarithmic terms can be substituted with good results. Duty cycles less than 50% $\left(\frac{t_H}{t_H + t_L}\right)$ will require that $\frac{t_H}{t_L} < 1$ and possibly $R_A \leq r_{on}$. These conditions can be difficult to obtain.

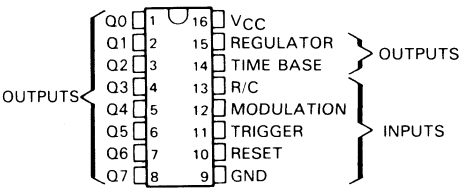
In monostable applications, the trip point of the trigger input can be set by a voltage applied to the control pin. An input voltage between 10% and 80% of the supply voltage from a resistor divider with at least 500 μA bias provides good results.

TYPE uA2240C
PROGRAMMABLE TIMER/COUNTER

D2442, JUNE 1978—REVISED FEBRUARY 1984

- **Accurate Timing from Microseconds to Days**
- **Programmable Delays from 1 Time Constant to 255 Time Constants**
- **Outputs Compatible with TTL and CMOS**
- **Wide Supply-Voltage Range**
- **External Sync and Modulation Capability**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



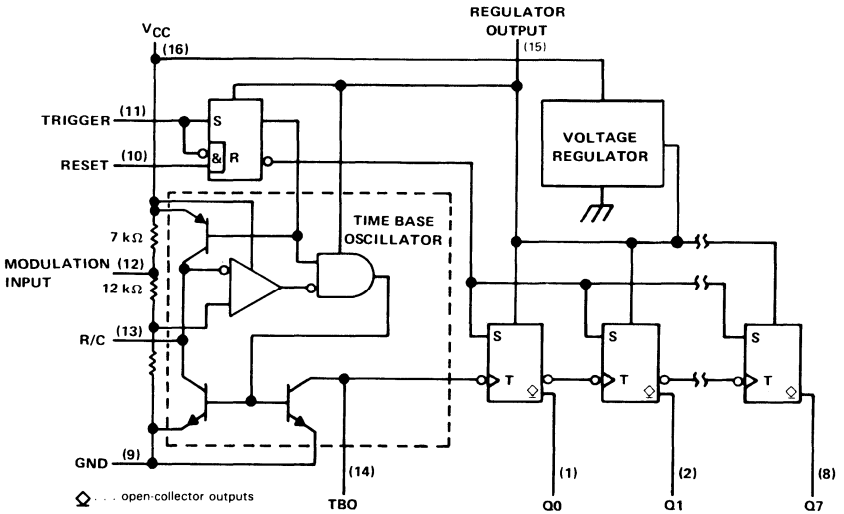
description

These circuits consist of a time-base oscillator, an eight-bit counter, a control flip-flop, and a voltage regulator. The frequency of the time-base oscillator is set by the time constant of an external resistor and capacitor at pin 13 and can be synchronized or modulatd by signals applied to the modulation input. The output of the time-base section is applied directly to the input of the counter section and also appears at pin 14 (time base). The time-base pin may be used to monitor the frequency of the oscillator, to provide an output pulse to other circuitry, or (with the time-base section disabled) to drive the counter input from an external source. The counter input is activated on a negative-going transition. The reset input stops the time-base oscillator and sets each binary output, Q0 through Q7, and the time-base output to a TTL high level. After resetting, the trigger input starts the oscillator and all Q outputs go low. Once triggered, the uA2240C will ignore any signals at the trigger input until it is reset.

The uA2240C timer/counter may be operated in the free-running mode or with output-signal feeedback to the reset input for automatic reset. Two or more binary outputs may be connected together to generate complex pulse patterns, or each output may be used separately to provide eight output frequencies. Using two circuits in cascade can provide precise time delays of up to three years.

The uA2240C is characterized for operation from 0°C to 70°C.

functional block diagram



absolute maximum ratings

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Output voltage: Q0 thru Q7 . . . . . 18 V
Output current: Q0 thru Q7 . . . . . 10 mA
Regulator output current . . . . . −5 mA
Continuous dissipation at (or below) 25°C free-air temperature (see Note 2): . . . . . 650 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to the network ground terminal.
2. For operation above 25°C, see the Dissipation Derating Curves, Section 2.

recommended operating conditions

	uA2240C			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 3)	4		14	V
Timing resistor	0.001		10	MΩ
Timing capacitor	0.01		1000	μF
Counter input frequency (Pin 14)		1.5		MHz
Pull-up resistor, time-base output		20		kΩ
Trigger and reset input pulse voltage	2	3		V
Trigger and reset input pulse duration	2			μs
External clock input pulse voltage	3			V
External clock input pulse duration	1			μs

NOTE 3: For operation with $V_{CC} \leq 4.5$ V, short regulator output to V_{CC}.

electrical characteristics at 25°C free-air temperature

PARAMETER	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Regulator output voltage	1	V_{CC} = 5 V, Trigger and reset open or grounded	3.9	4.4		V
	2	V_{CC} = 15 V, Trigger and reset open or grounded	5.8	6.3	6.8	
Modulation input open circuit voltage	1	V_{CC} = 5 V, Trigger and reset open or grounded	2.8	3.5	4.2	V
		V_{CC} = 15 V, Trigger and reset open or grounded		10.5		
Trigger threshold voltage	1	V_{CC} = 5 V, Reset at 0 V		1.4	2	V
High-level trigger current	1	V_{CC} = 5 V, Trigger at 2 V, Reset at 0 V		10		μA
Reset threshold voltage	1	V_{CC} = 5 V, Trigger at 0 V		1.4	2	V
High-level reset current	1	V_{CC} = 5 V, Trigger at 0 V		10		μA
Couonter input (time base) threshold voltage	2	V_{CC} = 5 V, Trigger and reset open or grounded	1	1.4		V
Low-level output current, Q0 thru Q7	2	V_{CC} = 5 V, Trigger at 2 V, Reset at 0 V, V_{OL} < 0.4 V	2	4		mA
High-level output current, Q0 thru Q7	2	V_{OH} = 15 V, Reset at 2 V, Trigger at 0 V		0.01	15	μA
Supply current	1	V_{CC} = 5 V, Trigger at 0 V, Reset at 5 V		4	7	mA
	1	V_{CC} = 15 V, Trigger at 0 V, Reset at 5 V		13	18	
	3	V+ = 4 V		1.5		

operating characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CIRCUIT	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Initial error of time base‡	1	V_{CC} = 5 V, Trigger at 5 V, Reset at 0 V			±0.5	±5	%
Temperature coefficient of time-base period	1	T_A = 0°C to 70°C	V_{CC} = 5 V		−200		ppm/°C
			V_{CC} = 15 V		−80		
Supply voltage sensitivity of time-base period	1	V_{CC} ≥ 8 V			−0.08	−0.3	%/V
Time-base output frequency	1	V_{CC} = 5 V, R = MIN, C = MIN			130		kHz
Propagation delay time		see Note 4	From trigger input		1		μs
			From reset input		0.8		
Output rise time	2	R_L = 3 kΩ, C_L = 10 pF	Q0 thru Q7		180		ns
Output fall time					180		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡This is the time-base period error due only to the uA2240C and expressed as a percentage of nominal (1.00 RC).
NOTE 4: Propagation delay time is measured from the 50% point on the leading edge of an input pulse to the 50% point on the leading edge of the resulting change of state at Q0.

PARAMETER MEASUREMENT INFORMATION

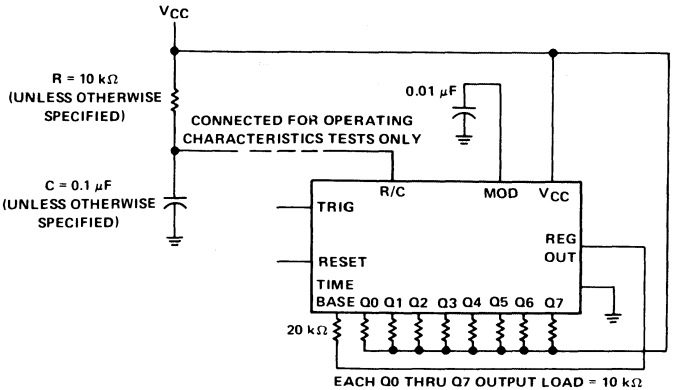


FIGURE 1–GENERAL TEST CIRCUIT

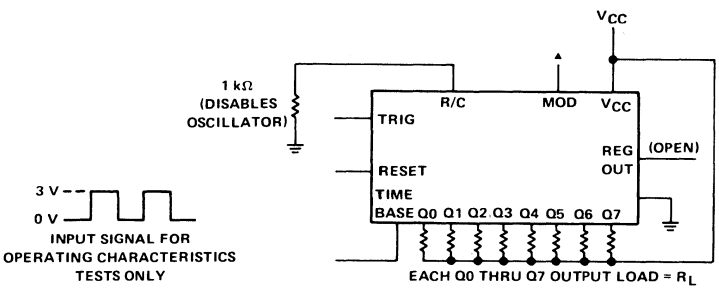


FIGURE 2–COUNTER TEST CIRCUIT

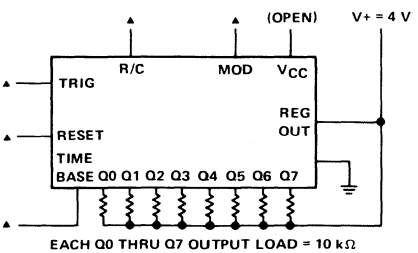


FIGURE 3–REDUCED-POWER TEST CIRCUIT
(TIME BASE DISABLED)

▲These connections may be open or grounded for this test.

Special Functions

5

TYPICAL CHARACTERISTICS

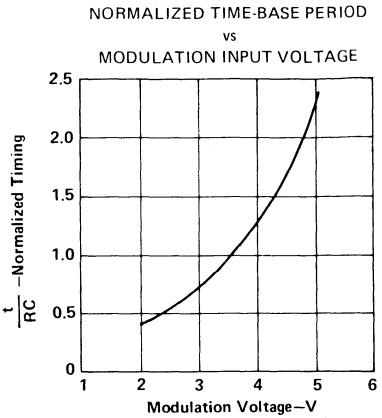


FIGURE 4

TYPICAL APPLICATION INFORMATION

Figure 5 shows voltage waveforms for typical operation of the uA2240C. If both reset and trigger inputs are low during power-up, the timer/counter will be in a reset state with all binary (Q) outputs high and the oscillator stopped. In this state, a high level on the trigger input starts the time-base oscillator. The initial negative-going pulse from the oscillator sets the Q outputs to low logic levels at the beginning of the first time-base period. The uA2240C will ignore any further signals at the trigger input until after a reset signal is applied to the reset input. With the trigger input low, a high level at the reset input will set Q outputs high and stop the time-base oscillator. If the reset signal occurs while the trigger input is high, the reset is ignored. If the reset input remains high when the trigger input goes low, the uA2240C will reset.

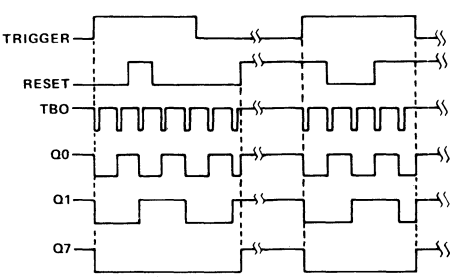


FIGURE 5—TIMING DIAGRAM OF OUTPUT WAVEFORMS

TYPICAL APPLICATION INFORMATION

In monostable applications of the uA2240C one or more of the binary outputs will be connected to the reset terminal as shown in Figure 6. The binary outputs are open-collector stages that can be connected together to a common pull-up resistor to provide a "wired-OR" function. The combined output will be low as long as any one of the outputs is low. This type of arrangement can be used for time delays that are integer multiples of the time-base period. For example, if Q5 ($2^5 = 32$) only is connected to the reset input, every trigger pulse will generate a 32-period active-low output. Similarly, if Q0, Q4, and Q5 are connected to reset, each trigger pulse creates a 49-period delay.

In astable operation, the uA2240C will free-run from the time it is triggered until it receives an external reset signal.

The period of the time-base oscillator is equal to the RC time constant of an external resistor and capacitor connected as shown in Figure 6 when the modulation input is open (approximately 3.5 volts internal, see Figure 4). Under conditions of high supply voltage ($V_{CC} > 7$ V) and low value of timing capacitor ($C < 0.1$ μF), the pulse duration of the time-base oscillator may be too short to properly trigger the counters. This situation can be corrected by adding a 300-picofarad capacitor between the time-base output and ground. The time-base output (TBO) is an open-collector output that requires a 20-kΩ pull-up resistor to Pin 15 for proper operation. The time-base pin may also be used as an input to the counters for an external time-base or as an active-low inhibit input to interrupt counting without resetting.

The modulation input varies the ratio of the time-base period to the RC time constant as a function of the dc bias voltage (see Figure 4). It can also be used to synchronize the timer/counter to an external clock or sync signal.

The regulator output is used internally to drive the binary counters and the control logic. This terminal can also be used to supply voltage to additional uA2240C devices to minimize power dissipation when several timer circuits are cascaded. For circuit operation with an external clock, the regulator output can be used as the V_{CC} input terminal to power down the internal time base and reduce power dissipation. When supply voltages less than 4.5 volts are used with the internal time base, Pin 15 should be shorted to Pin 16.

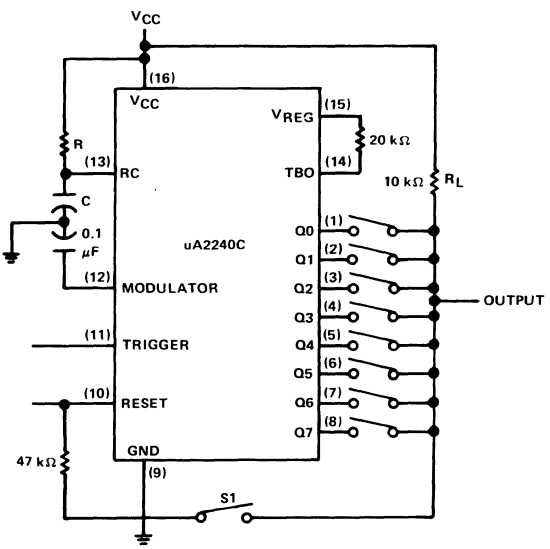


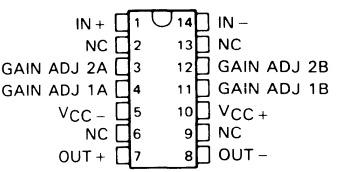
FIGURE 6–BASIC CONNECTIONS FOR TIMING APPLICATIONS

TYPES uA733M, uA733C
DIFFERENTIAL VIDEO AMPLIFIERS

D922, NOVEMBER 1970 – REVISED OCTOBER 1979

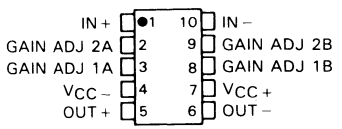
- 200 MHz Bandwidth
- 250 kΩ Input Resistance
- Selectable Nominal Amplification of 10, 100, or 400
- No Frequency Compensation Required
- Designed to be Interchangeable with Fairchild μA733M and μA733C

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC No internal connection

uA733M . . . U FLAT PACKAGE
(TOP VIEW)



description

The uA733 is a monolithic two-stage video amplifier with differential inputs and differential outputs.

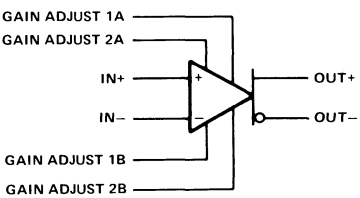
Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

Fixed differential amplification of 10, 100, or 400 may be selected without external components, or amplification may be adjusted from 10 to 400 by the use of a single external resistor connected between 1A and 1B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disc-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

The uA733M is characterized for operation over the full military temperature range of −55°C to 125°C; the uA733C is characterized for operation from 0°C to 70°C.

symbol



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA733M	uA733C	UNIT
Supply voltage V_{CC+} (See Note 1)		8	8	V
Supply voltage V_{CC-} (See Note 1)		−8	−8	V
Differential input voltage		±5	±5	V
Common-mode input voltage		±6	±6	V
Output current		10	10	mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	C
Storage temperature range		−65 to 150	−65 to 150	C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or U package	300	300	C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	N package		260	C

NOTES: 1. All voltage values, except differential input voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J package, uA733M chips are alloy mounted; uA733C chips are glass mounted.

electrical characteristics, V_{CC+} = 6 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	uA733M			uA733C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification	1	V_{OD} = 1 V	1	300	400	500	250	400	600	
				2	90	100	110	80	100	120	
				3	9	10	11	8	10	12	
BW	Bandwidth	2	R_S = 50 Ω	1		50			50		MHz
				2		90			90		
				3		200			200		
I_{IO}	Input offset current			Any		0.4	3		0.4	5	μA
I_{IB}	Input bias current			Any		9	20		9	30	μA
V_{ICR}	Common-mode input voltage range	1		Any	±1			±1			V
V_{OC}	Common-mode output voltage	1		Any	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1		1		0.6	1.5		0.6	1.5	V
				2 & 3		0.35	1		0.35	1.5	
V_{OPP}	Maximum peak-to-peak output voltage swing	1		Any	3	4.7		3	4.7		V
r_i	Input resistance *	3	V_{OD} ≈ 1 V	1		4			4		kΩ
				2	20	24		10	24		
				3		250			250		
r_o	Output resistance					20			20		Ω
C_i	Input capacitance	3	V_{OD} ≈ 1 V	2		2			2		pF
CMRR	Common-mode rejection ratio	4	V_{IC} = ±1 V, f ≈ 100 kHz	2	60	86		60	86		dB
			V_{IC} = ±1 V, f = 5 MHz	2		70			70		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	1	$\Delta V_{CC+} \approx \pm 0.5$ V, $\Delta V_{CC-} \approx \pm 0.5$ V	2	50	70		50	70		dB
V_n	Broadband equivalent input noise voltage	5	BW = 1 kHz to 10 MHz	Any		12			12		μV
t_{pd}	Propagation delay time*	2	R_S = 50 Ω, Output voltage step = 1 V	1		7.5			7.5		ns
				2		6.0	10		6.0	10	
				3		3.6			3.6		
t_r	Rise time *	2	R_S = 50 Ω, Output voltage step = 1 V	1		10.5			10.5		ns
				2		4.5	10		4.5	12	
				3		2.5			2.5		
$I_{sink(max)}$	Maximum output sink current			Any	2.5	3.6		2.5	3.6		mA
I_{CC}	Supply current		No load, no signal	Any		16	24		16	24	mA

†The gain option is selected as follows:
Gain Option 1 . . . Gain-adjust pin 1A is connected to pin 1B, and pins 2A and 2B are open.
Gain Option 2 . . . Gain-adjust pin 1A and pin 1B are open, pin 2A is connected to pin 2B.
Gain Option 3 . . . All four gain-adjust pins are open.

*For M-suffix devices these parameters are guaranteed but not tested.

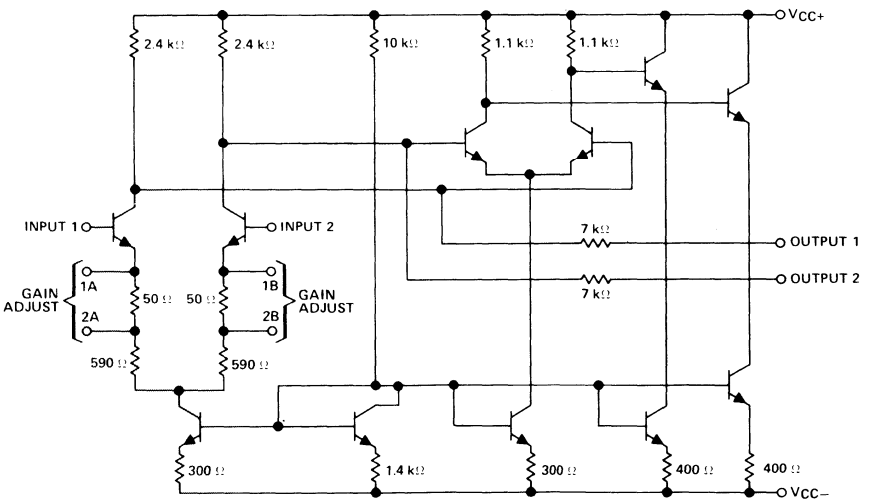
electrical characteristics (continued), V_{CC+} = 6 V, V_{CC-} = −6 V
T_A = −55°C to 125°C for uA733M, 0°C to 70°C for uA733C

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	uA733M		uA733C		UNIT
					MIN	MAX	MIN	MAX	
A_{VD}	Large-signal differential voltage amplification	1	V_{OD} = 1 V	1	200	600	250	600	
				2	80	120	80	120	
				3	8	12	8	12	
I_{IO}	Input offset current			Any		5		6	μA
I_{IB}	Input bias current			Any		40		40	μA
V_{ICR}	Common-mode input voltage range	1		Any	±1		±1		V
V_{OO}	Output offset voltage	1		1		1.5		1.5	V
				2 & 3		1.2		1.5	
V_{OPP}	Maximum peak-to-peak output voltage swing	1		Any	2.5		2.8		V
r_i	Input resistance*	3	V_{OD} ≤ 1 V	2	8		8		kΩ
CMRR	Common-mode rejection ratio	4	V_{IC} = ±1 V, f ≤ 100 kHz	2	50		50		dB
			V_{IC} = ±1 V, f = 5 MHz	2					
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	1	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50		50		dB
$I_{sink(max)}$	Maximum output sink current			Any	2.2		2.5		mA
I_{CC}	Supply current		No load, No signal	Any		27		27	mA

†The gain option is selected as follows:
Gain Option 1 . . . Gain-adjust pin 1A is connected to pin 1B, and pins 2A and 2B are open.
Gain Option 2 . . . Gain-adjust pin 1A and pin 1B are open, pin 2A is connected to pin 2B.
Gain Option 3 . . . All four gain-adjust pins are open.

*For M-suffix devices these parameters are guaranteed but not tested.

schematic



Component values shown are nominal.

DEFINITION OF TERMS

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in voltage between the output terminals to the change in voltage between the input terminals producing it.

Bandwidth (BW) The range of frequencies within which the differential gain of the amplifier is not more than 3 dB below its low-frequency value.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the inputs grounded.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the inputs grounded.

Input Voltage Range (V_I) The range of voltage that if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Common-Mode Output Voltage (V_{OC}) The average of the d-c voltages at the two output terminals.

Output Offset Voltage (V_{OO}) The difference between the d-c voltages at the two output terminals when the input terminals are grounded.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between either output terminal and ground.

Input Capacitance (C_i) The capacitance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) The absolute value of the ratio of the change in power supply voltages to the change in input offset voltage. For these devices, both supply voltages are varied symmetrically.

Equivalent Input Noise Voltage (V_n) The voltage of an ideal voltage source (having an internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.

Propagation Delay Time (t_{pd}) The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Maximum Output Sink Current ($I_{sink(max)}$) The maximum available current into either output terminal when that output is at its most negative potential.

Supply Current (I_{CC}) The average of the magnitudes of the two supply currents I_{CC1} and I_{CC2}.

PARAMETER MEASUREMENT INFORMATION

test circuits

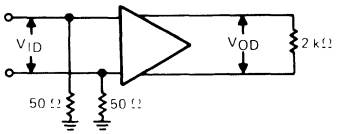


FIGURE 1

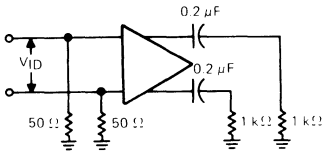


FIGURE 2

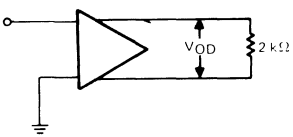


FIGURE 3

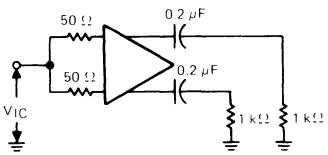


FIGURE 4

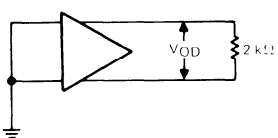
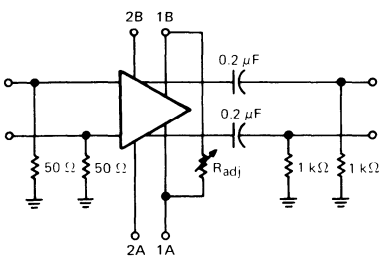


FIGURE 5



VOLTAGE AMPLIFICATION ADJUSTMENT

FIGURE 6

TYPICAL CHARACTERISTICS

PHASE SHIFT
vs
FREQUENCY

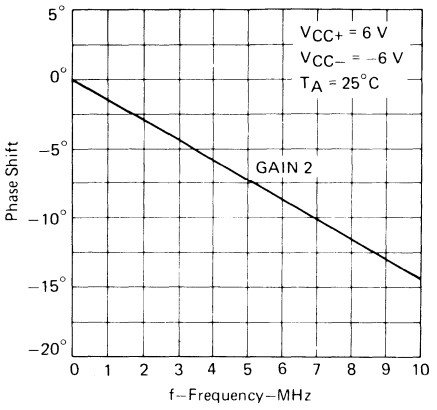


FIGURE 7

PHASE SHIFT
vs
FREQUENCY

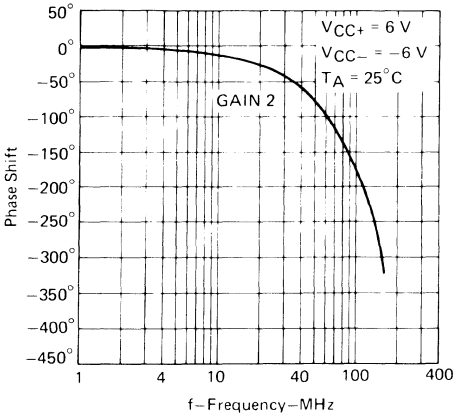


FIGURE 8

VOLTAGE AMPLIFICATION
(SINGLE-ENDED OR DIFFERENTIAL)
vs
TEMPERATURE

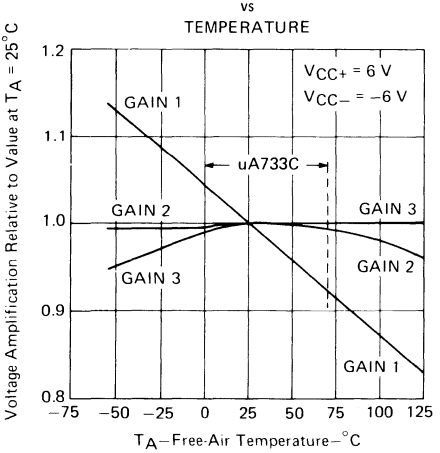


FIGURE 9

VOLTAGE AMPLIFICATION
(SINGLE-ENDED OR DIFFERENTIAL)
vs
SUPPLY VOLTAGE

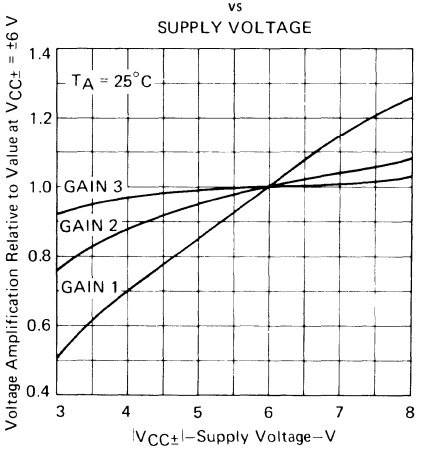


FIGURE 10

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
RESISTANCE BETWEEN G1A AND G1B

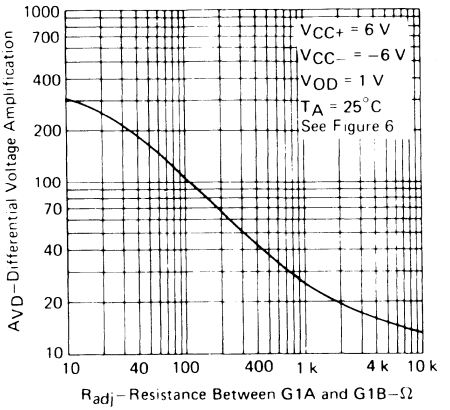


FIGURE 11

SINGLE-ENDED VOLTAGE AMPLIFICATION
vs
FREQUENCY

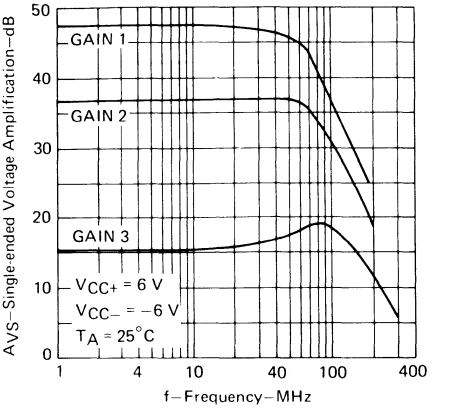


FIGURE 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

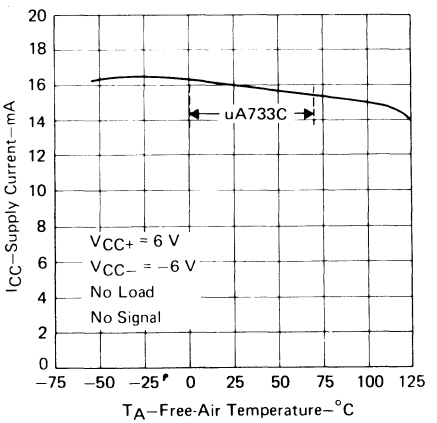


FIGURE 13

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

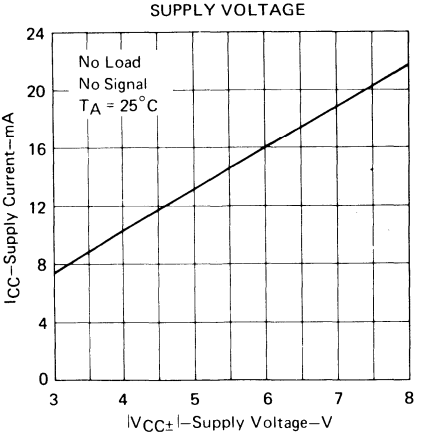


FIGURE 14

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

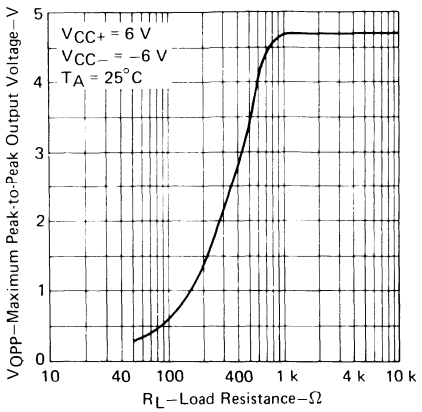


FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

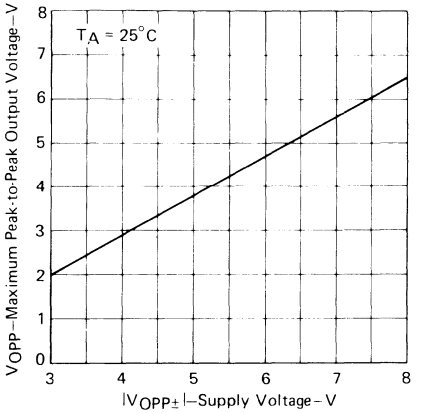


FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

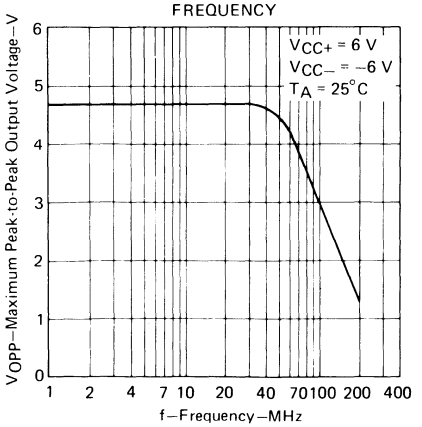


FIGURE 17

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

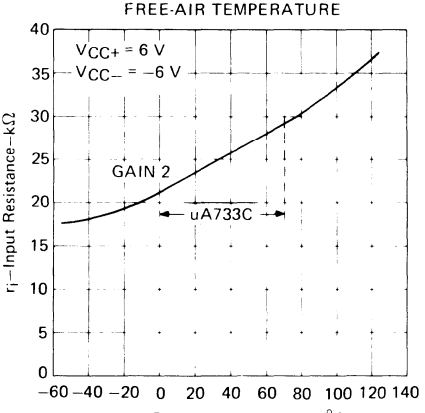


FIGURE 18

General Information 1

Thermal Information 2

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SERIES REGULATORS

Input Regulation

The change in output voltage, often expressed as a percentage of output voltage, for a change in input voltage from one level to another level.
NOTE: Sometimes this characteristic is normalized with respect to the input voltage change.

Ripple Rejection

The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.
NOTE: This is the reciprocal of ripple sensitivity.

Ripple Sensitivity

The ratio of the peak-to-peak output ripple voltage, sometimes expressed as a percentage of output voltage, to the peak-to-peak input ripple voltage.
NOTE: This is the reciprocal of ripple rejection.

Output Regulation

The change in output voltage, often expressed as a percentage of output voltage, for a change in load current from one level to another level.

Output Resistance

The output resistance under small-signal conditions.

Temperature Coefficient of Output Voltage (αVO)

The ratio of the change in output voltage, usually expressed as a percentage of output voltage, to the change in temperature. This is the average value for the total temperature change.

$$\alpha VO = \pm \left[\frac{V_O \text{ at } T_2 - V_O \text{ at } T_1}{V_O \text{ at } 25°C} \right] \left[\frac{100\%}{T_2 - T_1} \right]$$

Output Voltage Change with Temperature

The percentage change in the output voltage for a change in temperature. This is the net change over the total temperature range.

Output Voltage Long-Term Drift

The change in output voltage over a long period of time.

Output Noise Voltage

The rms value of the ac component of the output voltage, sometimes expressed as a percentage of the dc output voltage, with constant load and no input ripple.

Current-Limit Sense Voltage

The current-sense voltage at which current limiting occurs.

Current-Sense Voltage

The voltage that is a function of the load current and is normally used for control of the current-limiting circuitry.

Dropout Voltage

The low input-to-output differential voltage at which the circuit ceases to regulate against further reductions in input voltage.

Feedback Sense Voltage

The voltage that is a function of the output voltage and is used for feedback control of the regulator.

Reference Voltage

The voltage that is compared with the feedback sense voltage to control the regulator.

Bias Current

The difference between input and output currents.
NOTE: This is sometimes referred to as quiescent current.

Standby Current

The input current drawn by the regulator with no output load and no reference voltage load.

Short-Circuit Output Current

The output current of the regulator with the output shorted to ground.

Peak Output Current

The maximum output current that can be obtained from the regulator due to limiting circuitry within the regulator.

Overvoltage Shutdown Voltage

The input voltage applied to a regulator having overvoltage shutdown protection that will cause the output voltage to go nearly to zero.

Junction Temperature, Virtual Junction Temperature

A temperature representing the temperature of the junction(s), field-effect transistor channel(s), or other internal point(s) of heat generation calculated on the basis of a simplified model of the thermal and electrical behavior of the semiconductor device.

SHUNT REGULATORS

NOTE: These terms and symbols are based on JEDEC and IEC standards for voltage regulator diodes.

Shunt Regulator

A device having a voltage-current characteristic similar to that of a voltage-regulator diode; normally biased to operate in a region of low differential resistance (corresponding to the breakdown region of a regulator diode) to develop across its terminals an essentially constant voltage throughout a specified current range.

Anode

The electrode to which the regulator current flows within the regulator when it is biased for regulation.

Cathode

The electrode from which the regulator current flows within the regulator when it is biased for regulation.

Reference Input Voltage (V_{ref}) (of an adjustable shunt regulator)

The voltage at the reference input terminal with respect to the anode terminal.

Temperature Coefficient of Reference Voltge (αV_{ref})

The ratio of the change in reference voltage to the change in temperature. This is the average value for the total temperature change.
To obtain a value in ppm/°C:

$$\alpha Vref = \left[\frac{V_{ref} \text{ at } T_2 - V_{ref} \text{ at } T_1}{V_{ref} \text{ at } 25°C}\right]\left[\frac{10^6}{T_2 - T_1}\right]$$

Regulator Voltage (V_Z)

The dc voltage across the regulator when it is biased for regulation.

Regulator Current (I_Z)

The dc current through the regulator when it is biased for regulation.

Regulator Current near Lower Knee of Regulation Range (I_{ZK})

The regulator current near the lower limit of the region within which regulation occurs; this corresponds to the breakdown knee of a regulator diode.

Regulator Current at Maximum Limit of Regulation Range (I_{ZM})

The regulator current above which the differential resistance of the regulator significantly increases.

Differential Regulator Resistance (r_z)

The quotient of a change in voltage across the regulator and the corresponding change in current through the regulator when it is biased for regulation.

Noise Voltage (V_{nz})

The rms value of the ac component of the voltage across the regulator with the regulator biased for regulation and with no input ripple.

MARCH 1988

FEATURES

- 20μA to 20mA operating range
- 1% initial voltage tolerance
- 1 Ω dynamic impedance
- Very low power consumption

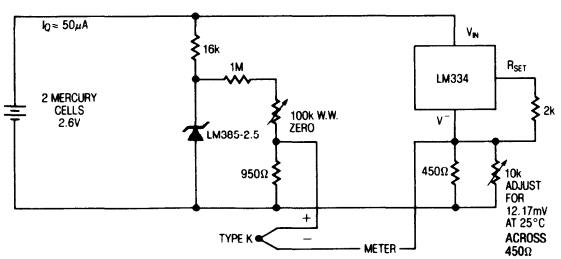
APPLICATIONS

- Portable meter references
- Portable test instruments
- Battery operated systems
- Panel meters
- Current loop instrumentation

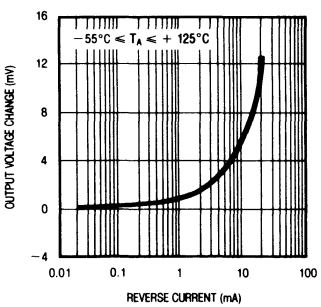
DESCRIPTION

The LM185-2.5 is a two terminal band gap reference diode that has been designed for applications which require precision performance with micropower operation. The device provides operating specifications at currents as low as 20μA. The nominal voltage is 2.5V with both 1% and 2% tolerances available. Some additional features are: maximum dynamic impedance of 1Ω, low noise and excellent stability over time and temperature. The advanced design, processing and testing techniques make Linear's LM185-2.5 a superior choice over previous designs. A circuit for cold junction compensation of a thermocouple is shown below.

Thermocouple Cold Junction Compensator



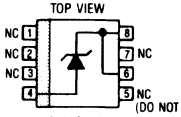
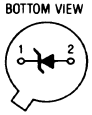
Reverse Voltage Change



ABSOLUTE MAXIMUM RATINGS

Reverse Breakdown Current..... 30mA
Forward Current..... 10mA
Operating Temperature Range
LM185-2.5..... −55°C to 125°C
LM385-2.5..... 0°C to 70°C
Storage Temperature Range
LM185-2.5..... −65°C to 150°C
LM385-2.5..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 D PACKAGE PLASTIC SO	LM385D-1.2 LM385D-2.5
	PART MARKING
	3851 (1.2V VERSION) 3852 (2.5V VERSION)
 LD PACKAGE TO-46 METAL CAN	LM185LD-2.5 LM385LD-2.5 LM385BLD-2.5
 LP PACKAGE TO-92 PLASTIC	LM385LP-2.5 LM385BLP-2.5

The D packages are available taped and reeled. Add the suffix R to the device type when ordering. (e.g., LM385DR-1.2)

ELECTRICAL CHARACTERISTICS (See Note 1)

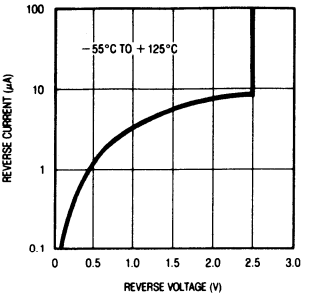
SYMBOL	PARAMETER	CONDITIONS		LM185-2.5 MIN	LM185-2.5 TYP	LM185-2.5 MAX	LM385-2.5/385B-2.5 MIN	LM385-2.5/385B-2.5 TYP	LM385-2.5/385B-2.5 MAX	UNITS
V_Z	Reverse Breakdown Voltage	$T_A = 25°C$, $20\mu A \leq I_R \leq 20mA$								
		LM185-2.5		2.462	2.5	2.538				V
		LM385-2.5					2.425	2.5	2.575	V
		LM385B-2.5					2.462	2.5	2.538	V
$\frac{\Delta V_Z}{\Delta \text{ Temp}}$	Average Temperature Coefficient	$20\mu A \leq I_R \leq 20mA$			20			20		ppm/°C
I_{min}	Minimum Operating Current	$T_{min} \leq T_A \leq T_{max}$	●		8	20		8	20	μA
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Voltage Change with Current	$20\mu A \leq I_R \leq 1mA$								
		$T_A = 25°C$				1			2	mV
		$T_{min} \leq T_A \leq T_{max}$	●			1.5			2.5	mV
		$1mA \leq I_R \leq 20mA$								
		$T_A = 25°C$				10			20	mV
		$T_{min} \leq T_A \leq T_{max}$	●			20			25	mV
r_Z	Reverse Dynamic Impedance	$I_R = 100\mu A$								
		$T_A = 25°C$			0.2	0.6		0.4	1	Ω
		$T_{min} \leq T_A \leq T_{max}$	●			1.5			1.5	Ω
e_n	Wide Band Noise (RMS)	$10Hz \leq f \leq 10kHz$, $I_R = 100\mu A$			120			120		μV
$\frac{\Delta V_Z}{\Delta \text{ Time}}$	Long Term Stability	$T_A = 25°C \pm 0.1°C$, $I_R = 100\mu A$			20			20		ppm/kHr

The ● denotes the specifications which apply over full operating temperature range.

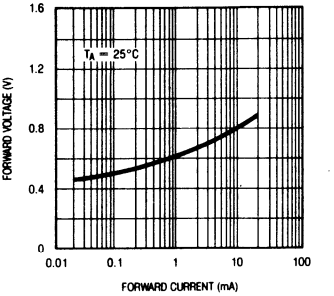
Note 1: All specifications are for $T_A = 25°C$ unless otherwise noted. For the LM185-2.5 $T_{min} = -55°C$ and $T_{max} = +125°C$. For LM385-2.5 $T_{min} = 0°C$ and $T_{max} = +70°C$.

TYPICAL PERFORMANCE CHARACTERISTICS

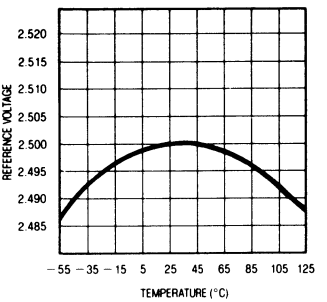
Reverse Characteristics



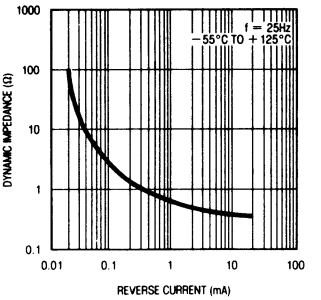
Forward Characteristics



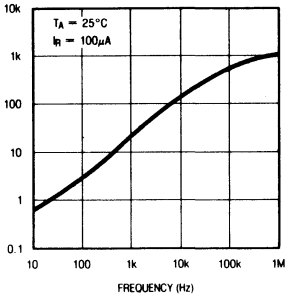
Temperature Drift



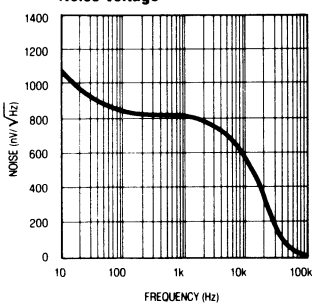
Reverse Dynamic Impedance



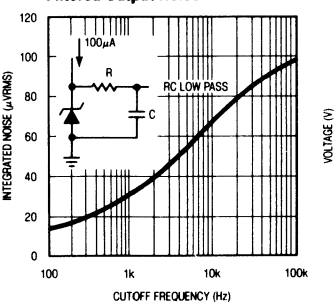
Reverse Dynamic Impedance



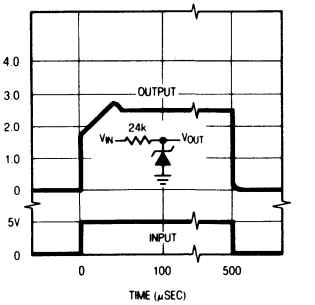
Noise Voltage



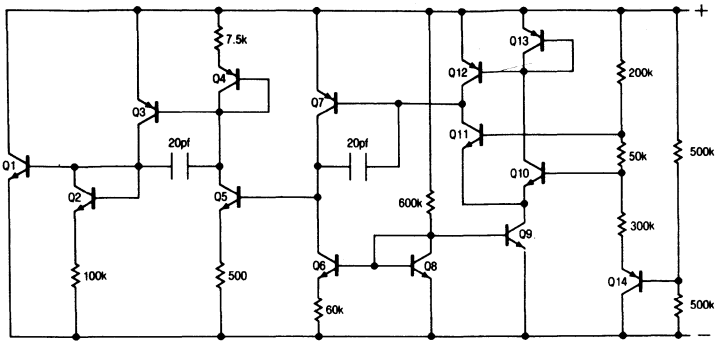
Filtered Output Noise



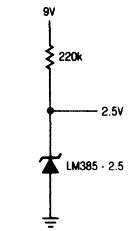
Response Time



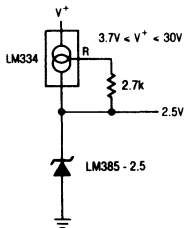
SCHEMATIC DIAGRAM



TYPICAL APPLICATIONS



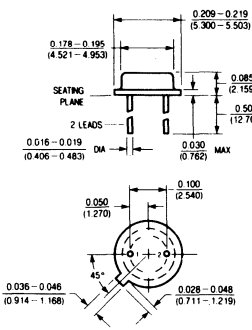
REFERENCE FROM A 9V BATTERY



OPERATION OVER A WIDE SUPPLY RANGE

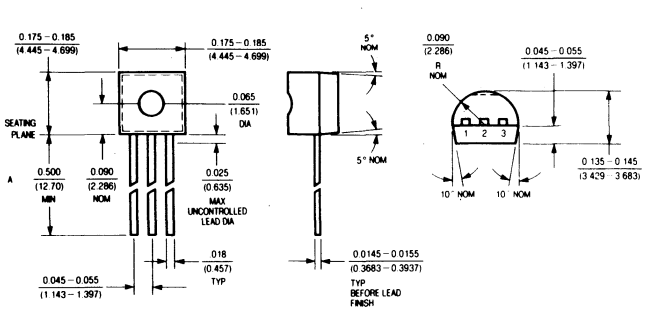
PACKAGE DESCRIPTION

LD Package, 2 Lead TO-46 Metal Can



$T_j$max	Θ_{ja}	Θ_{jc}
150°C	440°C/W	80°C/W

LP Package, 3 Lead TO-92 Plastic

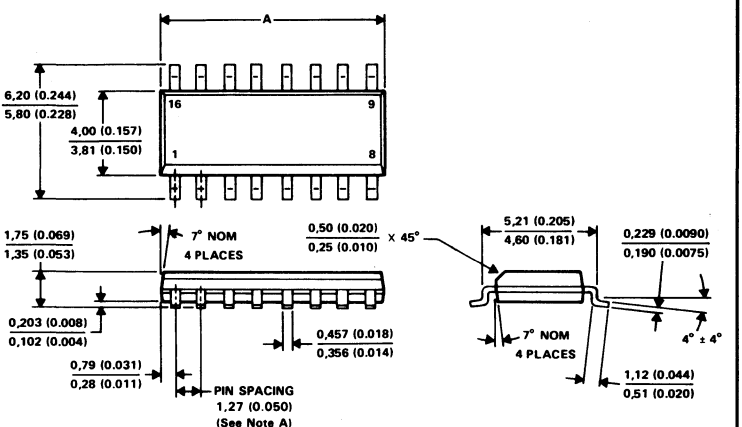


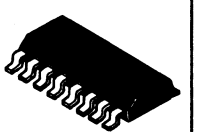
$T_j$max	Θ_{ja}
150°C	160°C/W

D008, D014, and D016 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008, D014, and D016
(16-pin package used for illustration)





DIM \ PINS	8	14	16
A MIN	4,80 (0.189)	8,55 (0.337)	9,80 (0.386)
A MAX	5,00 (0.197)	8,74 (0.344)	10,00 (0.394)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

TYPES LM217, LM317
3-TERMINAL ADJUSTABLE REGULATORS

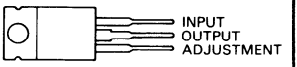
D2212, SEPTEMBER 1977 – REVISED DECEMBER 1982

- **Output Voltage Range Adjustable from 1.2 V to 37 V**
- **Guaranteed Output Current Capability of 1.5 A**
- **Input Regulation Typically 0.01% Per Input-Volt Change**
- **Output Regulation Typically 0.1%**
- **Peak Output Current Constant Over Temperature Range of Regulator**
- **Popular 3-Lead TO-220AB Package**
- **Ripple Rejection Typically 80 dB**
- **Direct Replacement for National LM217 and LM317**

terminal assignments

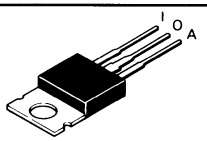
KC PACKAGE

(TOP VIEW)



THE OUTPUT TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

TO-220AB



description

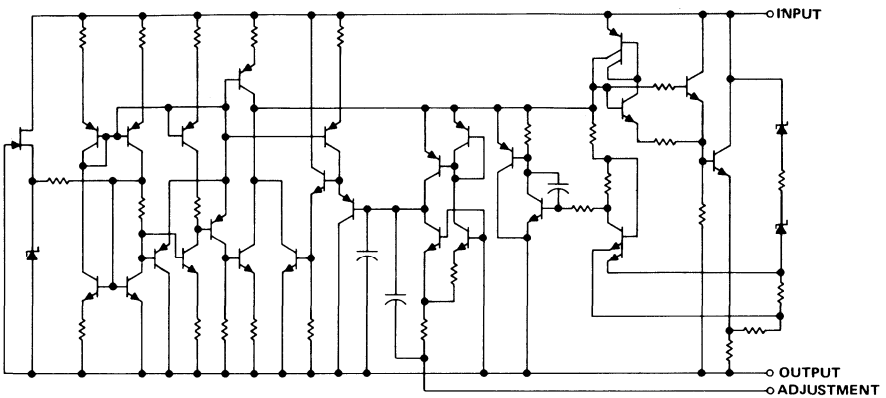
The LM217, and LM317 are adjustable 3-terminal positive-voltage regulators capable of supplying 1.5 amperes over a differential voltage range of 3 volts to 40 volts. They are exceptionally easy to use and require only two external resistors to set the output voltage. Both input and output regulation are better than standard fixed regulators. The devices are packaged in a standard transistor package that is easily mounted and handled.

In addition to higher performance than fixed regulators, these regulators offer full overload protection available only in integrated circuits. Included on the chip are current limit, thermal overload protection, and safe-area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected. Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection, which is difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, these regulators are useful in a wide variety of other applications. The primary applications of each of these regulators is that of a programmable output regulator, but by connecting a fixed resistor between the adjustment terminal and the output terminal, each device can be used as a precision current regulator. Even though the regulator is floating and sees only the input-to-output differential voltage, use of these devices to regulate output voltages that would cause the maximum-rated differential voltage to be exceeded if the output became shorted to ground is not recommended. The TL783 or TL783A is recommended for output voltages exceeding 37 volts. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground, which programs the output to 1.2 volts where most loads draw little current.

The LM217 and LM317 are characterized for operation from −25°C to 150°C and from 0°C to 125°C, respectively.

schematic



absolute maximum ratings over operation temperature range (unless otherwise noted)

	LM217	LM317	UNIT
Input-to-output differential voltage, $V_I - V_O$	40	40	V
Continuous total dissipation at 25°C free-air temperature (see Note 1)	2000	2000	mW
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)	20	20	W
Operating free-air, case, or virtual junction temperature range	−25 to 150	0 to 125	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	260	°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 15 and 16. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

	LM217		LM317		UNIT
	MIN	MAX	MIN	MAX	
Output current, I_O	5	1500	10	1500	mA
Operating virtual junction temperature, T_J	−25	150	0	125	°C

electrical characteristics over recommended ranges of operating virtual junction temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		LM217			LM317			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input regulation (See Note 2)	$V_I - V_O$ = 3 V to 40 V, See Note 3	T_J = 25°C		0.01	0.02		0.01	0.04	%/V
		I_O = 10 mA to 1.5 A		0.02	0.05		0.02	0.07	
Ripple rejection	V_O = 10 V,	f = 120 Hz		65			65		dB
	V_O = 10 V, 10-μF capacitor between ADJ and ground	f = 120 Hz	66	80		66	80		
Output regulation	I_O = 10 mA to 1.5 A, T_J = 25°C, See Note 3	$V_O \leq 5$ V		5	15		5	25	mV
		$V_O > 5$ V		0.1	0.3		0.1	0.5	%
	I_O = 10 mA to 1.5 A, See Note 3	$V_O \leq 5$ V		20	50		20	70	mV
		$V_O > 5$ V		0.3	1		0.3	1.5	%
Output voltage change with temperature	T_J = MIN to MAX			1			1		%
Output voltage long-term drift (see Note 4)	After 1000 h at T_J = MAX and $V_I - V_O$ = 40 V			0.3	1		0.3	1	%
Output noise voltage	f = 10 Hz to 10 kHz, T_J = 25°C			0.003			0.003		%
Minimum output current to maintain regulation	$V_I - V_O$ = 40 V			3.5	5		3.5	10	mA
Peak output current	$V_I - V_O \leq 15$ V		1.5	2.2		1.5	2.2		A
	$V_I - V_O \leq 40$ V			0.4			0.4		
Adjustment-terminal current				50	100		50	100	μA
Change in adjustment-terminal current	$V_I - V_O$ = 2.5 V to 40 V, I_O = 10 mA to 1.5 A			0.2	5		0.2	5	μA
Reference voltage (output to ADJ)	$V_I - V_O$ = 3 V to 40 V, I_O = 10 mA to 1.5 A, P ≤ 20 W		1.2	1.25	1.3	1.2	1.25	1.3	V

† Unless otherwise noted, these specifications apply for the following test conditions; $V_I - V_O$ = 5 V and I_O = 0.5 A. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 2. Input regulation is expressed here as the percentage change in output voltage per 1-volt change at the input.

3. Input regulation and output regulation are measured using pulse techniques ($t_w \leq 10$ μs, duty cycle ≤ 5%) to limit changes in average internal dissipation. Output voltage changes due to large changes in internal dissipation must be taken into account separately.

4. Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

TYPICAL APPLICATION DATA

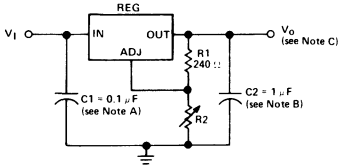


FIGURE 1—ADJUSTABLE VOLTAGE REGULATOR

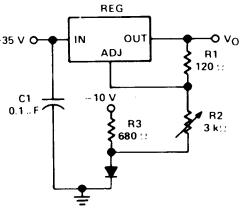


FIGURE 2—0 V to 30 V REGULATOR CIRCUIT

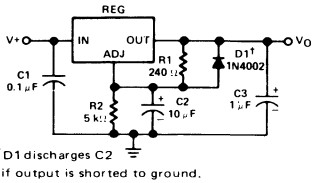


FIGURE 3—ADJUSTABLE REGULATOR CIRCUIT WITH IMPROVED RIPPLE REJECTION

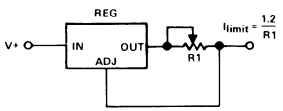


FIGURE 4—PRECISION CURRENT LIMITER CIRCUIT

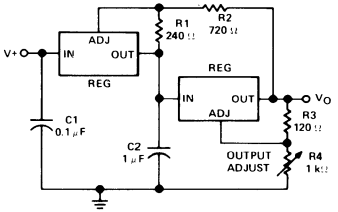


FIGURE 5—TRACKING PREREGULATOR CIRCUIT

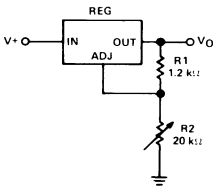


FIGURE 6—1.2 to 20-V REGULATOR CIRCUIT WITH MINIMUM PROGRAM CURRENT

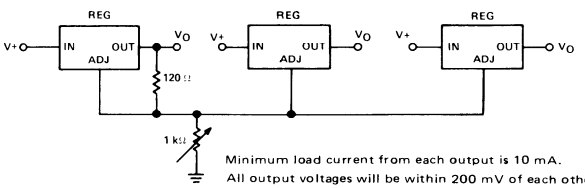


FIGURE 7—ADJUSTING MULTIPLE ON-CARD REGULATORS WITH A SINGLE CONTROL

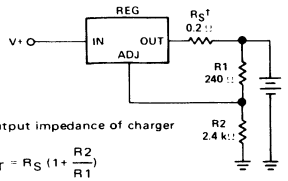
NOTES: A. Use of an input bypass capacitor is recommended if regulator is far from filter capacitors.

B. Use of an output capacitor improves transient response but is optional.

C. Output voltage is calculated from the equation: $V_O = V_{ref}\left(1 + \frac{R2}{R1}\right)$

V_{ref} equals the difference between the output and adjustment terminal voltages.

TYPICAL APPLICATIONS



†R_S controls output impedance of charger

$$Z_{OUT} = R_S\left(1+\frac{R2}{R1}\right)$$

The use of R_S allows low charging rates with a fully charged battery.

FIGURE 8–BATTERY CHARGER CIRCUIT

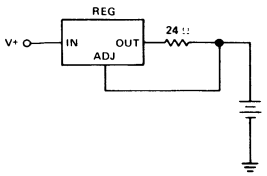


FIGURE 9–50-mA CONSTANT-CURRENT BATTERY CHARGER CIRCUIT

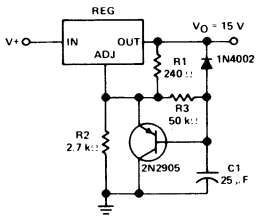


FIGURE 10–SLOW-TURN-ON 15-V REGULATOR CIRCUIT

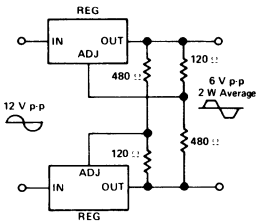
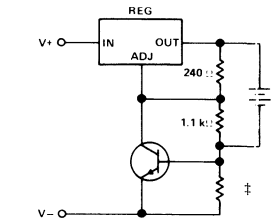


FIGURE 11–A-C VOLTAGE REGULATOR CIRCUIT



‡ This resistor sets peak current (0.6 A for 1 Ω)

FIGURE 12–CURRENT-LIMITED 6-V CHARGER

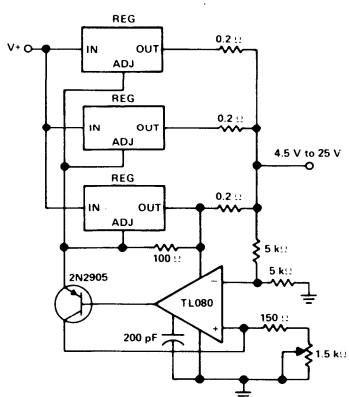
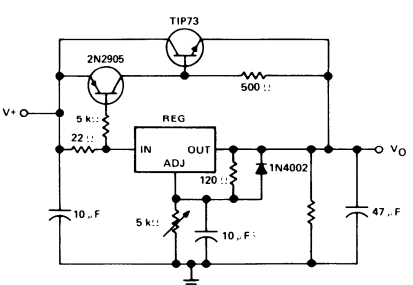


FIGURE 13–ADJUSTABLE 4-A REGULATOR



¶ Minimum load current is 30 mA.
§ Optional capacitor improves ripple rejection

FIGURE 14–HIGH-CURRENT ADJUSTABLE REGULATOR

THERMAL INFORMATION

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

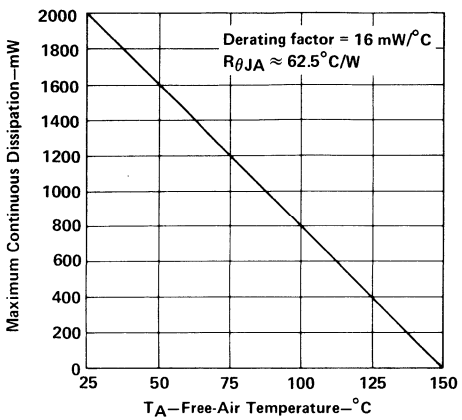


FIGURE 15

CASE TEMPERATURE
DISSIPATION DERATING CURVE

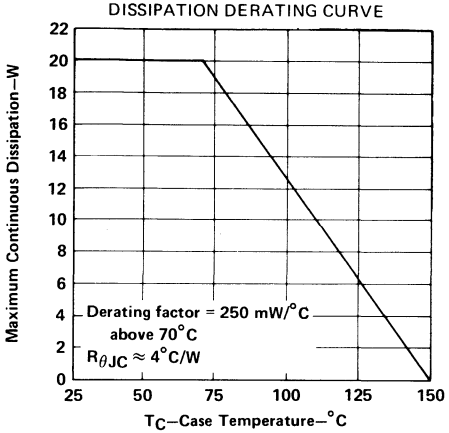


FIGURE 16

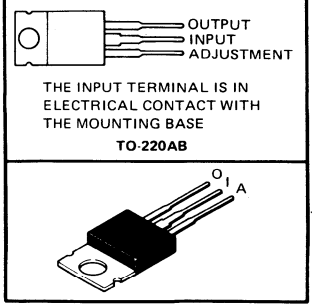
TYPES LM237, LM337
3-TERMINAL ADJUSTABLE REGULATORS

D2640, NOVEMBER 1981

- Output Voltage Range Adjustable from −1.2 V to −37 V
- Guaranteed I_O Capability of 1.5 A
- Input Regulation Typically 0.01% per Input-Volt Change
- Output Regulation Typically 0.3%
- Peak Output Current Constant Over Temperature Range of Regulator
- Ripple Rejection Typically 77 dB
- Direct Replacement for National Semiconductor LM237, LM337

LM237, LM337 . . . KC PACKAGE

(TOP VIEW)



THE INPUT TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

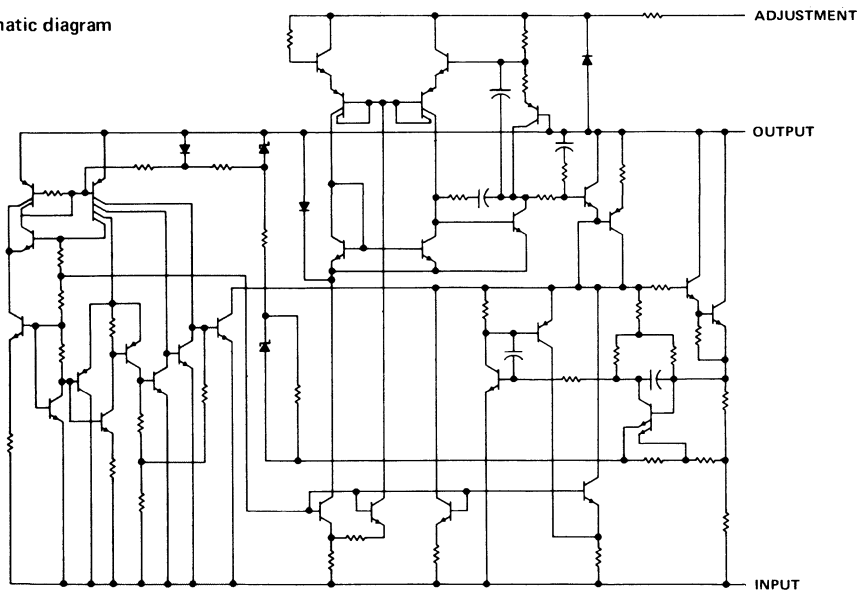
TO-220AB

description

The LM237 and LM337 are adjustable 3-terminal negative-voltage regulators capable of supplying in excess of −1.5 A over an output voltage range of −1.2 V to −37 V. They are exceptionally easy to use, requiring only two external resistors to set the output voltage and one output capacitor for frequency compensation. The current design has been optimized for excellent regulation and low thermal transients. In addition the LM237 and LM337 feature internal current limiting, thermal shutdown, and safe-area compensation, making them virtually immune to blowout by overloads.

The LM237 and LM337 serve a wide variety of applications including local on-card regulation, programmable output voltage regulation, or precision current regulation. They are ideal complements to the LM217 and LM317 adjustable positive-voltage regulators.

schematic diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)

Input-to-output differential voltage, $V_I - V_O$	−40 V
Continuous total dissipation at 25°C free-air temperature (see Note 1)	2 W
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)	20 W
Operating free-air, case, or virtual junction temperature range: LM237	−25°C to 150°C
LM337	0°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 10 seconds	260°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

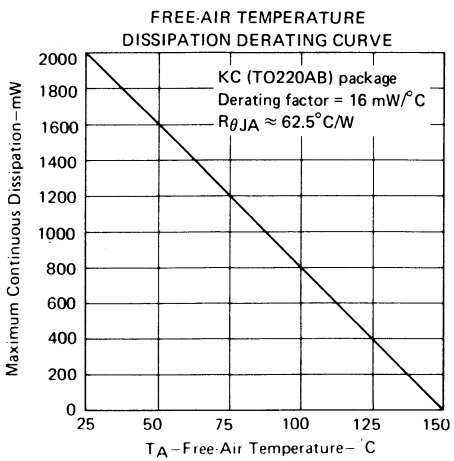


FIGURE 1

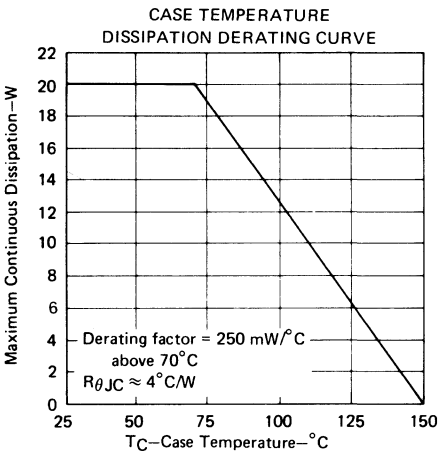


FIGURE 2

recommended operating conditions

		LM237		LM337		UNIT
		MIN	MAX	MIN	MAX	
Output current, I_O	$\lvert V_I - V_O \rvert \leq 40$ V, $P \leq 15$ W	10	1500	10	1500	mA
	$\lvert V_I - V_O \rvert \leq 10$ V, $P \leq 15$ W	6	1500	6	1500	
Operating virtual junction temperature, T_J		−25	150	0	125	°C

electrical characteristics over recommended ranges of operating virtual junction temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		LM237			LM337			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input regulation‡	$V_I - V_O = -3$ V to −40 V, See Note 2	$T_J = 25°C$		0.01	0.02		0.01	0.04	%/V
		T_J = MIN to MAX		0.02	0.05		0.02	0.07	
Ripple rejection	$V_O = -10$ V,	f = 120 Hz		60			60		dB
	$V_O = -10$ V, $C_{ADJ} = 10\ \mu F$	f = 120 Hz	66	77		66	77		
Output regulation	I_O = 10 mA to 1.5 A, $T_J = 25°C$, See Note 2	$\lvert V_O \rvert \leq 5$ V			25			50	mV
		$\lvert V_O \rvert \geq 5$ V			0.5			1	%
	I_O = 10 mA to 1.5 A, See Note 2	$\lvert V_O \rvert \leq 5$ V			50			70	mV
		$\lvert V_O \rvert \geq 5$ V			1			1.5	%
Output voltage change with temperature	T_J = MIN to MAX			0.6			0.6		%
Output voltage long-term drift (see Note 3)	After 1000 h at T_J = MAX and $V_I - V_O = -40$ V			0.3	1		0.3	1	%
Output noise voltage	f = 10 Hz to 10 kHz,	$T_J = 25°C$		0.003			0.003		%
Minimum output current to maintain regulation	$\lvert V_I - V_O \rvert \leq 40$ V			2.5	5		2.5	10	mA
	$\lvert V_I - V_O \rvert \leq 10$ V			1.2	3		1.5	6	
Peak output current	$\lvert V_I - V_O \rvert \leq 15$ V		1.5	2.2		1.5	2.2		A
	$\lvert V_I - V_O \rvert \leq 40$ V,	$T_J = 25°C$	0.24	0.4		0.15	0.4		
Adjustment-terminal current				65	100		65	100	μA
Change in adjustment terminal current	$V_I - V_O$ = −2.5 V to −40 V, I_O = 10 mA to MAX,	$T_J = 25°C$		2	5		2	5	μA
Reference voltage (output to ADJ)	$V_I - V_O = -3$ to −40 V, I_O = 10 mA to 1.5 A, $P \leq$ rated dissipation	$T_J = 25°C$	−1.225	−1.250	−1.275	−1.213	−1.25	−1.287	V
		T_J = MIN to MAX	−1.2	−1.25	−1.3	−1.2	−1.25	−1.3	
Thermal regulation	Initial $T_J = 25°C$,	10-ms pulse		0.002	0.02		0.003	0.04	%/W

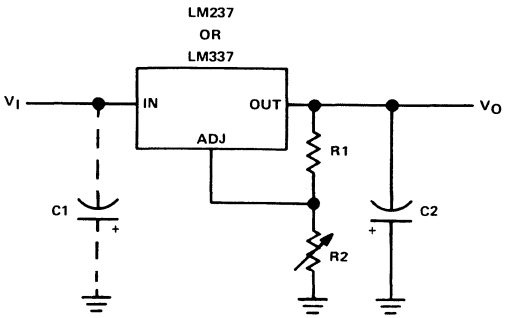
†Unless otherwise noted, these specifications apply for the following test conditions $\lvert V_I - V_O \rvert = 5$ V and $I_O = 0.5$ A. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡Input regulation is expressed here as the percentage change in output voltage per 1 volt change at the input.

NOTES: 2. Input regulation and output regulation are measured using pulse techniques ($t_w \leq 10\ \mu s$, duty cycle ≤ 5%) to limit changes in average internal dissipation. Output voltage changes due to large changes in internal dissipation must be taken into account separately.

3. Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

TYPICAL APPLICATION DATA



R1 R1 is typically 120 Ω.

$$R2 = R1\left(\frac{-V_O}{-1.25} - 1\right)$$ where V_O is the output in volts.

C1 is a 1-μF solid tantalum required only if the regulator is more than 10 cm (4 in.) from the power supply filter capacitor.

C2 is a 1-μF solid tantalum or 10-μF aluminum electrolytic required for stability.

FIGURE 3 – ADJUSTABLE NEGATIVE-VOLTAGE REGULATOR

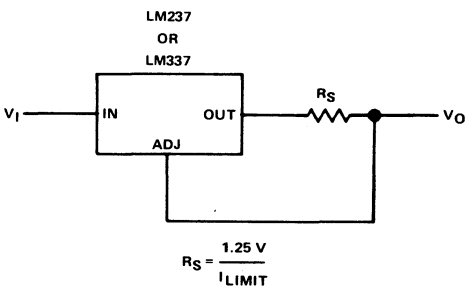


FIGURE 4–CURRENT-LIMITING CIRCUIT

TYPES LM2930-5, LM2930-8
3-TERMINAL POSITIVE REGULATORS

D2733, APRIL 1983

- **Input-Output Differential Less than 0.6 V**
- **Output Current of 150 mA**
- **Reverse Battery Protection**
- **Line Transient Protection**
- **40-Volt Load-Dump Protection**
- **Internal Short-Circuit Current Limiting**
- **Internal Thermal Overload Protection**
- **Mirror-Image Insertion Protection**
- **Direct Replacement for National LM2930 Series**

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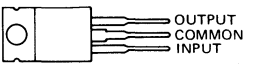
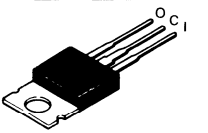
(TOP VIEW)



THE COMMON TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

TO-220AB



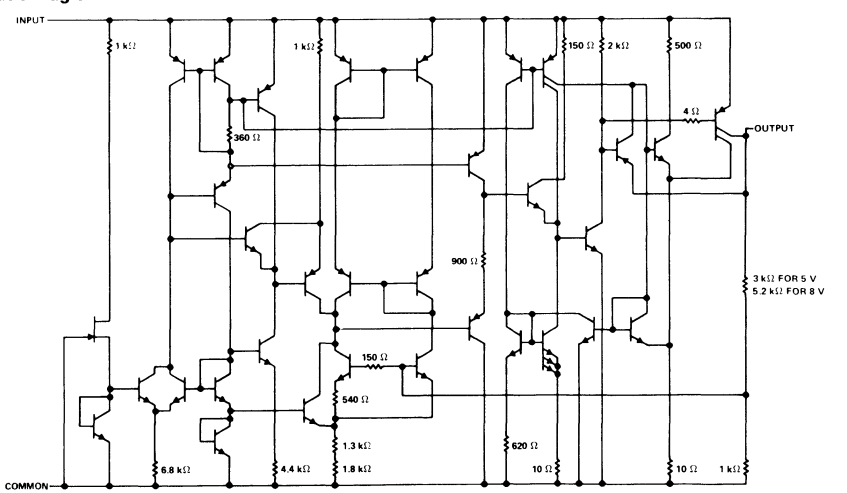
description

The LM2930-5 and LM2930-8 are 3-terminal positive regulators that provide fixed 5-volt and 8-volt regulated outputs. Each features the ability to source 150 milliamperes of output current with an input-output differential of 0.6 volt or less. Familiar regulator features such as current limit and thermal overload protection are also provided.

The LM2930 series has low voltage dropout making it useful for certain battery applications. For example, the low voltage dropout feature allows a longer battery discharge before the output falls out of regulation; the battery supplying the regulator input voltage may discharge to 5.6 volts and still properly regulate the system and load voltage. Supporting this feature, the LM2930 series protects both itself and the regulated system from reverse battery installation or two-battery jumps.

Other protection features include line transient protection for load-dump of up to 40 volts. In this case the regulator shuts down to avoid damaging internal and external circuits. The LM2930 series regulator cannot be harmed by temporary mirror-image insertion.

schematic diagram



All component values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Continuous input voltage	26 V
Transient input voltage: t = 1 s	40 V
Continuous reverse input voltage	−6 V
Transient reverse input voltage: t = 100 ms	−12 V
Continuous total dissipation at 25°C free-air temperature (see Note 1)	2 W
Continuous total dissipation at (or below) 25°C case-temperature (see Note 1)	20 W
Operating free-air, case, or virtual junction temperature	−40°C to 150°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case to 10 seconds	260°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variation in individual device elecrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

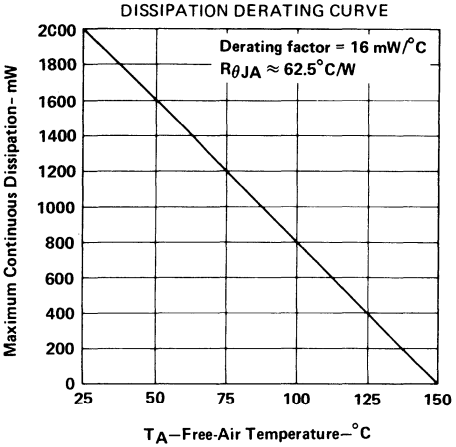


FIGURE 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

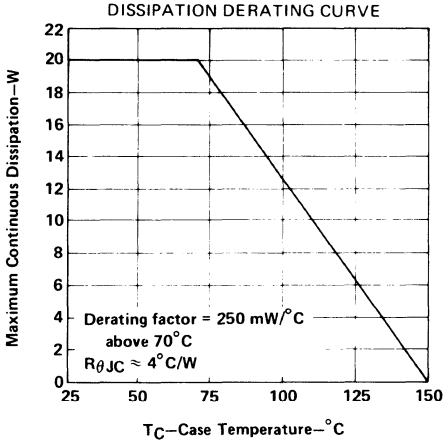


FIGURE 2

recommended operating conditions

		MIN	MAX	UNIT
I_O	Output current		150	mA
T_J	Operating virtual junction temperature	−40	125	°C

LM2930-5 electrical characteristics at 25°C virtual junction temperature, V_I = 14 V, I_O = 150 mA, (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 6 V to 26 V, T_J = −40°C to 125°C	I_O = 5 mA to 150 mA,	4.5	5	5.5	V
Input regulation	I_O = 5 mA	V_I = 9 V to 16 V		7	25	mV
		V_I = 6 V to 26 V		30	80	
Ripple rejection	f = 120 Hz			56		dB
Output regulation	I_O = 5 mA to 150 mA			14	50	mV
Output voltage long-term drift‡	After 1000 h at T_J = 125°C			20		mV
Dropout voltage	I_O = 150 mA			0.32	0.6	V
Output noise voltage	f = 10 Hz to 100 kHz			60		μV
Output voltage during line transients	V_I = −12 V to 40 V,	R_L = 100 Ω	−0.3		5.5	V
Output impedance	I_O = 100 mA, I_o = 10 mA (rms), f = 100 Hz to 10 kHz			200		mΩ
Bias current	I_O = 10 mA			4	7	mA
	I_O = 150 mA			18	40	
Peak output current			150	300	700	mA

LM2930-8 electrical characteristics at 25°C virtual junction temperature, V_I = 14 V, I_O = 150 mA, (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 9.4 V to 26 V, T_J = −40°C to 125°C	I_O = 5 mA to 150 mA,	7.2	8	8.8	V
Input regulation	I_O = 5 mA	V_I = 9.4 V to 16 V		12	50	V
		V_I = 9.4 V to 26 V		50	100	
Ripple rejection	f = 120 Hz			52		dB
Output regulation	I_O = 5 mA to 150 mA			25	50	mV
Output voltage long-term drift‡	After 1000 h at T_J = 125°C			30		mV
Dropout voltage	I_O = 150 mA			0.32	0.6	V
Output noise voltage	f = 10 Hz to 100 kHz			90		μV
Output voltage during line transients	V_I = −12 V to 40 V,	R_L = 100 Ω	−0.3		8.8	V
Output impedance	I_O = 100 mA, I_o = 10 mA (rms), f = 100 Hz to 10 kHz			300		mΩ
Bias current	I_O = 10 mA			4	7	mA
	I_O = 150 mA			18	40	
Peak output current			150	300	700	mA

† Unless otherwise specified, all characteristics, except ripple rejection and noise voltage measurements, are measured using pulse techniques ($t_w \leq$ 10 ms, duty cycle ≤ 5%) with a capacitor of 0.1 μF across the input and a capacitor of 10 μF across the output. Output voltage changes due to changes in internal temperature must be taken into account separately.

‡ Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

TYPICAL CHARACTERISTICS

NORMALIZED OUTPUT VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

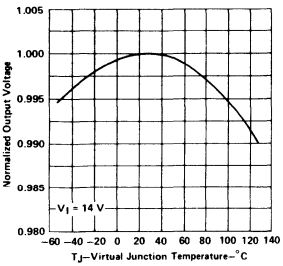


FIGURE 3

LM2930-5
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

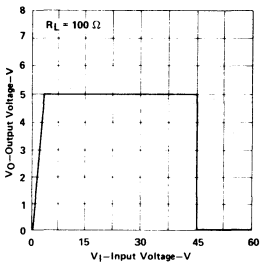


FIGURE 4

LM2930-5
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

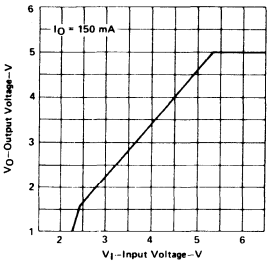


FIGURE 5

RIPPLE REJECTION
vs
FREQUENCY

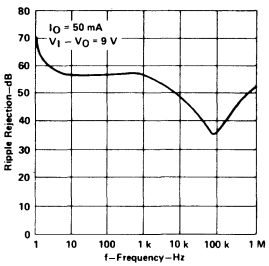


FIGURE 6

RIPPLE REJECTION
vs
OUTPUT CURRENT

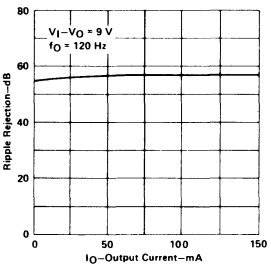


FIGURE 7

DROPOUT VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

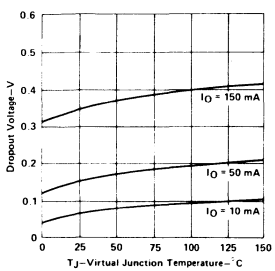


FIGURE 8

DROPOUT VOLTAGE
vs
OUTPUT CURRENT

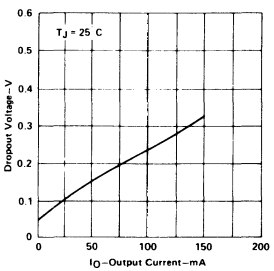


FIGURE 9

OUTPUT IMPEDANCE
vs
FREQUENCY

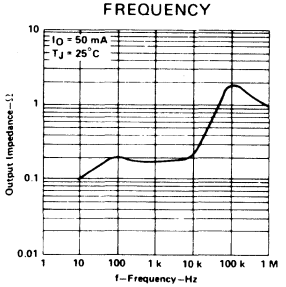


FIGURE 10

TYPICAL CHARACTERISTICS

INPUT CURRENT
vs
INPUT VOLTAGE

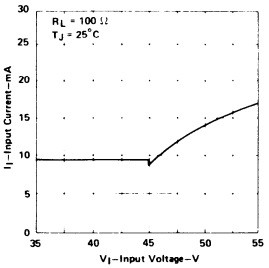


FIGURE 11

LINE TRANSIENT RESPONSE

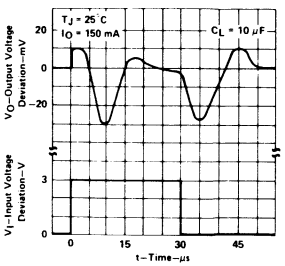


FIGURE 12

INPUT CURRENT
vs
REVERSE INPUT VOLTAGE

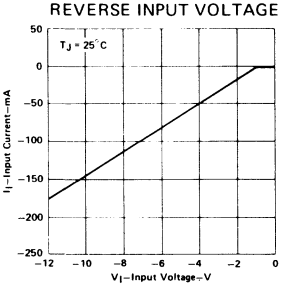


FIGURE 13

OUTPUT VOLTAGE
vs
REVERSE INPUT VOLTAGE

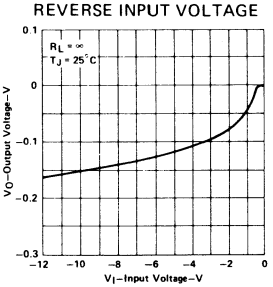


FIGURE 14

LOAD TRANSIENT RESPONSE

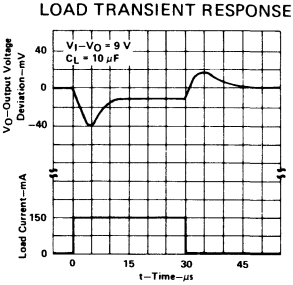


FIGURE 15

LM2905-5

BIAS CURRENT
vs
OUTPUT CURRENT

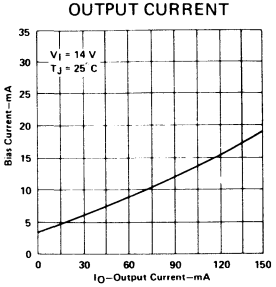


FIGURE 16

BIAS CURRENT
vs
VIRTUAL JUNCTION TEMPERATURE

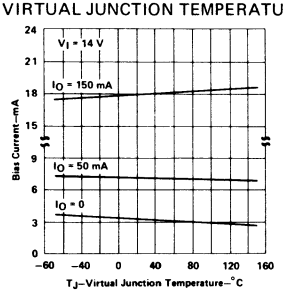


FIGURE 17

BIAS CURRENT
vs
INPUT VOLTAGE

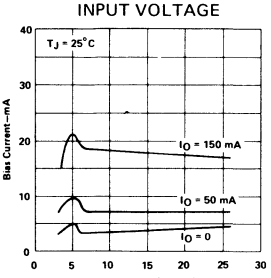
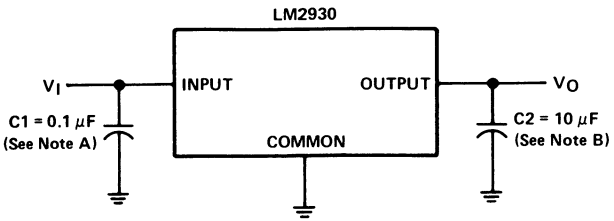


FIGURE 18

TYPICAL APPLICATION DATA



NOTES: A. Use of C1 is required if the regulator is not located in close proximity to the supply filter.
B. Capacitor C2 must be located as close as possible to the regulator and may be an aluminum or tantalum type capacitor. The minimum value required for stability is 10 μF. The capacitor must be rated for operation at −40°C to guarantee stability to that extreme.

FIGURE 19

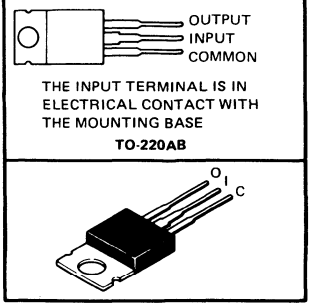
TYPE SERIES LM320
3-TERMINAL NEGATIVE-VOLTAGE REGULATORS

D2334, APRIL 1983

- 3-Terminal Regulators
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Easily Adjustable to Higher Output Voltage
- Interchangeable with National Semiconductor LM320 Series

NOMINAL OUTPUT VOLTAGE	MAXIMUM OUTPUT CURRENT	REGULATOR
−5 V	1.5 A	LM320-5
−12 V	1 A	LM320-12
−15 V	1A	LM320-15

KC PACKAGE
(TOP VIEW)

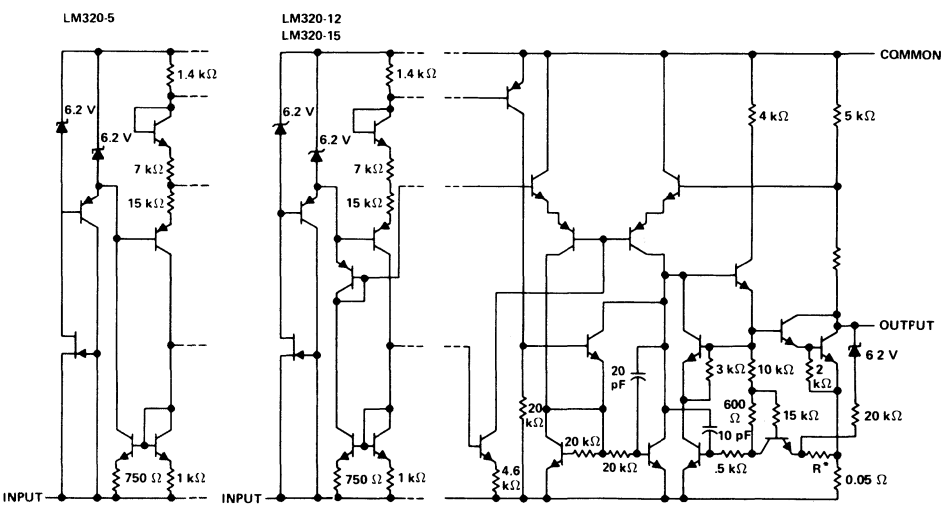


description

The LM320 series of three-terminal, fixed-negative-voltage monolithic integrated circuit voltage regulators are designed to provide a fixed output voltage of −5 volts, −12 volts, and −15 volts with up to 1.5 amperes of output current. Each is designed for a wide range of applications which includes on-card regulation for elimination of noise and distribution problems associated with single-point regulation.

The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. The LM320, when used as a fixed-voltage regulator, needs only one external component: a compensation capacitor at the output terminal. In addition, these devices can be used with external components to obtain adjustable output voltages and currents or as the power-pass element in precision regulators.

schematic diagram



For LM320-5, R* = 50 Ω. For LM320-12 and LM320-15, R* = 150 Ω
All component values are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Input voltage:	LM320-5	−25 V
	LM320-12	−35 V
	LM320-15	−35 V
Input-output voltage differential		25 V
Continuous total dissipation at 25°C free-air temperature (see Note 1)		2 W
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)		15 W
Operating free-air, case, or virtual junction temperature range		0°C to 150°C
Storage temperature range		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

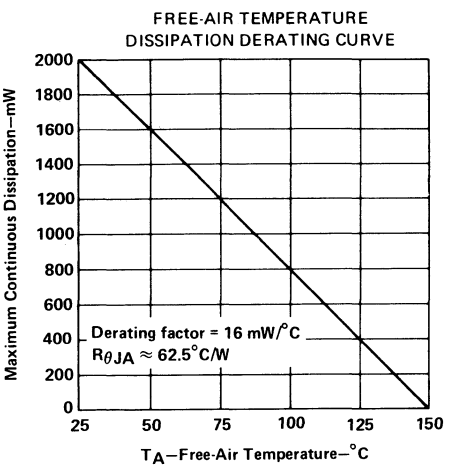


FIGURE 1

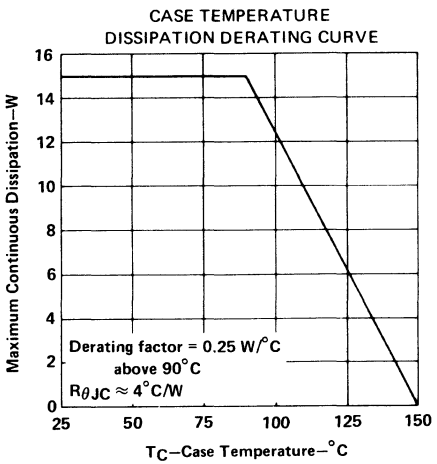


FIGURE 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	LM320-5	−7.5	−25	V
	LM320-12	−14.5	−32	
	LM320-15	−17.5	−35	
Output current, I_O	LM320-5		1.5	A
	LM320-12		1	
	LM320-15		1	
Operating virtual junction temperature, T_J		0	125	°C

LM320-5 electrical characteristics at specified virtual junction temperature, I_O = 5 mA, V_I = −10 V, (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage		T_J = 25°C	−4.8		−5.2	V
	V_I = −7.5 V to −25 V, $P \leq 15$ W,	I_O = 5 mA to 1.5 A, T_J = 0°C to 125°C	−4.75		−5.25	
Input regulation	V_I = −7.5 V to −25 V,	T_J = 25°C		10	40	mV
Ripple rejection	f = 120 Hz,	T_J = 0°C to 125°C	54	64		dB
Output regulation	I_O = 5 mA to 1.5 A,	T_J = 25°C		50	100	mV
Output noise voltage	C_L = 1 μF, f = 10 Hz to 100 kHz,	T_J = 25°C		150		μV
Output voltage long-term drift (see Note 2)	After 1000 h at T_J = 125°,	T_J = 25°C		10		mV
Bias current	V_I = −7.5 V to −25 V,	T_J = 0°C to 125°C		1	2	mA
Bias current change	V_I = −7.5 V to −25 V	T_J = 25°C		0.1	0.4	mA
	I_O = 5 mA to 1.5 A			0.1	0.4	

LM320-12 electrical characteristics at specified virtual junction temperature, I_O = 5 mA, V_I = −17 V, (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage		T_J = 25°C	−11.6	−12	−12.4	V
	V_I = −14.5 V to −32 V, $P \leq 15$ W,	I_O = 5 mA to 1 A, T_J = 0°C to 125°C	−11.4		−12.6	
Input regulation	V_I = −14.5 V to −32 V,	T_J = 25°C		4	20	mV
Ripple rejection	f = 120 Hz,	T_J = 0°C to 125°C	56	80		dB
Output regulation	I_O = 5 mA to 1 A,	T_J = 25°C		30	80	mV
Output noise voltage	C_L = 1 μF, f = 10 Hz to 100 kHz,	T_J = 25°C		400		μV
Output voltage long-term drift (see Note 2)	After 1000 h at T_J = 125°C,	T_J = 25°C		24		mV
Bias current	V_I = −14.5 V to −32 V,	T_J = 0°C to 125°C		2	4	mA
Bias current change	V_I = −14.5 V to −32 V	T_J = 25°C		0.1	0.4	mA
	I_O = 5 mA to 1 A			0.1	0.4	

LM320-15 electrical characteristics at specified virtual junction temperature, I_O = 5 mA, V_I = −20 V, (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage		T_J = 25°C	−14.5	−15	−15.5	V
	V_I = −17.5 V to −35 V, $P \leq 15$ W,	I_O = 5 mA to 1 A, T_J = 0°C to 125°C	−14.3		−15.7	
Input regulation	V_I = −17.5 V to −35 V,	T_J = 25°C		5	20	mV
Ripple rejection	f = 120 Hz,	T_J = 0°C to 125°C	56	80		dB
Output regulation	I_O = 5 mA to 1 A	T_J = 25°C		30	80	mV
Output noise voltage	C_L = 1 μF, f = 10 Hz to 100 kHz,	T_J = 25°C		400		μV
Output voltage long-term drift (see Note 2)	After 1000 h at T_J = 125°C,	T_J = 25°C		30		mV
Bias current	V_I = −17.5 V to −35 V,	T_J = 0°C to 125°C		2	4	mA
Bias current change	V_I = −17.5 V to −35 V,	T_J = 25°C		0.1	0.4	mA
	I_O = 5 mA to 1 A			0.1	0.4	

†All characteristics are measured with a 1-μF capacitor across the input and a 2-μF solid-tantalum capacitor across the output. All characteristics except ripple rejection and output noise voltage are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

NOTE 2: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

TYPICAL CHARACTERISTICS

NORMALIZED OUTPUT VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

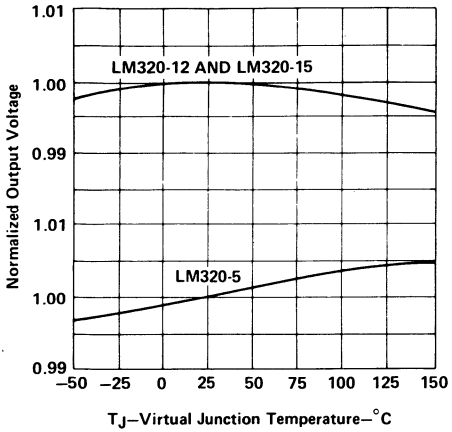


FIGURE 3

RIPPLE REJECTION
vs
FREQUENCY

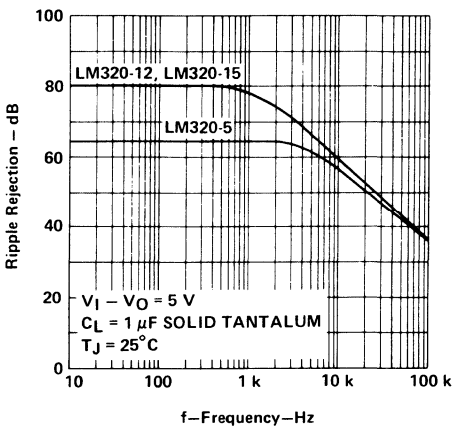


FIGURE 4

BIAS CURRENT
vs
INPUT VOLTAGE

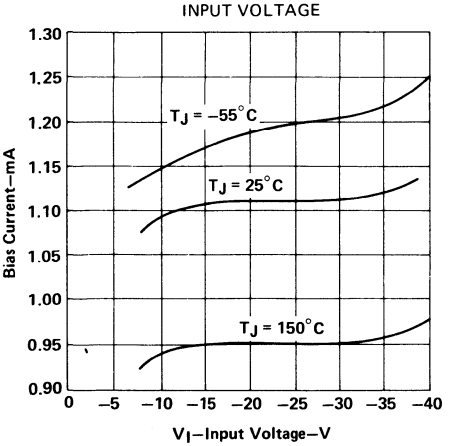


FIGURE 5

BIAS CURRENT
vs
OUTPUT CURRENT

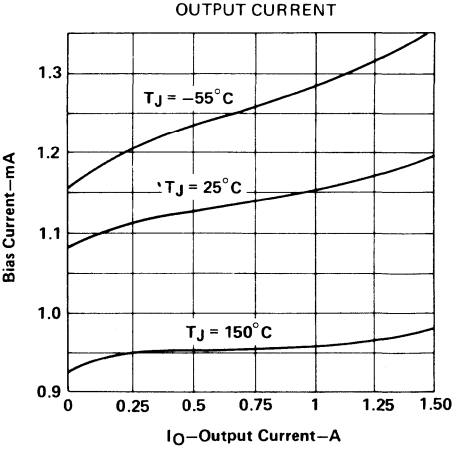


FIGURE 6

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT
vs
INPUT-OUTPUT VOLTAGE DIFFERENTIAL

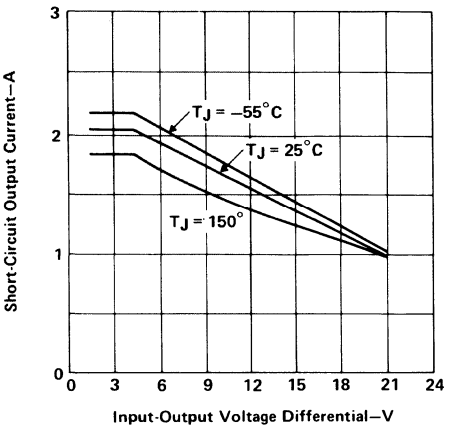


FIGURE 7

DROPOUT VOLTAGE
vs
OUTPUT CURRENT

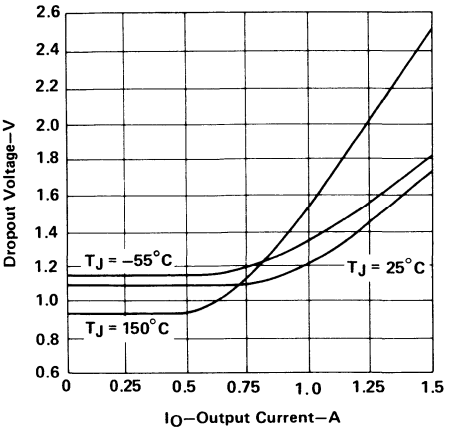


FIGURE 8

OUTPUT IMPEDANCE
vs
FREQUENCY

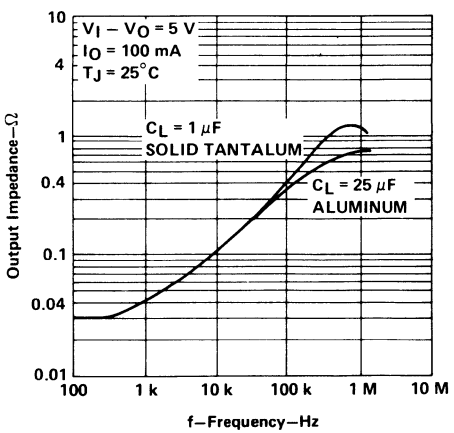


FIGURE 9

TYPICAL APPLICATION INFORMATION

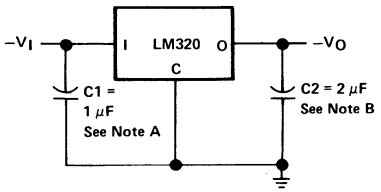


FIGURE 10 — FIXED-VOLTAGE REGULATOR

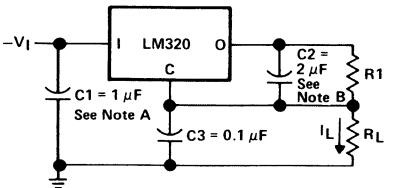


FIGURE 11 — CURRENT SOURCE REGULATOR

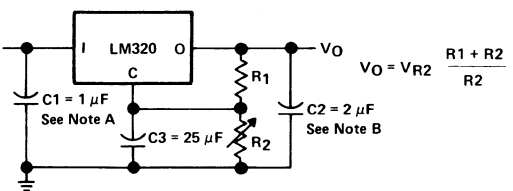


FIGURE 12 — ADJUSTABLE OUTPUT REGULATOR

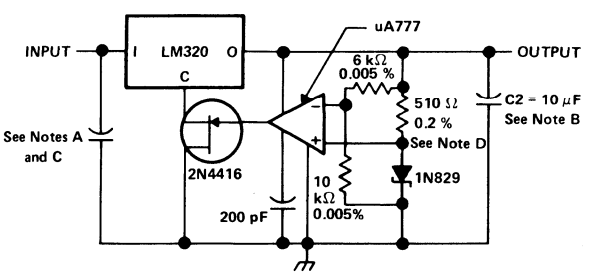


FIGURE 13 — HIGH-STABILITY REGULATOR

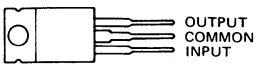
NOTES: A. Capacitor C1 is required if the regulator is not located within 75 mm (3 inches) of the power supply filter.
B. Capacitor C2 is required for stability. For the value given, the capacitor must be solid tantalum but a 25-μF aluminum electrolytic may be substituted. Values given may be increased without limit.
C. In Figure 13 capacitor C1 is solid tantalum.
D. This resistor determines zener current. Adjust to minimize thermal drift.

TYPE LM330
3-TERMINAL POSITIVE REGULATOR

D2700, APRIL 1983

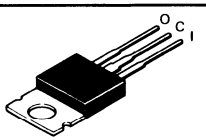
- Input-Output Differential Less than 0.6 V
- Output Current of 150 mA
- Reverse Polarity Protection
- Line Transient Protection
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- Mirror-Image Insertion Protection
- Direct Replacement for National LM330T-5.0

KC PACKAGE
(TOP VIEW)



THE COMMON TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

TO-220AB



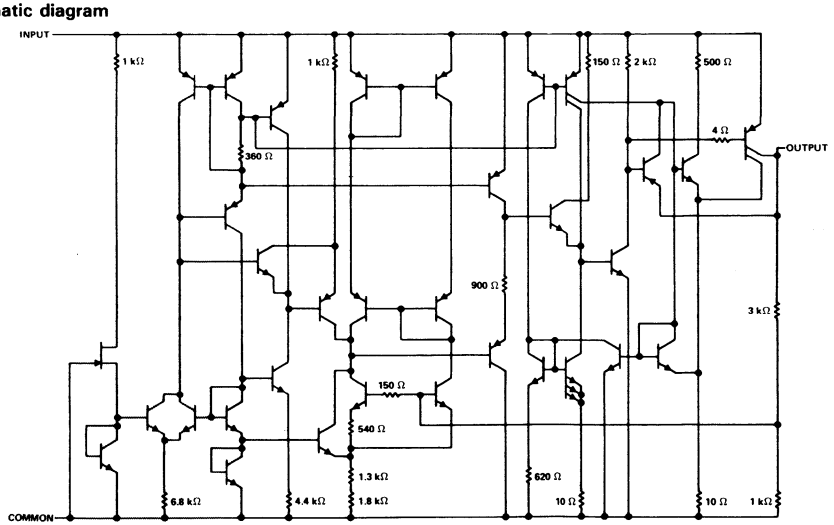
description

The LM330 3-terminal positive regulator features an ability to source 150 milliamperes of output current with an input-output differential of 0.6 volt or less. Familar regulator features such as current limit and thermal overload protection are also provided.

The LM330 has low dropout voltage making it useful for certain battery applications. For example, since the low dropout voltage allows a longer battery discharge before the output falls out of regulation, a battery supplying the regulator input voltage may discharge to 5.6 volts and still properly regulate the system and load voltage. The LM330 protects both itself and the regulated system from reverse installation of batteries.

Other protection features include line transient protection above 40 volts, where the output actually shuts down to avoid damaging internal and external circuits. The LM330 regulator cannot be harmed by temporary mirror-image insertion.

schematic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Continuous input voltage	26 V
Transient input voltage t = 1 s	50 V
t = 100 ms	60 V
Continuous total dissipation at 25°C free-air temperature (see Note 1)	2 W
Continuous total dissipation at (or below) case temperature (see Note 1)	20 W
Operating free-air, case, or virtual junction temperature	0°C to 150°C
Storage temperature	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

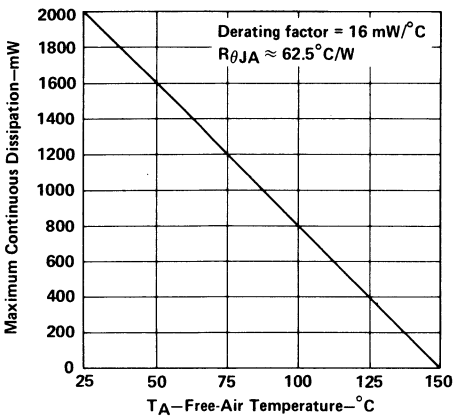


FIGURE 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

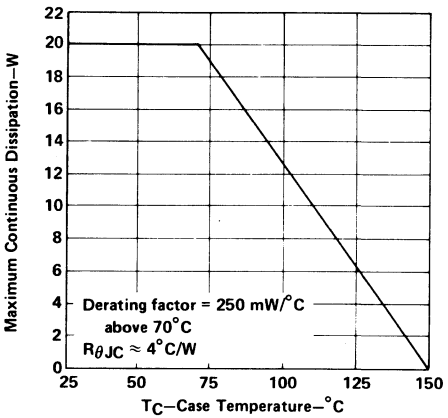


FIGURE 2

recommended operating conditions

		MIN	MAX	UNIT
I_O	Output current	5	150	mA
T_A	Operating virtual junction temperature	0	100	°C

electrical characteristics at 25°C virtual junction temperature, V_I = 14 V, I_O = 150 mA, (unless otherwise noted)

PARAMETERS	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 6 V to 26 V,	I_O = 5 mA to 150 mA,	4.8	5	5.2	V
	T_J = 0°C to 100°C		4.75		5.25	
Input regulation	I_O = 5 mA	V_I = 9 V to 16 V		7	25	mV
		V_I = 6 V to 26 V		30	60	
Ripple rejection	f = 120 Hz			56		dB
Output regulation	I_O = 5 mA to 150 mA			14	50	mV
Output voltage long-term drift‡	After 1000 h at T_J = 100°C			20		mV
Dropout voltage	I_O = 150 mA			0.32	0.6	V
Output noise voltage	f = 10 Hz to 100 kHz			50		μV
Output voltage with input polarity reversed	R_L = 100 Ω	V_I = −30 V, t = 100 ms		> −0.3		V
		V_I = −12 V, DC		> −0.3		
Output voltage with input transient	V_I = 60 V,	t = 100 ms		< 5.5		V
	V_I = 50 V,	t = 1 s		< 5.5		
Bias current with input transient	R_L = 100 Ω	V_I = 40 V, t = 1 s		14		mA
		V_I = −6 V, t = 1 s		−80		
Overvoltage shutdown voltage			26	45		V
Output impedance	I_O = 100 mA, I_o = 10 mA (rms), f = 100 Hz to 10 kHz			200		mΩ
Bias current	I_O = 10 mA			3.5	7	mA
	I_O = 50 mA			5	11	
	I_O = 150 mA			18	40	
Bias current change	V_I = 6 V to 26 V			10		%
Peak output current			150	420	700	mA

†Unless otherwise specified, all characteristics except ripple rejection and noise voltage measurements are measured using pulse techniques ($t_w \leq$ 10 ms, duty cycle ≤ 5%) with a capacitor of 0.1 μF across the input and a capacitor of 10 μF across the output. Output voltage changes due to changes in internal temperature must be taken into account separately.

‡Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

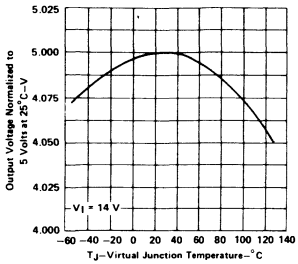


FIGURE 3

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

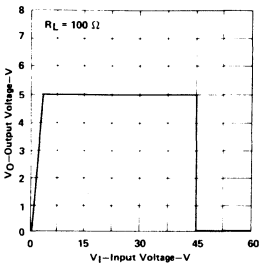


FIGURE 4

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

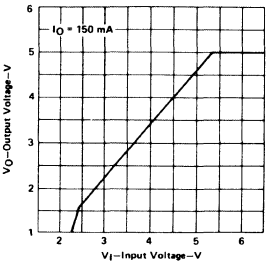


FIGURE 5

PEAK OUTPUT CURRENT
vs
INPUT VOLTAGE

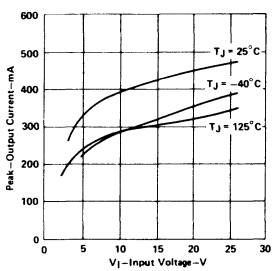


FIGURE 6

RIPPLE REJECTION
vs
FREQUENCY

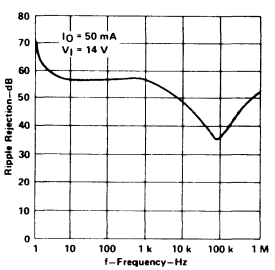


FIGURE 7

RIPPLE REJECTION
vs
OUTPUT CURRENT

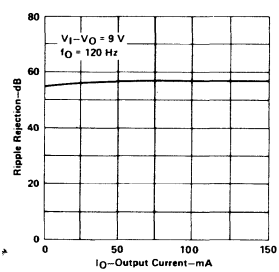


FIGURE 8

DROPOUT VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

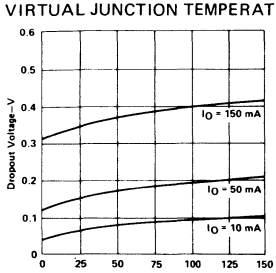


FIGURE 9

DROPOUT VOLTAGE
vs
OUTPUT CURRENT

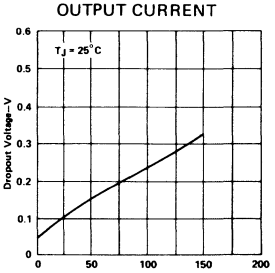


FIGURE 10

OUTPUT IMPEDANCE
vs
FREQUENCY

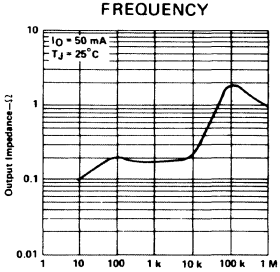


FIGURE 11

TYPICAL CHARACTERISTICS

INPUT CURRENT
vs
INPUT VOLTAGE

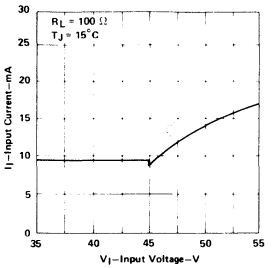


FIGURE 12

LINE TRANSIENT RESPONSE

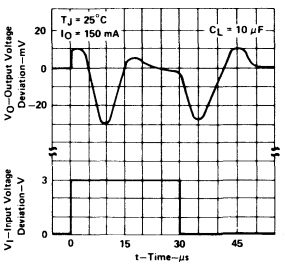


FIGURE 13

INPUT CURRENT
vs
REVERSE INPUT VOLTAGE

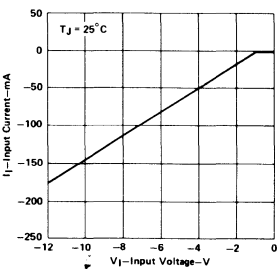


FIGURE 14

OUTPUT VOLTAGE
vs
REVERSE INPUT VOLTAGE

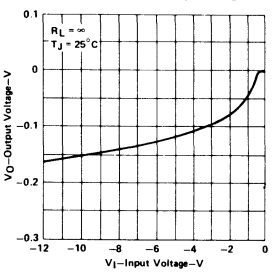


FIGURE 15

LOAD TRANSIENT RESPONSE

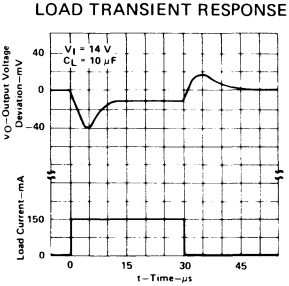


FIGURE 16

BIAS CURRENT
vs
OUTPUT CURRENT

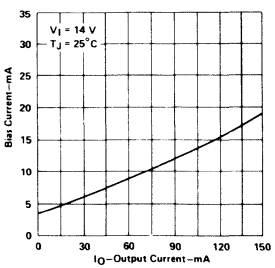


FIGURE 17

BIAS CURRENT
vs
VIRTUAL JUNCTION TEMPERATURE

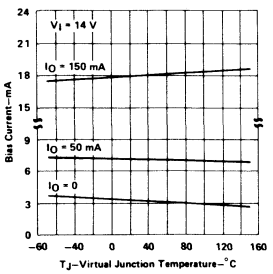


FIGURE 18

BIAS CURRENT
vs
INPUT VOLTAGE

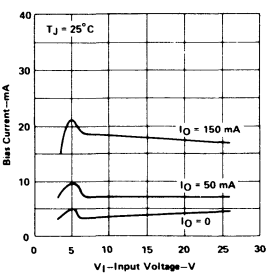
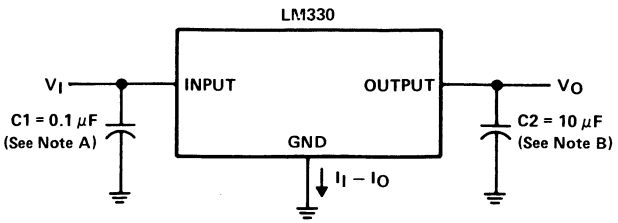


FIGURE 19

TYPICAL APPLICATION DATA



NOTES: A. Use of C1 is required if the regulator is not located in close proximity to the supply filter.
B. Capacitor C2 must be located as close as possible to the regulator and may be an aluminum or tantalum type capacitor. The minimum capacitance that will provide stability is 10 μF. The capacitor must be rated for operation at −40°C to guarantee stability to that extreme.

FIGURE 20

SERIES LM340
POSITIVE-VOLTAGE REGULATORS

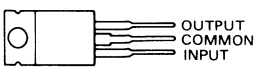
D2332, SEPTEMBER 1977 – REVISED MARCH 1983

- 3-Terminal Regulators
- Output Current up to 1.5 A
- No External Components
- Internal Thermal Overload
- High Power Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Output Load Regulation . . . 0.3% Typ
- Direct Replacements for National LM340 Series

NOMINAL OUTPUT VOLTAGE	REGULATOR
5 V	LM340-5
12 V	LM340-12
15 V	LM340-15

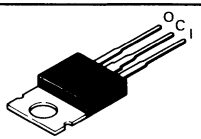
KC PACKAGE

(TOP VIEW)



THE COMMON TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

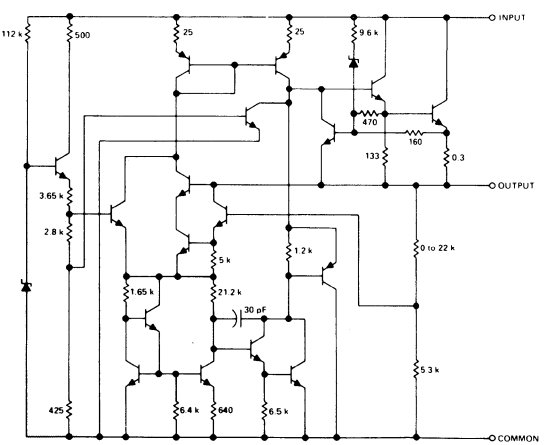
TO-220AB



description

This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Any of these regulators can deliver up to 1.5 amperes of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power-pass element in precision regulators.

schematic



Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Input voltage	35 V
Continuous total dissipation at 25°C free-air temperature (see Note 1)	2 W
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)	15 W
Operating free-air, case, or virtual junction temperature range	0°C to 150°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

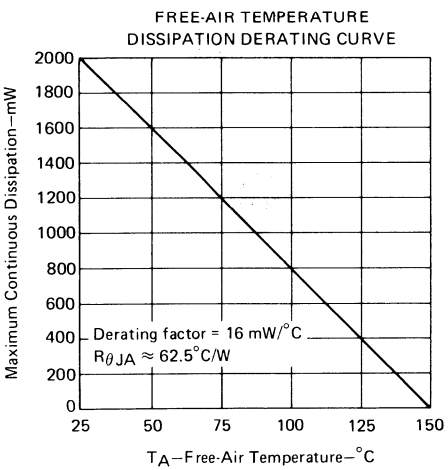


FIGURE 1

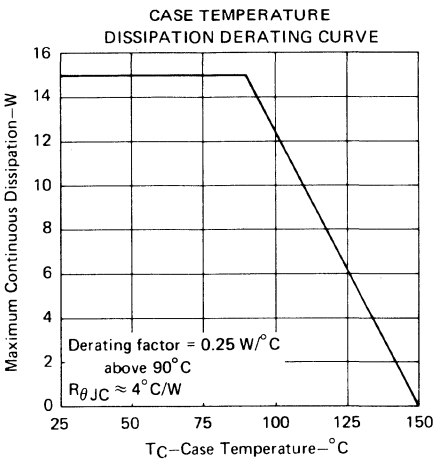


FIGURE 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	LM340-5	7	25	V
	LM340-12	14.5	30	
	LM340-15	17.5	30	
Output current, I_O			1.5	A
Operating virtual junction temperature, T_J		0	125	°C

LM340-5 electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 1 A (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
Output voltage	I_O = 5 mA to 1 A		25°C	4.8	5	5.2	V
	V_I = 7 V to 20 V, $P \leq 15$ W	I_O = 5 mA to 1 A,	0°C to 125°C	4.75		5.25	
Input regulation	I_O = 500 mA	V_I = 7 V to 25 V	25°C		3	50	mV
		V_I = 8 V to 20 V	0°C to 125°C			50	
	I_O = 1 A	V_I = 7.3 V to 20 V	25°C			50	
		V_I = 8 V to 12 V	0°C to 125°C			25	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	$I_O \leq$ 1 A	25°C	62	80		dB
		$I_O \leq$ 500 mA	0°C to 125°C	62			
Output regulation	I_O = 250 mA to 750 mA		25°C			25	mV
	I_O = 5 mA to 1.5 A				10	50	
	I_O = 5 mA to 1 A		0°C to 125°C			50	
Output noise voltage	f = 10 Hz to 100 kHz		25°C		40		μV
Dropout voltage	I_O = 1 A		25°C		2		V
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−0.6		mV/°C
Output impedance	f = 1 kHz		25°C		8		mΩ
Bias current	$I_O \leq$ 1 A		25°C			8	mA
			0°C to 125°C			8.5	
Bias current change	V_I = 7.5 V to 20 V,	$I_O \leq$ 1 A	25°C			1	mA
	V_I = 7 V to 25 V,	$I_O \leq$ 500 mA	0°C to 125°C			1	
	I_O = 5 mA to 1 A					0.5	
Peak output current			25°C		2.4		A
Short-circuit current			25°C		2.1		A

† All characteristics are measured with a capacitor across the input of 0.22 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage rejection ratio are measured using pulse techniques ($t_w \leq$ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

LM340-12 electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 1 A (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
Output voltage	I_O = 5 mA to 1 A		25°C	11.5	12	12.5	V
	V_I = 14.5 V to 27 V, I_O = 5 mA to 1 A, P ≤ 15 W		0°C to 125°C	11.4		12.6	
Input regulation	I_O = 500 mA	V_I = 14.5 V to 30 V	25°C		4	120	mV
		V_I = 15 V to 27 V	0°C to 125°C			120	
	I_O = 1 A	V_I = 14.6 V to 27 V	25°C			120	
		V_I = 16 V to 22 V	0°C to 125°C			120	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	I_O ≤ 1 A	25°C	55	72		dB
		I_O ≤ 500 mA	0°C to 125°C	55			
Output regulation	I_O = 250 mA to 750 mA		25°C			60	mV
	I_O = 5 mA to 1.5 A				12	120	
	I_O = 5 mA to 1 A		0°C to 125°C			120	
Output noise voltage	f = 10 Hz to 100 kHz		25°C		75		μV
Dropout voltage	I_O = 1 A		25°C		2		V
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1.5		mV/°C
Output impedance	f = 1 kHz		25°C		18		mΩ
Bias current	I_O ≤ 1 A		25°C			8	mA
			0°C to 125°C			8.5	
Bias current change	V_I = 14.8 V to 27 V, I_O ≤ 1 A		25°C			1	mA
	V_I = 14.5 V to 30 V, I_O ≤ 500 mA		0°C to 125°C			1	
	I_O = 5 mA to 1 A					0.5	
Peak output current			25°C		2.4		A
Short-circuit current			25°C		1.5		A

† All characteristics are measured with a capacitor across the input of 0.22 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

LM340-15 electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 1 A (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
Output voltage	I_O = 5 mA to 1 A		25°C	14.4	15	15.6	V
	V_I = 17.5 V to 30 V, P ≤ 15 W	I_O = 5 mA to 1 A,	0°C to 125°C	14.25		15.75	
Input regulation	I_O = 500 mA	V_I = 17.5 V to 30 V	25°C		4	150	mV
		V_I = 18.5 V to 30 V	0°C to 125°C			150	
	I_O = 1 A	V_I = 17.7 V to 30 V	25°C			150	
		V_I = 20 V to 26 V	0°C to 125°C			75	
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz	I_O ≤ 1 A	25°C	54	70		dB
		I_O ≤ 500 mA	0°C to 125°C	54			
Output regulation	I_O = 250 mA to 750 mA		25°C			75	mV
	I_O = 5 mA to 1.5 A				12	150	
	I_O = 5 mA to 1 A		0°C to 125°C			150	
Output noise voltage	f = 10 Hz to 100 kHz		25°C		90		μV
Dropout voltage	I_O = 1 A		25°C		2		V
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1.8		mV/°C
Output impedance	f = 1 kHz		25°C		19		mΩ
Bias current	I_O ≤ 1 A		25°C			8	mA
			0°C to 125°C			8.5	
Bias current change	V_I = 17.9 V to 30 V,	I_O ≤ 1 A	25°C			1	mA
	V_I = 17.5 V to 30 V,	I_O ≤ 500 mA	0°C to 125°C			1	
	I_O = 5 mA to 1 A					0.5	
Peak output current			25°C		2.4		A
Short-circuit current			25°C		1.2		A

† All characteristics are measured with a capacitor across the input of 0.22 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

TYPICAL CHARACTERISTICS

NORMALIZED OUTPUT VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

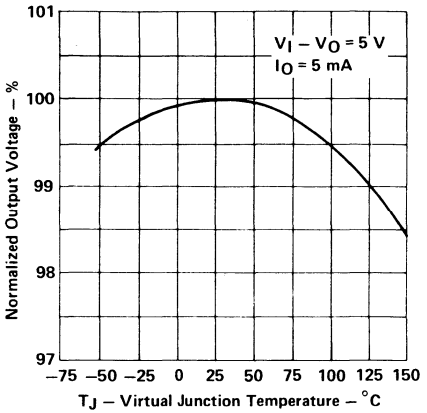


FIGURE 3

RIPPLE REJECTION
vs
FREQUENCY

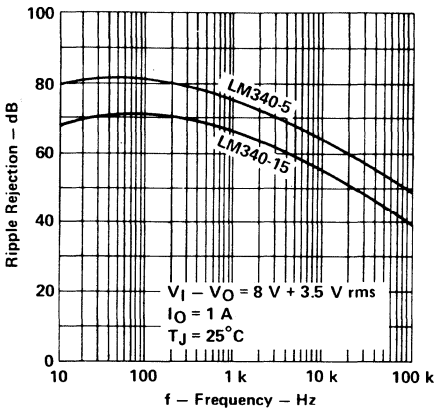


FIGURE 4

DROPOUT VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

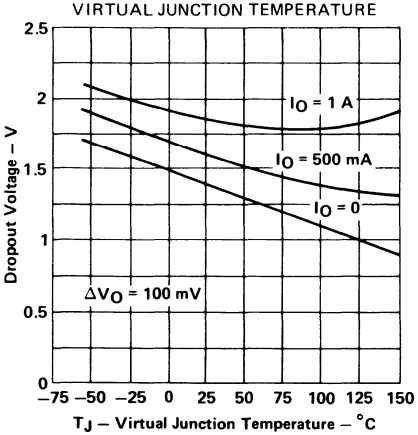


FIGURE 5

LM340-5
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

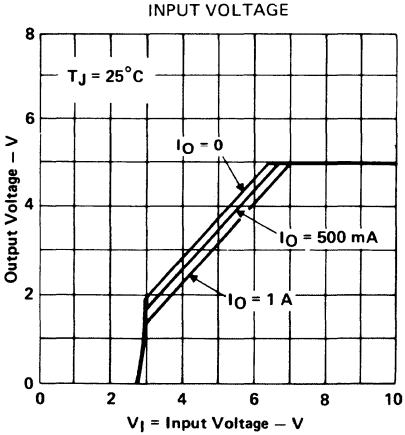


FIGURE 6

TYPICAL CHARACTERISTICS

LM340-5
BIAS CURRENT
vs
VIRTUAL JUNCTION TEMPERATURE

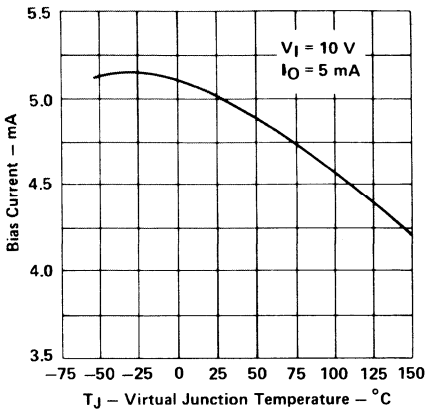


FIGURE 7

LM340-5
BIAS CURRENT
vs
INPUT VOLTAGE

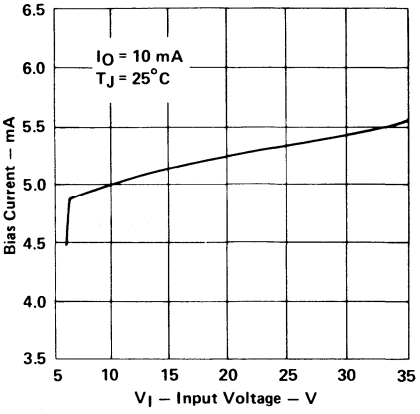


FIGURE 8

LM340-5
OUTPUT IMPEDANCE
vs
FREQUENCY

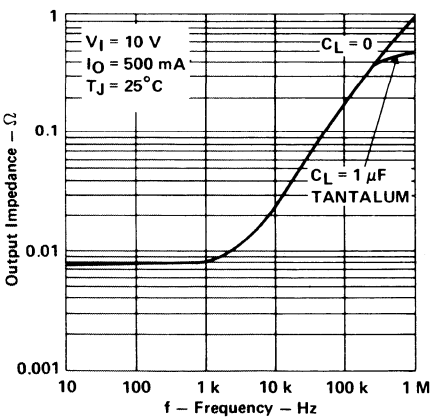


FIGURE 9

PEAK OUTPUT CURRENT
vs
INPUT-TO-OUTPUT VOLTAGE DIFFERENTIAL

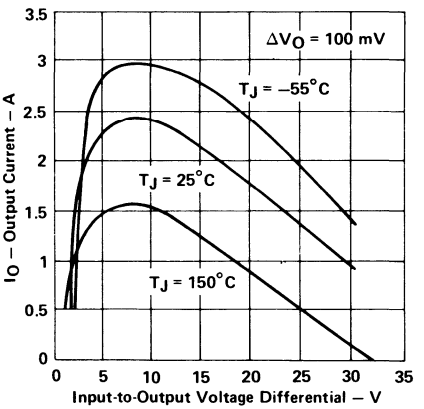


FIGURE 10

TYPICAL APPLICATION DATA

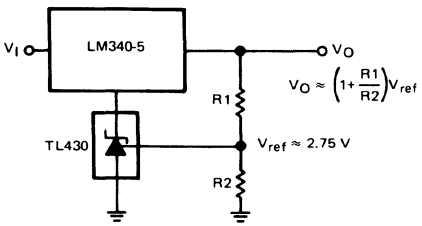
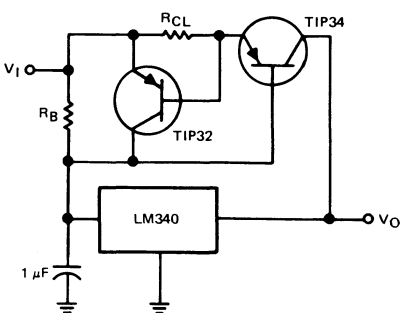


FIGURE 11–ADJUSTABLE SUPPLY WITH STABLE OUTPUT FROM 8 VOLTS TO 35 VOLTS



The boost circuit takes over at a level determined by R_B.

$$R_B \approx \frac{0.6\text{ V}}{I_B}$$

where I_B is the LM340 operating level.

Maximum current limit I_{CL} is determined by R_{CL}.

$$R_{CL} \approx \frac{0.6\text{ V}}{I_{CL}}$$

Example: If I_B is selected to be 0.5 A, then $R_B = 1.2\ \Omega$. If I_{CL} is 3 A, then $R_{CL} = 0.2\ \Omega$.

FIGURE 12–OUTPUT CURRENT BOOST CIRCUIT

MAY 1988

FEATURES

- ± 4mV initial accuracy LT1004-1.2
- ± 20mV accuracy LT1004-2.5
- 10μA operating current
- Temperature performance
- Operates up to 20mA
- Very low dynamic impedance

APPLICATIONS

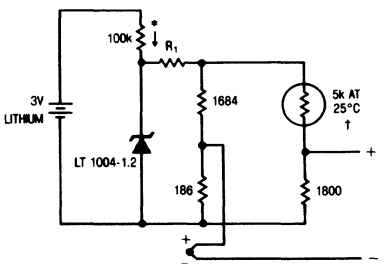
- Portable meter references
- Portable test instruments
- Battery operated systems
- Current loop instrumentation

DESCRIPTION

The LT1004 Micropower Voltage References are two terminal bandgap reference diodes designed to provide high accuracy and excellent temperature characteristics at very low operating currents. Optimization of the key parameters in the design, processing and testing of the device results in accuracy specifications previously attainable only with selected units. Below is a distribution plot of reference voltage for a typical lot of LT1004-1.2. Virtually all of the units fall well within the prescribed limits of ±4mV.

The LT1004 is a pin for pin replacement for the LM185/385 series of references with improved accuracy specifications. More important, the LT1004 is an attractive device for use in systems where accuracy was previously obtained at the expense of power consumption and trimming.

Micropower Cold Junction Compensation For Thermocouples



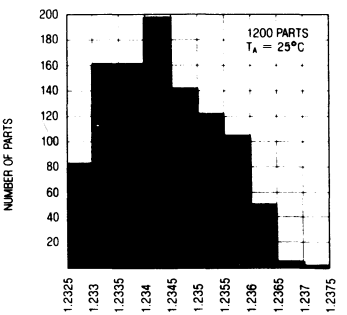
THERMOCOUPLE TYPE	R_1
J	233k
K	299k
T	300k
S	2.1M

* QUIESCENT CURRENT ≃ 15μA

† YELLOW SPRINGS INST. CO. PART #44007

COMPENSATES WITHIN ±1°C FROM 0°C TO 60°C

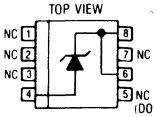
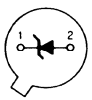
Typical Distribution of Reference Voltage (LT1004-1.2)



ABSOLUTE MAXIMUM RATINGS

Reverse Breakdown Current..... 30mA
Forward Current..... 10mA
Operating Temperature Range
LT1004M ..... −55°C to 125°C
LT1004C ..... 0°C to 70°C
Storage Temperature Range
LT1004M ..... −65°C to 150°C
LT1004C ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
TOP VIEW  D PACKAGE PLASTIC SO	LT1004CD
	PART MARKING
	0412 (1.2V VERSION) 0425 (2.5V VERSION)
BOTTOM VIEW  LD PACKAGE TO-46 METAL CAN	LT1004MLD-2.5 LT1004CLD-1.2 LT1004CLD-2.5
BOTTOM VIEW  LP PACKAGE TO-92 PLASTIC	LT1004CLP-1.2 LT1004CLP-2.5

The D packages are available taped and reeled. Add the suffix R to the device type when ordering taped parts. (ie. LT1004CDR)

ELECTRICAL CHARACTERISTICS (See Note 1)

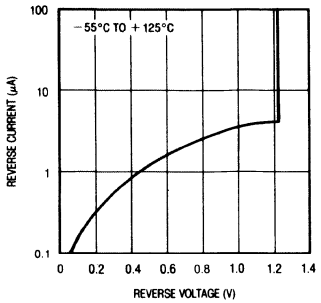
SYMBOL	PARAMETER	CONDITIONS		LT1004-1.2 MIN	LT1004-1.2 TYP	LT1004-1.2 MAX	LT1004-2.5 MIN	LT1004-2.5 TYP	LT1004-2.5 MAX	UNITS
V_Z	Reverse Breakdown Voltage	$I_R = 100\mu A$		1.231	1.235	1.239	2.480	2.500	2.520	V
		LT1004M $-55°C \leq T_A \leq 125°C$	●	1.220	1.230	1.245	2.460	2.500	2.535	V
		LT1004M/C $0°C \leq T_A \leq 70°C$	●	1.225	1.235	1.245	2.470	2.500	2.530	V
$\frac{\Delta V_Z}{\Delta \text{Temp}}$	Average Temperature Coefficient	$I_{min} \leq I_R \leq 20mA$			20			20		ppm/°C
I_{min}	Minimum Operating Current		●		8	10		12	20	μA
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Voltage Change with Current	$I_{min} \leq I_R \leq 1mA$				1			1	mV
			●			1.5			1.5	mV
		$1mA \leq I_R \leq 20mA$				10			10	mV
			●			20			20	mV
r_Z	Reverse Dynamic Impedance	$I_R = 100\mu A$			0.2	0.6		0.2	0.6	Ω
			●			1.5			1.5	Ω
e_n	Wide Band Noise (RMS)	$I_R = 100\mu A$ $10Hz \leq f \leq 10kHz$			60			120		μV
$\frac{\Delta V_Z}{\Delta \text{Time}}$	Long Term Stability	$I_R = 100\mu A$ $T_A = 25°C \pm 0.1°C$			20			20		ppm/kHr

The ● denotes the specifications which apply over the full operating temperature range.

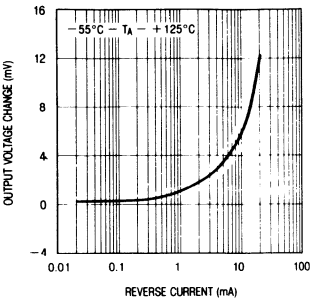
Note 1: All specifications are for $T_A = 25°C$ unless otherwise noted.

TYPICAL PERFORMANCE CHARACTERISTICS 1.2 VOLT

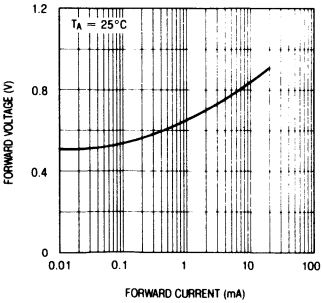
Reverse Characteristics



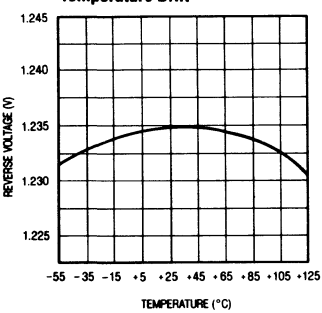
Reverse Voltage Change



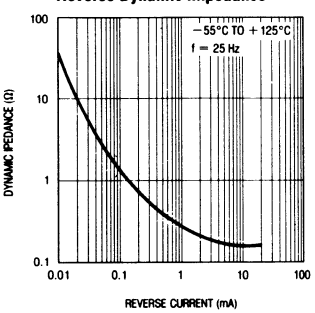
Forward Characteristics



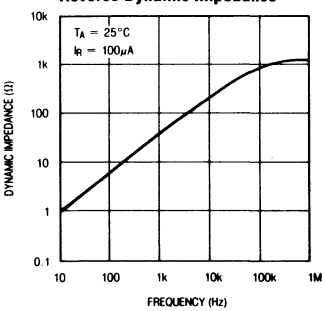
Temperature Drift



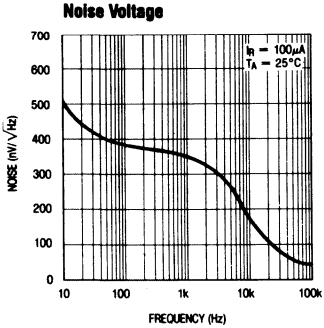
Reverse Dynamic Impedance



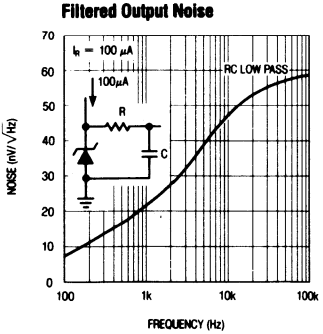
Reverse Dynamic Impedance



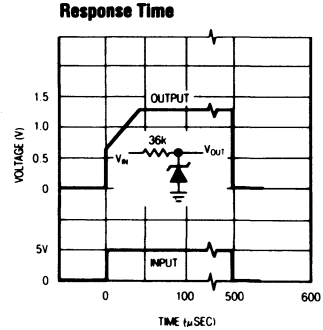
Noise Voltage



Filtered Output Noise

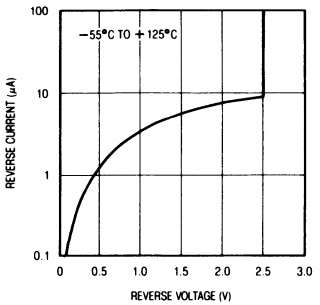


Response Time

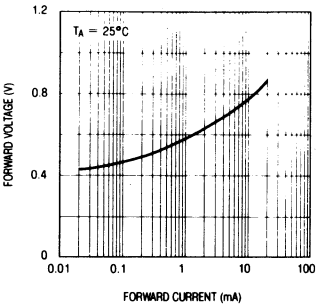


TYPICAL PERFORMANCE CHARACTERISTICS 2.5 VOLT

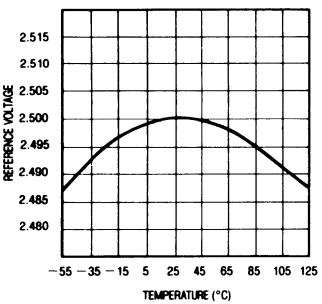
Reverse Characteristics



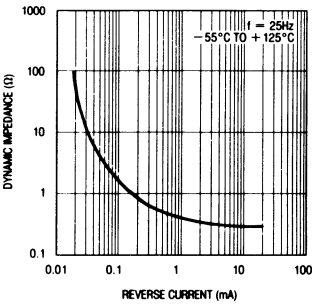
Forward Characteristics



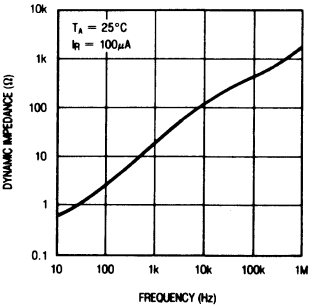
Temperature Drift



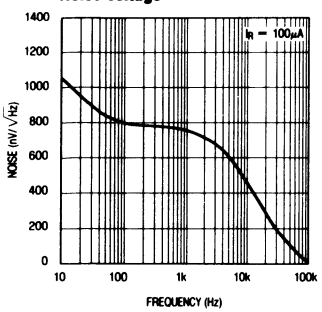
Reverse Dynamic Impedance



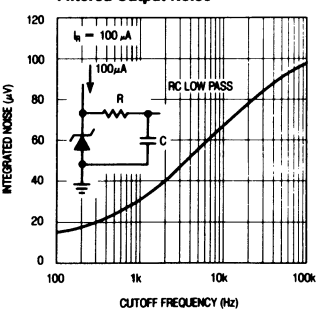
Reverse Dynamic Impedance



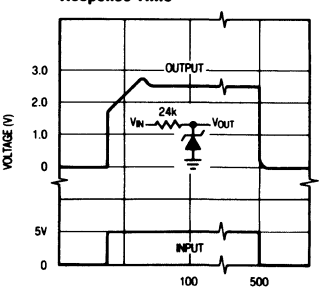
Noise Voltage



Filtered Output Noise

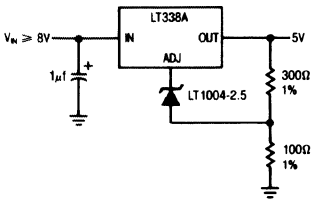


Response Time

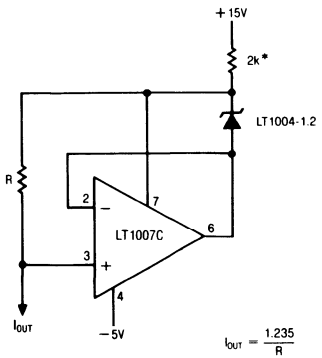


TYPICAL APPLICATIONS

High Stability 5V Regulator



Ground Referenced Current Source

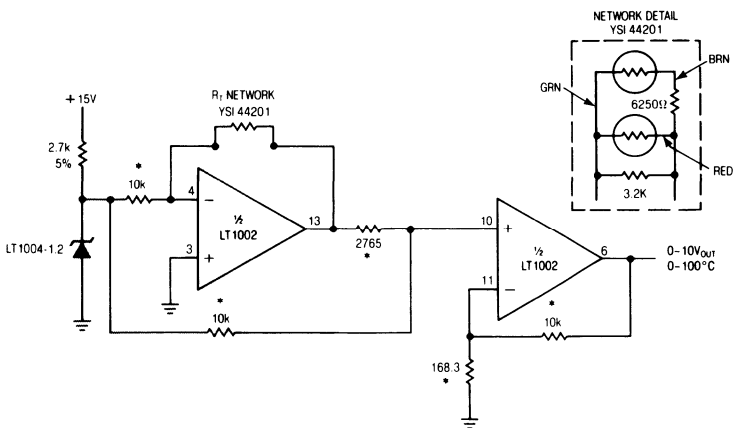


$I_{OUT} = \frac{1.235}{R}$

* MAY BE INCREASED FOR SMALL OUTPUT CURRENTS

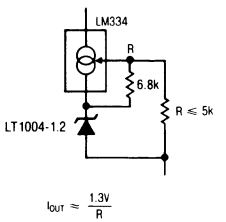
$R \approx \frac{2V}{I_{OUT} + 10\mu A}$

0-100°C Linear Output Thermometer

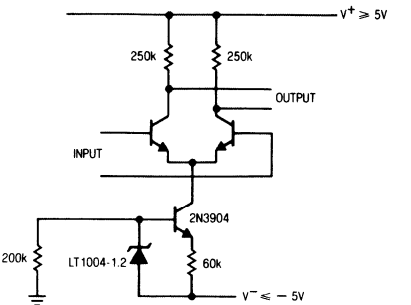


TYPICAL APPLICATIONS

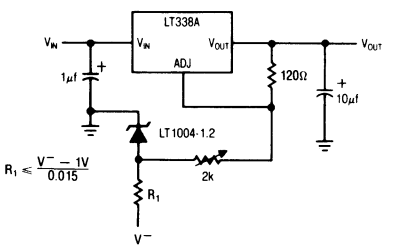
Low Temperature Coefficient 2 Terminal Current Source



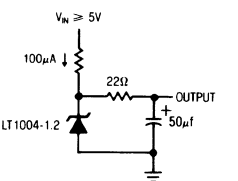
Constant Gain Amplifier Over Temperature



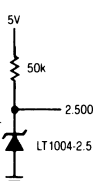
Variable Output Supply



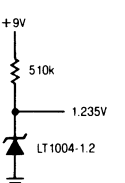
Low Noise Reference



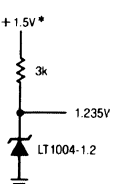
2.5V Reference



Micropower Reference from 9V Battery



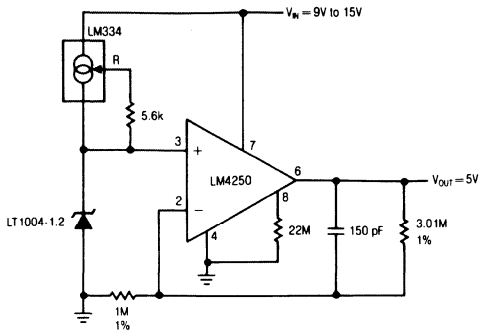
1.2V Reference from 1.5V Battery



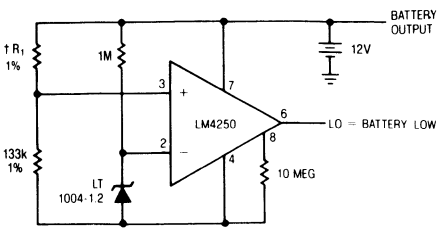
* OUTPUT REGULATES DOWN TO 1.285V FOR I_{OUT} = 0

TYPICAL APPLICATIONS

Micropower 5V Reference

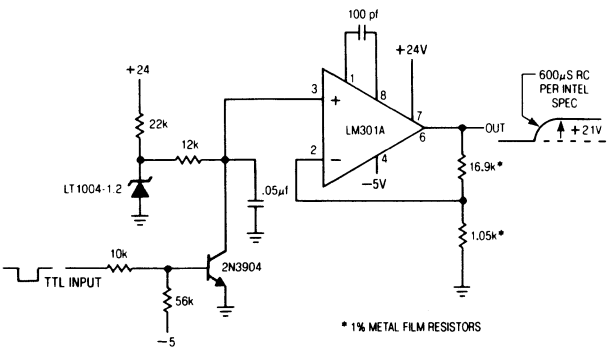


Lead Acid Low Battery Detector



†R_1 SETS TRIP POINT, 60.4k
PER CELL FOR 1.8V/CELL

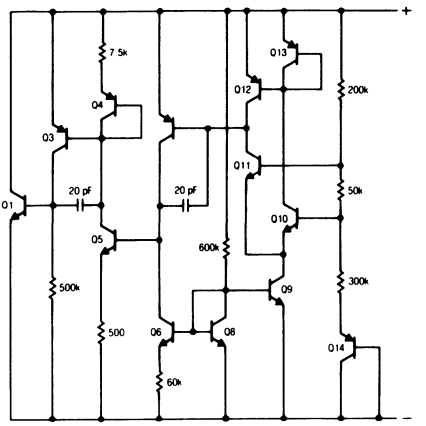
V_{pp} Generator for Eproms — No Trim Required



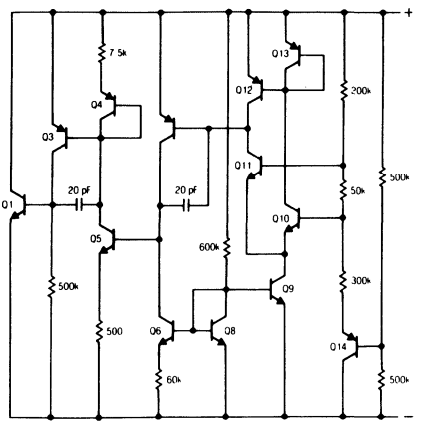
* 1% METAL FILM RESISTORS

SCHEMATIC DIAGRAM

LT1004-1.2



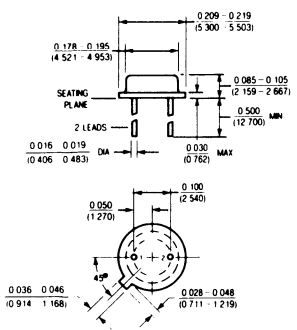
LT1004-2.5



PACKAGE DESCRIPTION

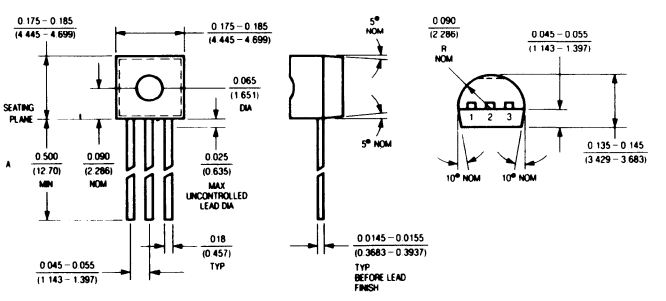
Dimensions in inches (millimeters) unless otherwise noted.

LD Package, 2 Lead TO-46 Metal Can



$T_j$max	θ_{ja}	θ_{jc}
150°C	440°C/W	80°C/W

LP Package, 3 Lead TO-92 Plastic

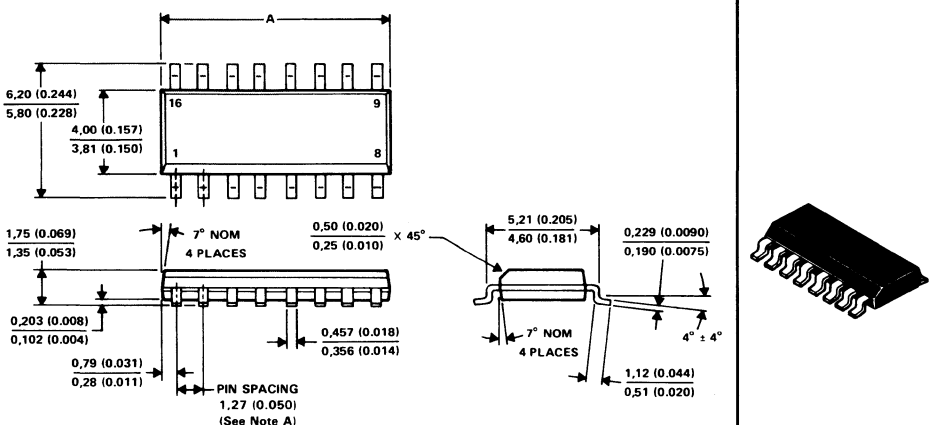


$T_j$max	θ_{ja}
100°C	160°C/W

D008, D014, and D016 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008, D014, and D016
(16-pin package used for illustration)



DIM \ PINS	8	14	16
A MIN	4,80	8,55	9,80
	(0.189)	(0.337)	(0.386)
A MAX	5,00	8,74	10,00
	(0.197)	(0.344)	(0.394)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

MAY 1987

FEATURES

- 0.2% Initial Tolerance Max
- Excellent Temperature Stability
- Maximum 0.6Ω Dynamic Impedance
- Wide Operating Current Range
- Directly Interchangeable with LM136 for Improved Performance
- No Adjustments Needed for Minimum Temperature Coefficient

APPLICATIONS

- Reference for 5V Systems
- 8 Bit A/D and D/A Reference
- Digital Voltmeters
- Current Loop Measurement and Control Systems
- Power Supply Monitor

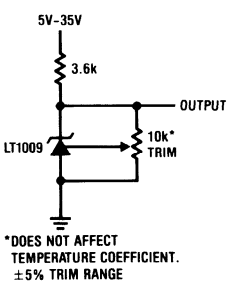
DESCRIPTION

The LT1009 is a precision trimmed 2.500 Volt shunt regulator diode featuring a maximum initial tolerance of only ±5mV. The low dynamic impedance and wide operating current range enhances its versatility. The 0.2% reference tolerance is achieved by on-chip trimming which not only minimizes the initial voltage tolerance but also minimizes the temperature drift.

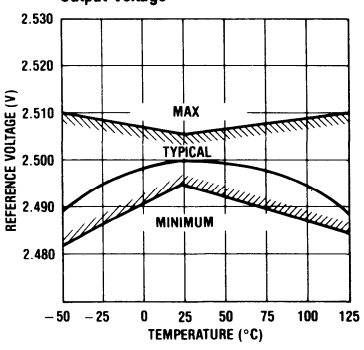
Even though no adjustments are needed with the LT1009, a third terminal allows the reference voltage to be adjusted ±5% to calibrate out system errors. In many applications, the LT1009 can be used as a pin-to-pin replacement of the LM136H-2.5 and the external trim network eliminated.

For a lower drift 2.5V reference, see the LT1019 data sheet.

2.5 Volt Reference



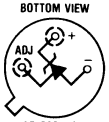
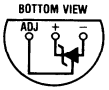
Output Voltage



ABSOLUTE MAXIMUM RATINGS

Reverse Current 20mA
Forward Current 10mA
Operating Temperature Range
LT1009M ..... −55°C to 125°C
LT1009C ..... 0°C to 70°C
Storage Temperature Range
LT1009M and C ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
BOTTOM VIEW  LD PACKAGE TO-46 METAL CAN	LT1009MLD LT1009LD
BOTTOM VIEW  LP PACKAGE TO-92 PLASTIC	LT1009CLP

ELECTRICAL CHARACTERISTICS

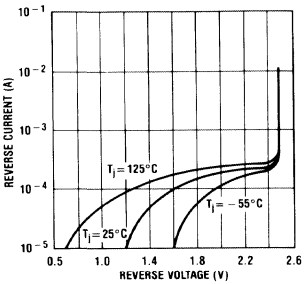
SYMBOL	PARAMETER	CONDITIONS		LT1009M MIN	LT1009M TYP	LT1009M MAX	LT1009C MIN	LT1009C TYP	LT1009C MAX	UNITS
V_Z	Reverse Breakdown Voltage	$T_A = 25°C$, $I_R = 1mA$		2.495	2.500	2.505	2.495	2.500	2.505	V
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Change with Current	$400\mu A \le I_R \le 10mA$			2.6	6		2.6	10	mV
			●		3	10		3	12	mV
r_Z	Reverse Dynamic Impedance	$I_R = 1mA$			0.2	0.6		0.2	1.0	Ω
			●		0.4	1		0.4	1.4	Ω
$\frac{\Delta V_Z}{\Delta Temp}$	Temperature Stability	$T_{MIN} \le T_A \le T_{MAX}$	●			15		1.8	4	mV
	Average Temperature Coefficient	$0°C \le T_A \le 70°C$			15	25		15	25	ppm/°C
		$-55°C \le T_A \le 125°C$ (Note 1)			25	35				ppm/°C
$\frac{\Delta V_Z}{\Delta Time}$	Long Term Stability	$T_A = 25°C \pm 0.1°C$, $I_R = 1mA$			20			20		ppm/kHr

The ● denotes the specifications which apply over full operating temperature range.

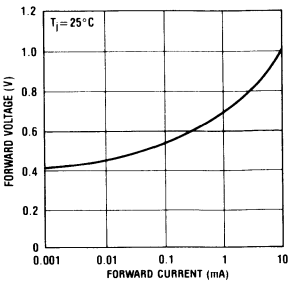
Note 1: Average temperature coefficient is defined as the total voltage change divided by the specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

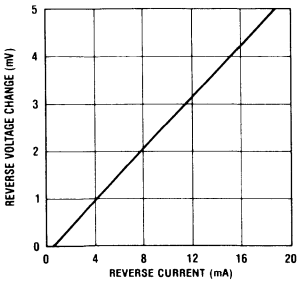
Reverse Characteristics



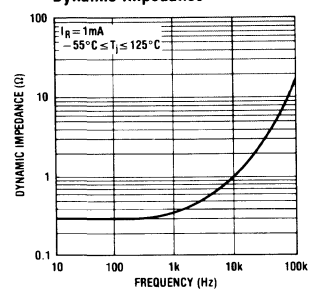
Forward Characteristics



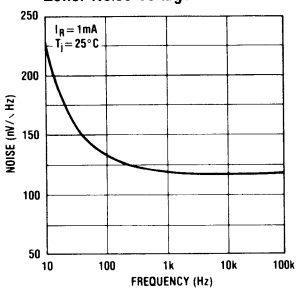
Reverse Voltage Change



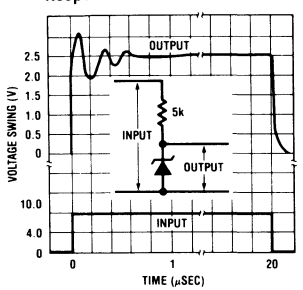
Dynamic Impedance



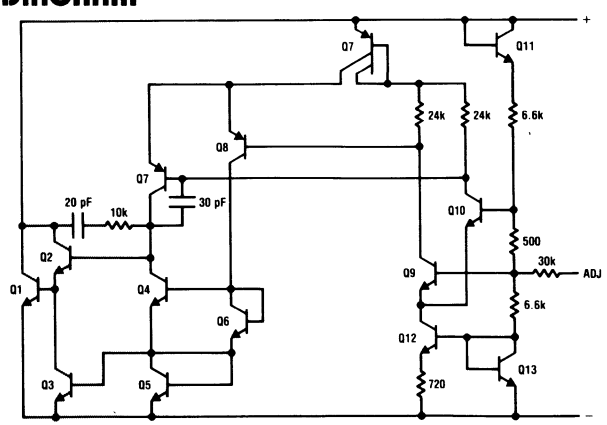
Zener Noise Voltage



Response Time

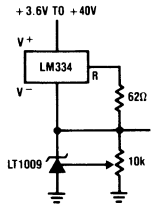


SCHEMATIC DIAGRAM

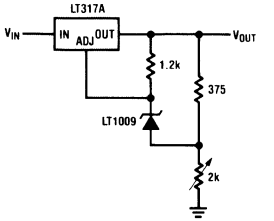


TYPICAL APPLICATIONS

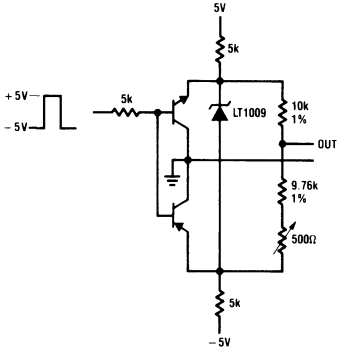
Wide Supply Range, Adjustable Reference



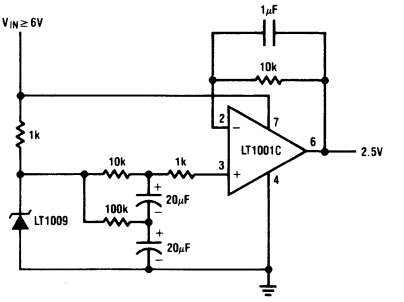
Low Temperature Coefficient Power Regulator



Switchable ±1.25V Bipolar Reference



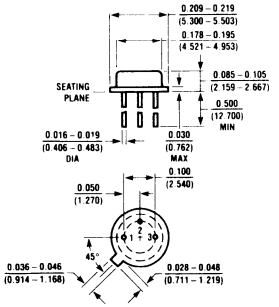
Low Noise 2.5V Buffered Reference



PACKAGE DESCRIPTION

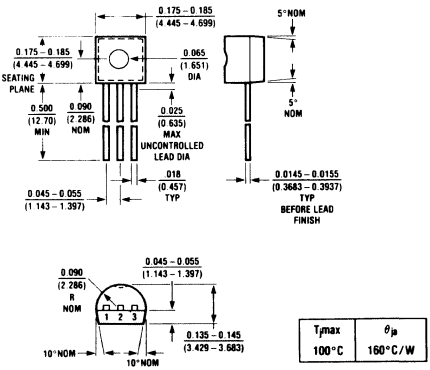
Dimensions in inches (millimeters) unless otherwise noted.

LD Package
Metal Can



$T_j$max	θ_{ja}	θ_{jc}
150°C	440°C/W	80°C/W

LP Package
Plastic



$T_j$max	θ_{ja}
100°C	160°C/W

JULY 1988

FEATURES

- Two Regulated Outputs
  - + 12V at 3A
  - + 5V at 75mA
- 2% Output Voltage Tolerance
- 60dB Ripple Rejection
- 0.7% Load Regulation
- TTL and CMOS Compatible Logic Control
- 100% Thermal Burn-In on All Devices

APPLICATIONS

- Power Supply Sequencing
- Remote On/Off Power Control
- Selective System Power during Emergency Power Operation
- Power Supply with Back-Up

DESCRIPTION

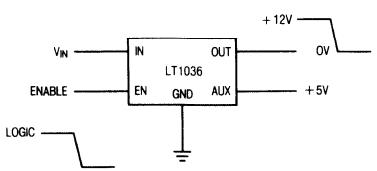
The LT1036 features two positive regulators in the same package. The 12V main regulator offers excellent performance while supplying load currents up to 3A, and the 5V auxiliary regulator provides similar performance while supplying lighter loads of 75mA. The main regulator has the additional feature of being under the shutdown control of a logic signal. When the enable pin is taken to a low logic level, the main regulator shuts down and its output voltage goes to near 0V. During this command, the auxiliary output is unaffected by the main regulator's condition and continues to provide a 5V output.

The main output has current and power limiting combined with thermal shutdown to make it virtually blowout proof. The auxiliary output is not affected by the thermal shutdown mechanism or the state of the main output, allowing it to be used as a back-up in case of overloads or shorts on the main supply.

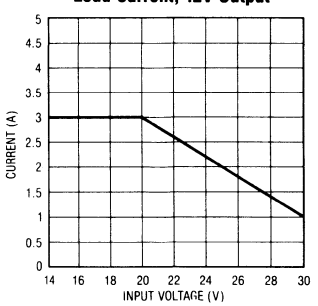
The logic input of the LT1036 (enable pin) has a 1.6V threshold and can be driven from a high source impedance. This allows it to be driven by most logic families, including TTL and CMOS.

For a dual 5V version of the LT1036, please see the LT1035 data sheet.

Functional Diagram



Load Current, 12V Output



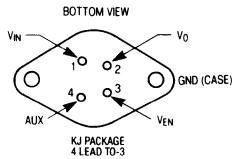
ABSOLUTE MAXIMUM RATINGS

Power Dissipation—Continuous (Note 6) 24W
Power Dissipation—Fault Conditions .. Internally Limited
Input Voltage (V_{IN}) 30V
Enable Voltage (V_{EN}) 30V
Operating Junction Temperature
LT1036M ..... −55°C to 150°C
LT1036C ..... 0°C to 125°C
Storage ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PRECONDITIONING

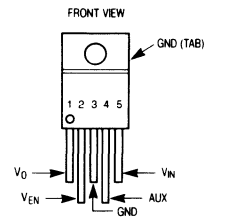
100% Burn-In in Thermal Limit

PACKAGE/ORDER INFORMATION



KJ PACKAGE
4 LEAD TO-3

ORDER PART NUMBER
LT1036MKJ LT1036CKJ



KV PACKAGE
5 LEAD TO-220

LT1036CKV

ELECTRICAL CHARACTERISTICS

Main Regulator (See Note 1) V_{IN} = 15V unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		LT1036M/C MIN	LT1036M/C TYP	LT1036M/C MAX	UNITS
V_O	Output Voltage	T_j = 25°C		11.76	12	12.24	V
	High	15V ≤ V_{IN} ≤ 30V I_{OUT} ≤ I_{MAX} (Note 6)	•	11.52		12.48	V
	Low	7V ≤ V_{IN} ≤ 30V	•		0.1	0.3	V
$\frac{\Delta V_O}{\Delta I_O}$	Load Regulation (Note 6)	V_{IN} = 16V 0 ≤ I_O ≤ 3A (Note 2)	•		10	80	mV
$\frac{\Delta V_O}{\Delta V_{IN}}$	Line Regulation	15V ≤ V_{IN} ≤ 30V (Note 2)			1	4	mV/V
	Ripple Rejection	50Hz ≤ f ≤ 500Hz (Note 8)		50	60		dB
	Thermal Regulation	ΔP_D = 20W (Note 4)			0.003	0.012	%/W
I_O	Available Load Current (Note 6)	15V ≤ V_{IN} ≤ 20V V_{IN} = 25V	• •	3 2	4 2.7		A A
I_{SC}	Short Circuit Current	V_{IN} = 15V V_{IN} = 25V			2.3 1	4 2	A A
V_{IN}	Input Voltage to Maintain Regulation (Dropout Voltage)	(Note 5) I_O = 1A I_O = 3A	 • •		 13.8 14.4	 14.5 15	 V V
I_Q	Quiescent Current	Output High Output Low			4 3	5.5 4.5	mA mA
θ_{JC}	Thermal Resistance, Junction to Case	TO-3 TO-220			1.5 2	2.5 3	°C/W °C/W

ELECTRICAL CHARACTERISTICS Auxiliary Regulator (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1036M/C MIN	LT1036M/C TYP	LT1036M/C MAX	UNITS
V_O	Output Voltage	$T_j = 25°C$		4.9	5.0	5.1	V
		$7.2V \le V_{IN} \le 30V$ $0mA \le I_O \le 75mA$	●	4.8	5.0	5.2	V
$\frac{\Delta V_O}{\Delta I_O}$	Load Regulation	$7.2V \le V_{IN} \le 30V$ $0mA \le I_O \le 75mA$ (Note 2)	●		5	15	mV
$\frac{\Delta V_O}{\Delta V_{IN}}$	Line Regulation	$7.2V \le V_{IN} \le 30V$ (Note 2)	 ●		0.2	1 2	mV/V mV/V
	Ripple Rejection	$50Hz \le f \le 500Hz$			74		dB
I_{SC}	Short Circuit Current (Note 7)	$7.0V \le V_{IN} = 30V$			140	250	mA
V_{IN}	Input Voltage to Maintain Regulation (Dropout Voltage)	(Note 5) $I_O \le 10mA$ $I_O = 75mA$	 ● ●		6.2 6.8	6.5 7.2	V V

ELECTRICAL CHARACTERISTICS Logic Control (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1036M/C MIN	LT1036M/C TYP	LT1036M/C MAX	UNITS
V_{EN}	Enable Threshold Voltage	$7.0V \le V_{IN} \le 30V$ $T_j = 25°C$	 ●	1.45 1.3	1.6 1.6	1.7 1.8	V V
	Enable Pin Current	$V_{EN} \le 1V$ (Note 3)	●	0	1.5	12	μA
		$V_{EN} \ge 2.4V$	●		0	6	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Unless otherwise indicated, these specifications apply for $V_{IN} = 15V$, $I_O = 0mA$, and $T_j = 25°C$.

Note 2: Line and load regulation is measured using a low duty cycle pulse, causing little change in the junction temperature. Effects due to thermal gradients and device heating must be taken into account separately.

Note 3: When the enable pin is at a low logic level, current flows out of the enable pin.

Note 4: Pulse length for this measurement is 20ms.

Note 5: Input voltage is reduced until output drops by 100mV from its initial value.

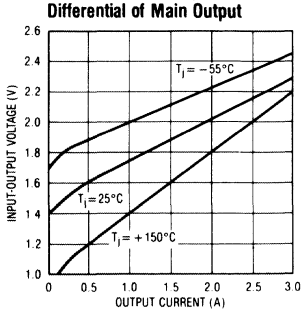
Note 6: See "Load Current" graph.

Note 7: Continuous shorts on the auxiliary output are not allowed unless adequate heat sinking is used to maintain junction temperature below 150°C.

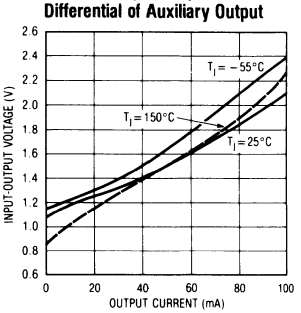
Note 8: Specified but not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

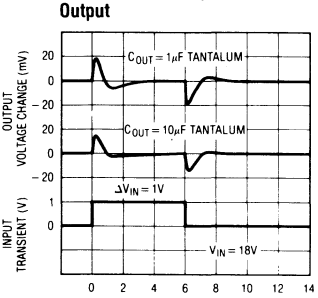
Minimum Input-Output Differential of Main Output



Minimum Input-Output Differential of Auxiliary Output

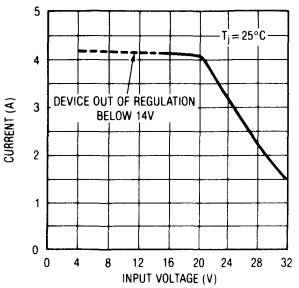


Line Transient Response, 12V Output

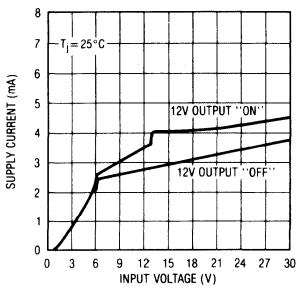


TYPICAL PERFORMANCE CHARACTERISTICS

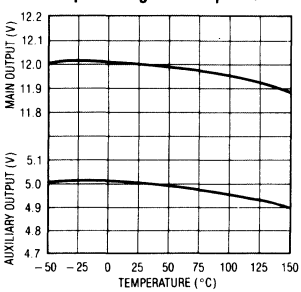
Maximum Available Load Current, 12V Output



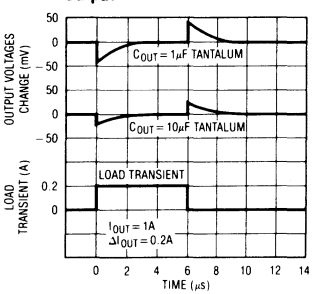
Quiescent Current



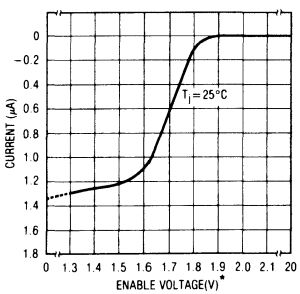
Output Voltage vs Temperature



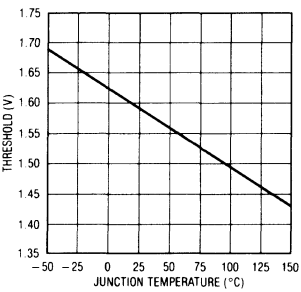
Load Transient Response, 12V Output



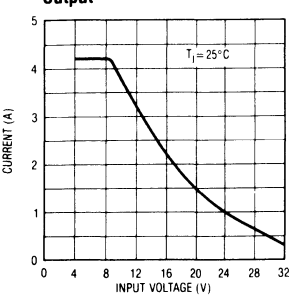
Enable Pin Characteristics



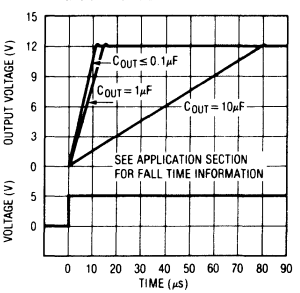
Enable Threshold



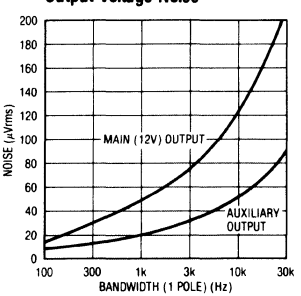
Short Circuit Current, 12V Output



Output Switching Characteristics



Output Voltage Noise



APPLICATIONS INFORMATION

General Information

The LT1036 is a dual output regulator. The main 12V output is capable of delivering up to 3A of load current and can be shut down with a logic signal. The auxiliary 5V output supplies a minimum of 75mA and is unaffected by the logic signal. The outputs are trimmed to ±2% initial tolerance and exhibit excellent line and load regulation.

The logic control feature makes the LT1036 ideal for many system applications where it is desirable to power-up a portion of the system for a period of time, and then power the system down during a standby operation. Applications such as multiple power supply sequencing, elimination of expensive AC and DC power switches, delayed start applications, switching 12V DC loads, and many others are now easily accomplished.

Timing functions, such as delayed power-up or power-down, can also be performed directly at the enable pin.

Because a logic low on the enable pin shuts down the main regulator, feedback from output to enable can be used to generate hysteresis or latching functions.

The low quiescent current drain of the LT1036 makes it useful in battery-powered or battery back-up applications. The enable pin can be used as a "low battery" detector or to shut down major portions of system power, allowing memory portions to continue to operate from the auxiliary output. At low output currents, the auxiliary output will regulate with input voltage typically as low as 6.2V, giving maximum battery life.

Good design practice with all regulators is to bypass the input and output terminals. A 2μF solid tantalum at the input and at both outputs is suggested. For the applications which follow, the bypass capacitors are still recommended, but for simplicity are not shown on the diagram. It is also recommended that for maximum noise immunity the voltage enable pin be tied high if it is unused. It can be tied directly to V_{IN}, as shown in Figure 1, or to the auxiliary output. If the enable pin is left open, it will float to a high logic level of approximately 1.6V and the main output regulator will be at 12V.

The enable pin is fully protected against input voltages up to 30V, even if the power input voltage is zero.

The basic shutdown control circuit uses a direct gate drive or an open collector driver and a pull-up resistor which are tied to V_{AUX}, as shown in Figure 2.

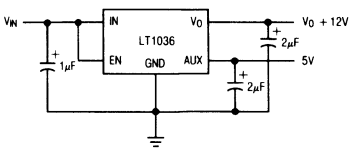


Figure 1

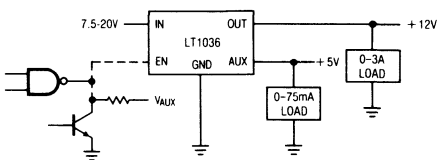


Figure 2

Driving the Enable Pin

The enable pin equivalent schematic is shown in Figure 3. Basically, enable pin current is zero above the threshold and about 1.5μA below the threshold, flowing out of the pin. Standard logic, such as TTL and CMOS, will interface directly to the enable pin, even if the logic output swing is higher than the input voltage (V_{IN}) to the regulator. 15V CMOS can be used to drive the enable pin, even if the regulator is not powered up, without loading the CMOS output.

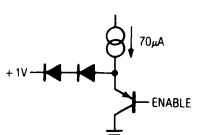


Figure 3

Timing functions, such as delayed power-up or power-down, can be implemented by driving the enable pin with an RC network. The current flowing out of the enable pin should not be used as the timing current in delayed power-up applications as it is temperature sensitive and varies somewhat from device to device. Instead, a resistor tied to the auxiliary output, the input, or to a logic signal

APPLICATIONS INFORMATION

should be used. The timing resistor chosen should provide at least 25μA of current to "swamp out" the effects of the internal current.

Main Output Current/Voltage Characteristics

Following a high to low transition at the enable pin, the main regulator output will begin to drop after a delay of approximately 0.4μs. With no capacitive load, the output will fall to zero in approximately 0.8μs (R_L = 4Ω to 100Ω). With a capacitive load, fall time is limited by the RC product of the load and the output capacitance. For light loads (R_L > 400Ω), the discharge time is controlled by an internal current pull-down of 15mA for output voltages down to 1.5V. Below 1.5V, the pull-down current drops to ≈4mA. The DC output voltage in the shutdown mode is approximately 0.12V due to an internal current path in the regulator. (See Figure 4)

The user should note that the output in the low state can only sink about 3mA. If current is forced into the output, the output voltage will rise to 1V at 5mA and about 1.5V at 10mA. With no output capacitor, the rise time of the main output is about 12μs. With an output capacitor, rise time is limited by the short circuit current of the LT1036 and the load capacitance. A 10μF output capacitor slows the output rise time to approximately 80μs.

Output Current

The main output current limits at about 4A for input voltages below 20V. Internal foldback, or "power limiting", circuitry detects the input-output voltage differential and reduces current limit for input to output voltages exceeding 8V. With 25V input, for instance, short circuit current is reduced to ≈0.9A.

An additional feature of the LT1036 is that the auxiliary supply does not incorporate, nor is it affected by, thermal shutdown. Any fault condition of the main regulator will not affect the auxiliary output voltage.

The following applications circuits will serve to indicate the versatility of the LT1036.

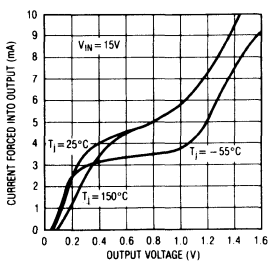
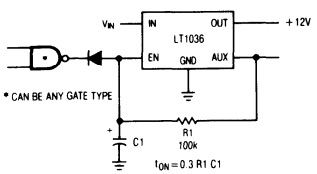


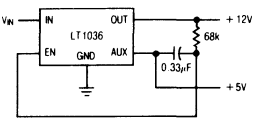
Figure 4

TYPICAL APPLICATIONS

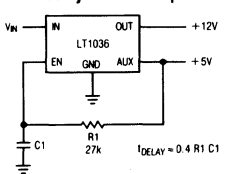
Fast Turn-Off, Delayed Turn-On



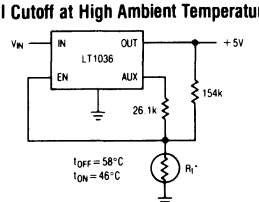
Latch-Off with Output Short



Delayed Power-Up

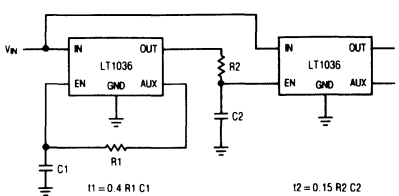


Thermal Cutoff at High Ambient Temperature



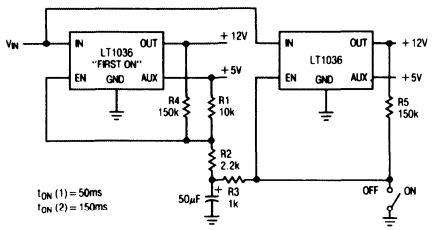
*YELLOW SPRINGS #44008, 30kΩ @ 25°C

Power Supply Turn-On Sequencing

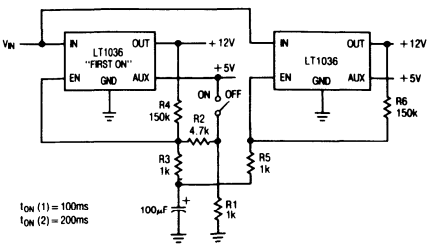


TYPICAL APPLICATIONS

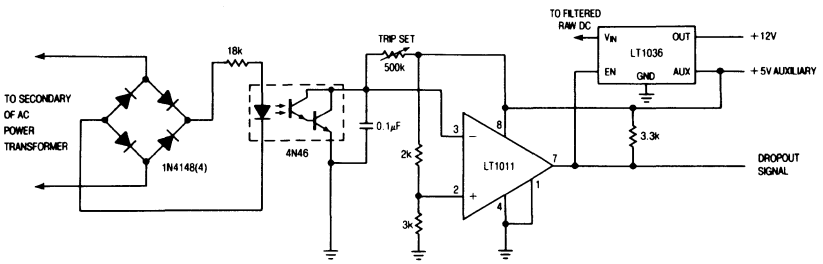
First-On, Last-Off Sequencing



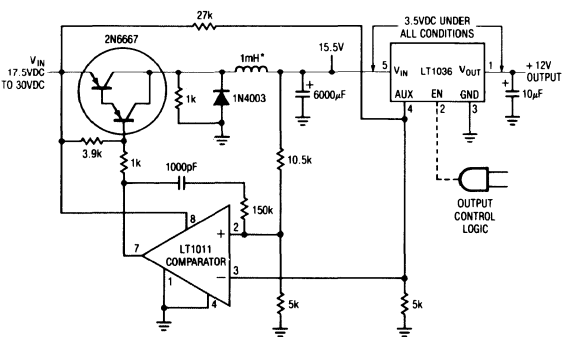
First-On, First-Off Sequencing



Line Dropout Detector

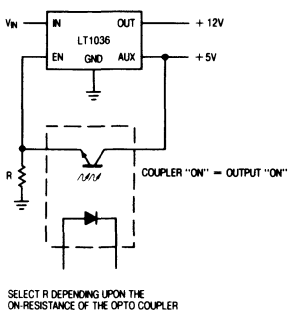


Low Dissipation Regulator



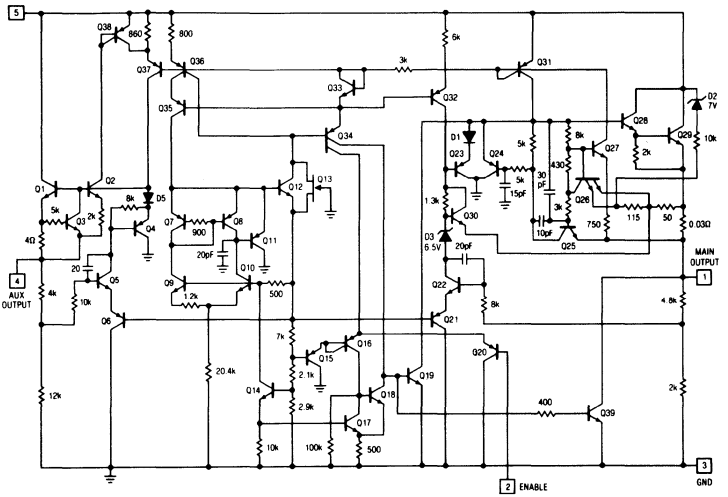
*DALE TD-5
THIS CIRCUIT IS DESIGNED TO REDUCE POWER DISSIPATION IN THE LT1036 OVER A 90VAC–140VAC INPUT RANGE.

Opto-Coupled Output Control



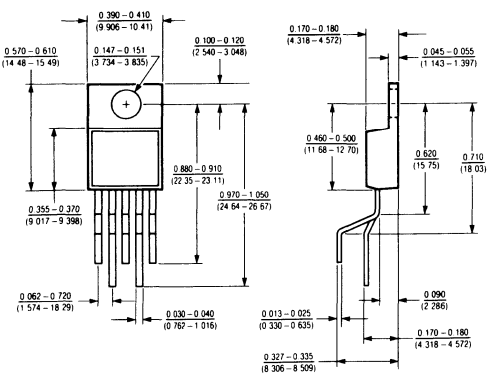
SELECT R DEPENDING UPON THE ON-RESISTANCE OF THE OPTO COUPLER

SCHEMATIC DIAGRAM



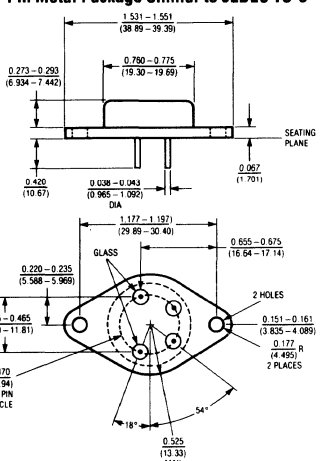
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

KV Package
TO-220 Package (5 Lead)



	T_{JMAX}	θ_{JC}
LT1036C	125°C	3°C/W

KJ Package
4-Pin Metal Package Similar to JEDEC TO-3



	T_{JMAX}	θ_{JC}
LT1036M	150°C	2.5°C/W
LT1036C	125°C	2.5°C/W

FEATURES

- 100mA Output Current
- Low Loss—1.1V at 100mA
- Operating Range 3.5V to 15V
- Reference and Error Amplifier for Regulation
- External Shutdown
- External Oscillator Sync
- Can be Paralleled
- Pin Compatible with the LTC1044/7660

APPLICATIONS

- Voltage Inverter
- Negative Voltage Doubler
- Voltage Regulator
- Positive Voltage Doubler

DESCRIPTION

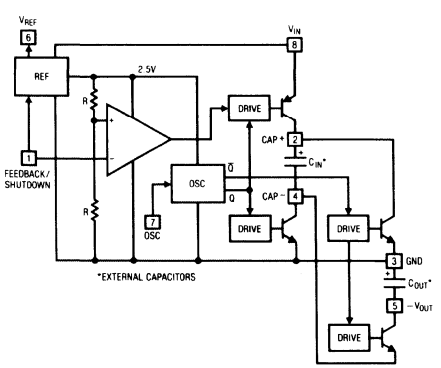
The LT1054 is a monolithic, bipolar, switched capacitor voltage converter and regulator. The LT1054 provides higher output current than previously available converters with significantly lower voltage losses. An adaptive switch drive scheme optimizes efficiency over a wide range of output currents. Total voltage loss at 100mA output current is typically 1.1V. This holds true over the full supply voltage range of 3.5V to 15V. Quiescent current is typically 2.5 mA.

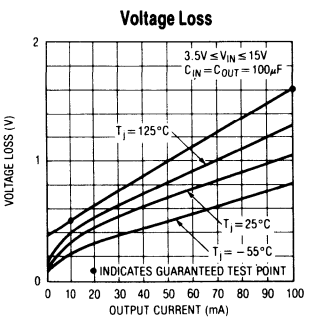
The LT1054 also provides regulation, a feature not previously available in switched capacitor voltage converters. By adding an external resistive divider, a regulated output can be obtained. This output will be regulated against changes in both input voltage and output current. The LT1054 can also be shut down by grounding the feedback pin. Supply current in shut down is less than 100μA.

The internal oscillator of the LT1054 runs at a nominal frequency of 25kHz. The oscillator pin can be used to adjust the switching frequency, or to externally synchronize the LT1054.

The LT1054 is pin compatible with previous converters such as the LTC1044/7660.

BLOCK DIAGRAM

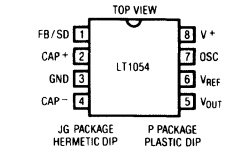




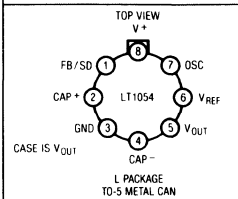
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1) 16V
Input Voltage (Pin 1) ..... $0V \le V_{PIN1} \le V^+$
Input Voltage (Pin 7) ..... $0V \le V_{PIN7} \le V_{REF}$
Operating Temperature Range
LT1054C ..... 0°C to 70°C
LT1054M ..... −55°C to 125°C
Junction Temperature (Note 2)
LT1054C ..... 125°C
LT1054M ..... 150°C
Storage Temperature Range ..... −55°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



JG PACKAGE HERMETIC DIP
P PACKAGE PLASTIC DIP



L PACKAGE
TO-5 METAL CAN

ORDER PART NUMBER
LT1054MJG LT1054CJG LT1054CP
LT1054ML LT1054CL

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	$I_{LOAD} = 0mA$					
	$V_{IN} = 3.5V$	●		2.5	3.5	mA
	$V_{IN} = 15V$	●		3.0	4.5	mA
Supply Voltage Range		●	3.5		15	V
Voltage Loss ($V_{IN} - \lvert V_{OUT} \rvert$)	$C_{IN} = C_{OUT} = 100\mu F$ Tantalum (Note 3)					
	$I_{OUT} = 10mA$	●		0.35	0.55	V
	$I_{OUT} = 100mA$	●		1.10	1.60	V
Output Resistance	$\Delta I_{OUT} = 10mA$ to 100mA (Note 4)	●		10	15	Ω
Oscillator Frequency	$3.5V \le V_{IN} \le 15V$	●	15	25	35	kHz
Reference Voltage	$I_{REF} = 60\mu A$ $T_j = 25°C$		2.35	2.50	2.65	V
		●	2.25		2.75	V
Regulated Voltage	$V_{IN} = 7V$, $T_j = 25°C$ (Note 5)		−4.70	−5.00	−5.20	V
Line Regulation	$7V \le V_{IN} \le 12V$ (Note 5)	●		5	25	mV
Load Regulation	$V_{IN} = 7V$ $500 \le R_L \le 100\Omega$ (Note 5)	●		10	50	mV
Maximum Switch Current				300		mA
Supply Current In Shutdown	$V_{PIN1} = 0V$	●		100	150	μA

The ● denotes specifications which apply over the full operating temperature range. For C grade parts these specifications also apply up to a junction temperature of 100°C.

Note 1: The absolute maximum supply voltage rating of 16V is for unregulated circuits. For regulation mode circuits with $V_{OUT} \le 15V$ at Pin 5, this rating may be increased to 20V.

Note 2: The devices are functional up to the absolute maximum junction temperature.

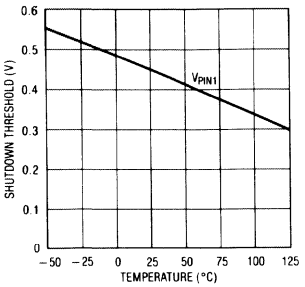
Note 3: For voltage loss tests, the device is connected as a voltage inverter, with Pins 1, 6, and 7 unconnected. The voltage losses may be higher in other configurations.

Note 4: Output resistance is defined as the slope of the curve, (ΔV_{OUT} vs ΔI_{OUT}), for output currents of 10 to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve will be higher at currents < 10mA due to the characteristics of the switch transistors.

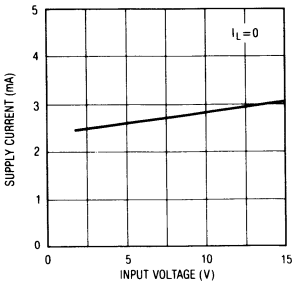
Note 5: All regulation specifications are for a device connected as a positive to negative converter/regulator with R1 = 20k, R2 = 102.5k, C1 = 0.05μF, $C_{IN} = 10\mu F$ tantalum, $C_{OUT} = 100\mu F$ tantalum.

TYPICAL PERFORMANCE CHARACTERISTICS

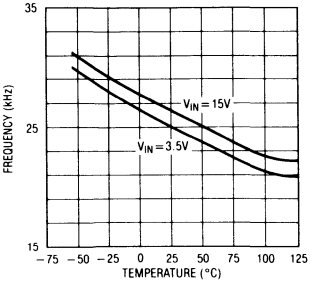
Shutdown Threshold



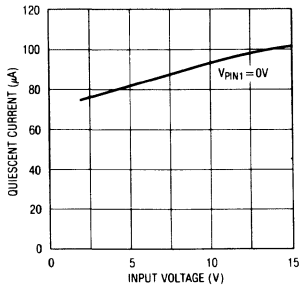
Supply Current



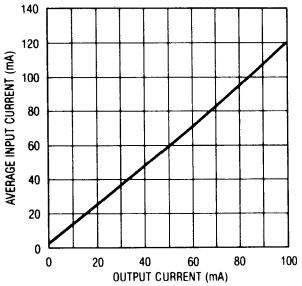
Oscillator Frequency



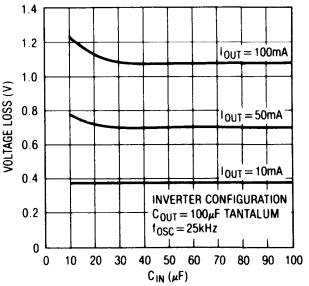
Supply Current in Shutdown



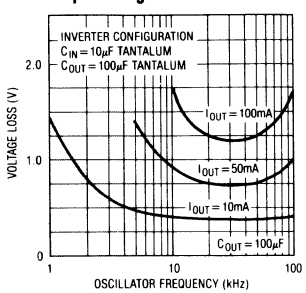
Average Input Current



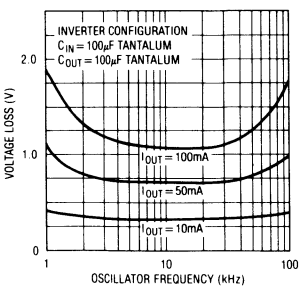
Output Voltage Loss



Output Voltage Loss

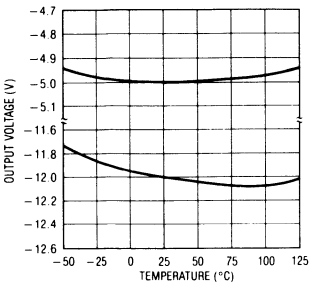


Output Voltage Loss

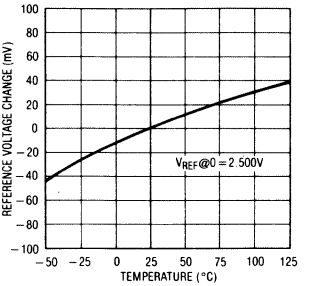


TYPICAL PERFORMANCE CHARACTERISTICS

Regulated Output Voltage



Reference Voltage Temperature Coefficient



APPLICATIONS INFORMATION

Theory of Operation

To understand the theory of operation of the LT1054, a review of a basic switched capacitor building block is helpful.

In Figure 1, when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be q1 = C1V1. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time, the charge on C1 is q2 = C1V2. Note that charge has been transferred from the source, V1, to the output, V2. The amount of charge transferred is:

$$\Delta q = q1 - q2 = C1(V1 - V2).$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is:

$$I = f \times \Delta q = f \times C1(V1 - V2).$$

To obtain an equivalent resistance for the switched-capacitor network we can rewrite this equation in terms of voltage and impedance equivalence:

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}}$$

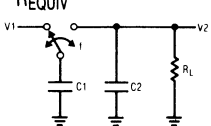


Figure 1. Switched Capacitor Building Block

A new variable, R_{EQUIV}, is defined such that $R_{EQUIV} = 1/fC1$. Thus, the equivalent circuit for the switched capacitor network is as shown in Figure 2. The LT1054 has the same switching action as the basic switched capacitor building block. Even though this simplification doesn't include finite switch on-resistance and output voltage ripple, it provides an intuitive feel for how the device works.

These simplified circuits explain voltage loss as a function of frequency (see typical curve). As frequency is decreased, the output impedance will eventually be dominated by the 1/fC1 term and voltage losses will rise.

Note that losses also rise as frequency increases. This is caused by internal switching losses which occur due to some finite charge being lost on each switching cycle. This charge loss per-unit-cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency this loss becomes significant and voltage losses again rise.

The oscillator of the LT1054 is designed to run in the frequency band where voltage losses are at a minimum.

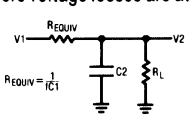


Figure 2. Switched Capacitor Equivalent Circuit

APPLICATIONS INFORMATION

Pin Functions

V^+ (Pin 8): Input supply pin. The LT1054 alternately charges C_{IN} to the input voltage when C_{IN} is switched in parallel with the input supply, and then transfers charge to C_{OUT} when C_{IN} is switched in parallel with C_{OUT}. Switching occurs at the oscillator frequency. During the time that C_{IN} is charging, the peak supply current will be approximately equal to 2.2 times the output current. During the time that C_{IN} is delivering charge to C_{OUT} the supply current drops to approximately 0.2 times the output current. An input supply bypass capacitor will supply part of the peak input current drawn by the LT1054, and average out the current drawn from the supply. A minimum input supply bypass capacitor of 2μF, preferably tantalum or some other low ESR type is recommended. A larger capacitor may be desirable in some cases, for example when the actual input supply is connected to the LT1054 through long leads, or when the pulse currents drawn by the LT1054 might affect other circuitry through supply coupling.

V_{OUT} (Pin 5): In addition to being the output pin, the pin is also tied to the substrate of the device. **Special care must be taken in LT1054 circuits to avoid pulling this pin positive with respect to any of the other pins.** For circuits with the output load connected from V^+ (Pin 8) to V_{OUT} (Pin 5), or from some external positive supply to V_{OUT} (Pin 5), an external transistor must be added as shown in Figure 3. This will prevent V_{OUT} (Pin 5) from being pulled above the ground pin (Pin 3) during start-up. Any small, general purpose transistor such as 2N2222 or 2N2219 can be used. R_X should be chosen to provide enough base drive to the external transistor, so that it is saturated under nominal output voltage and maximum output current conditions.

$$R_X \leq \frac{(|V_{OUT}| - V^+)\beta}{I_{OUT}}$$

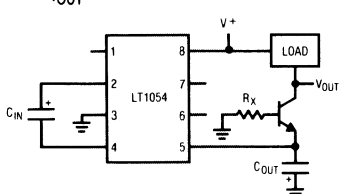


Figure 3

V_{REF} (Pin 6): Reference output pin. This pin provides a 2.5V reference point for use in LT1054 based regulator circuits. The temperature coefficient of the reference voltage has been adjusted so that the temperature coefficient of the regulated output voltage is close to zero. This requires the reference output to have a positive temperature coefficient as can be seen in the typical performance curves. This non-zero drift is necessary to offset a drift term inherent in the internal reference divider and comparator network tied to the feedback pin. The overall result of these drift terms is a regulated output which has a slight positive temperature coefficient at output voltages below 5V and a slight negative TC at output voltages above 5V. Reference output current should be limited, for regulator feedback networks, to approximately 60μA. The reference pin will draw ≈100μA when shorted to ground, and will not affect the internal reference/regulator, so that this pin can also be used as a pull-up for LT1054 circuits that require synchronization.

CAP^+/CAP^- (Pin 2/Pin 4): Pin 2, the positive side of the input capacitor (C_{IN}) is alternately driven between V^+ and ground. When driven to V^+, Pin 2 sources current from V^+. When driven to ground, Pin 2 sinks current to ground. Pin 4, the negative side of the input capacitor is driven alternately between ground and V_{OUT}. When driven to ground, Pin 4 sinks current to ground. When driven to V_{OUT}, Pin 4 sources current from C_{OUT}. In all cases current flow in the switches is unidirectional, as should be expected using bipolar switches.

OSC (Pin 7): Oscillator pin. This pin can be used to raise or lower the oscillator frequency, or to synchronize the device to an external clock. Internally, Pin 7 is connected to the oscillator timing capacitor ($C_t \approx 150pF$) which is alternately charged and discharged by current sources of ±7μA, so that the duty cycle is ≈50%. The LT1054 oscillator is designed to run in the frequency band where switching losses are minimized. However, the frequency can be raised, lowered or synchronized to an external system clock if necessary.

APPLICATIONS INFORMATION

The frequency can be lowered by adding an external capacitor (C1 Figure 4) from Pin 7 to ground. This will increase the charge and discharge times, which lowers the oscillator frequency. The frequency can be increased by adding an external capacitor (C2 Figure 4, in the range of 5pF-20pF) from Pin 2 to Pin 7. This capacitor will couple charge into C_t at the switch transitions, which will shorten the charge and discharge time, raising the oscillator frequency. Synchronization can be accomplished by adding an external resistive pull-up from Pin 7 to the reference pin (Pin 6). A 20k pull-up is recommended. An open collector gate or an NPN transistor can then be used to drive the oscillator pin at the external clock frequency as shown in Figure 4.

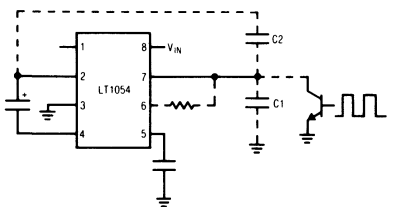


Figure 4

Feedback/Shutdown (Pin 1): This pin has two functions. Pulling Pin 1 below the shutdown threshold (≈0.45V) puts the device into shutdown. In shutdown, the reference/regulator is turned off and switching stops. The switches are set such that both C_{IN} and C_{OUT} are discharged through the output load. Quiescent current in shutdown drops to approximately 100μA (see typical curves). Any open-collector gate can be used to put the LT1054 into shutdown. For normal (unregulated) operation the device will start back up when the external gate is shut off. In LT1054 circuits that use the regulation feature, the external resistor divider can provide enough pull-down to keep the device in shutdown until the output capacitor (C_{OUT}) has fully discharged. For most applications where the LT1054 would be run intermittently, this does not present a problem because the discharge time of the output capacitor will be short compared to the off time of the device. In applications where the device has to start-up before the output capacitor (C_{OUT}) has fully discharged, a restart pulse must be applied to Pin 1 of the LT1054. Using the circuit of Figure 5, the restart signal can be either a pulse ($t_p > 100\mu s$) or a logic high. Diode coupling the restart signal into Pin 1 will allow the output voltage to come up and regulate without overshoot. The resistor divider R3/R4 in Figure 5 should be chosen to provide a signal level at Pin 1 of 0.7V-1.1V.

Pin 1 is also the inverting input of the LT1054's error amplifier, and as such can be used to obtain a regulated output voltage.

Regulation

The error amplifier of the LT1054 servoes the drive to the PNP switch to control the voltage across the input capacitor (C_{IN}), which in turn will determine the output voltage. Using the reference and error amplifier of the LT1054, an external resistive divider is all that is needed to set the regulated output voltage. Figure 5 shows the basic regulator configuration and the formula for calculating the appropriate resistor values. The recommended value for R1 is 20k for all output voltages. Frequency compensation is accomplished by adjusting the ratio of C_{IN}/C_{OUT}.

For best results, this ratio should be ≈1/10. C1, required for good load regulation, should be 0.05μF for all output voltages.

It can be seen from the circuit block diagram that the maximum regulated output voltage is limited by the supply voltage. For the basic configuration, $|V_{OUT}|$ referred to the ground pin of the LT1054 must be less than the total of the supply voltage minus the voltage loss due to the switches. The voltage loss versus output current due to the switches can be found in the typical performance curves. Other configurations such as the negative doubler can provide higher output voltages at reduced output currents (see typical applications).

APPLICATIONS INFORMATION

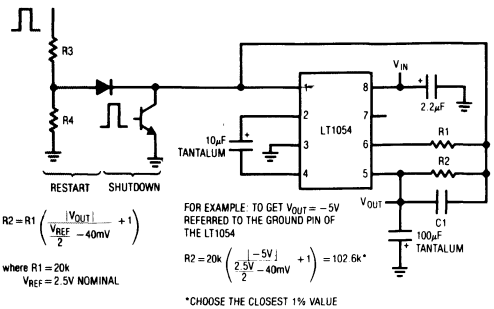


Figure 5

Capacitor Selection

While the exact values of C_{IN} and C_{OUT} are non-critical, good quality, low ESR capacitors such as solid tantalum are necessary to minimize voltage losses at high currents. For C_{IN} the effect of the ESR of the capacitor will be multiplied by four, due to the fact that switch currents are approximately two times higher than output current, and losses will occur on both the charge and discharge cycle. This means that using a capacitor with 1Ω of ESR for C_{IN} will have the same effect as increasing the output impedance of the LT1054 by 4Ω. This represents a significant increase in the voltage losses. For C_{OUT} the affect of ESR is less dramatic. C_{OUT} is alternately charged and discharged at a current approximately equal to the output current, and the ESR of the capacitor will cause a step function to occur, in the output ripple, at the switch transitions. This step function will degrade the output regulation for changes in output load current, and should be avoided. Realizing that large value tantalum capacitors can be expensive, a technique that can be used is to parallel a smaller tantalum capacitor with a large aluminum electrolytic capacitor to gain both low ESR and reasonable cost.

Output Ripple

The peak-to-peak output ripple is determined by the value of the output capacitor and the output current. Peak-to-peak output ripple may be approximated by the formula:

$$dV = \frac{I_{OUT}}{2fC_{OUT}}$$

where dV = p-p ripple
f = oscillator frequency

For output capacitors with significant ESR, a second term must be added to account for the voltage step at the switch transitions. This step is, approximately equal to:

$$(2I_{OUT})(\text{ESR of } C_{OUT})$$

Power Dissipation

The power dissipation of any LT1054 circuit must be limited such that the junction temperature of the device does not exceed the maximum junction temperature ratings. The total power dissipation must be calculated from two components, the power loss due to voltage drops in the switches, and the power loss due to drive current losses. The total power dissipated by the LT1054 can be calculated from:

$$P \approx (V_{IN} - |V_{OUT}|)(I_{OUT}) + (V_{IN})(I_{OUT})\ (0.2)$$

where both V_{IN} and V_{OUT} are referred to the ground pin (Pin 3) of the LT1054. For LT1054 regulator circuits, the power dissipation will be equivalent to that of a linear regulator. Due to the limited power handling capability of the LT1054 packages, the user will have to limit output current requirements or take steps to dissipate some power external to the LT1054 for large input/output differentials.

APPLICATIONS INFORMATION

This can be accomplished by placing a resistor in series with C_{IN} as shown in Figure 6. A portion of the input voltage will then be dropped across this resistor, without affecting the output regulation. Because switch current is approximately 2.2 times the output current, and the resistor will cause a voltage drop when C_{IN} is both charging and discharging, the resistor should be chosen as:

$$R_X = V_X/(4.4\ I_{OUT})$$

where

$$V_X \approx V_{IN} - [(\text{LT1054 voltage loss})\ (1.3) + |V_{OUT}|]$$

and I_{OUT} = maximum required output current. The factor of 1.3 will allow some operating margin for the LT1054.

For example: assume a +12V to −5V converter at 100mA output current. First calculate the power dissipation without an external resistor:

$$P = (12V - |-5V|)\ (100mA) + (12V)\ (100mA)\ (0.2)$$
$$P = 700mW + 240mW = 940mW$$

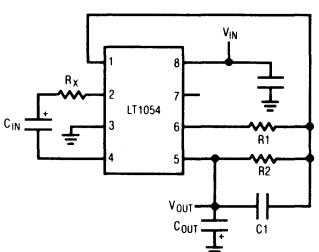


Figure 6

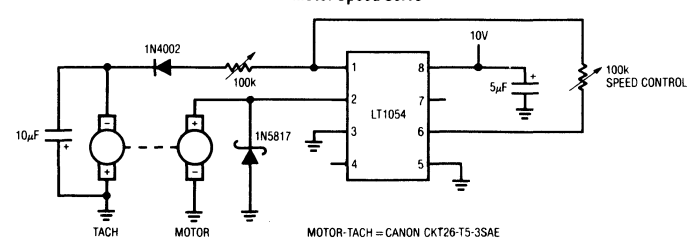
At θ_{JA} of 130°C/W for a commercial plastic device this would cause a junction temperature rise of 122°C, so that the device would exceed the maximum junction temperature at an ambient temperature of 25°C. Now calculate the power dissipation with an external-resistor (R_X). First find how much voltage can be dropped across R_X. The maximum voltage loss of the LT1054 in the standard regulator configuration at 100mA output current is 1.6V, so

$$V_X = 12V - [(1.6V)\ (1.3) + |-5V|] = 4.9V \text{ and}$$
$$R_X = 4.9V/(4.4)\ (100mA) = 11\Omega.$$

This resistor will reduce the power dissipated by the LT1054 by (4.9V) (100mA) = 490mW. The total power dissipated by the LT1054 would then be = (940mW − 490mW) = 450mW. The junction temperature rise would now be only 58°C. Although commercial devices are functional up to a junction temperature of 125°C, the specifications are tested to a junction temperature of 100°C, so ideally you should limit the junction temperature to 100°C. For the above example this would mean limiting the ambient temperature to 42°C. Other steps can be taken, however, to allow higher ambient temperatures. The thermal resistance numbers for the LT1054 packages represent worst-case numbers with no heat-sinking and still air. Small clip-on type heat sinks can be used to lower the thermal resistance of the LT1054 package. In some systems there may be some available airflow which will help to lower the thermal resistance. Wide PC board traces from the LT1054 leads can also help to remove heat from the device. This is especially true for plastic packages.

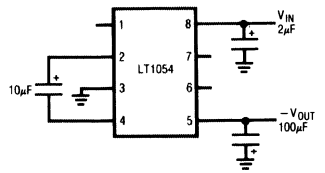
TYPICAL APPLICATIONS

Motor Speed Servo

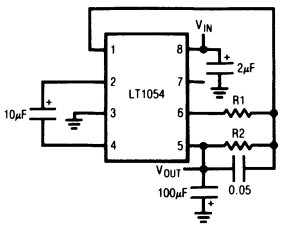


TYPICAL APPLICATIONS

Basic Voltage Inverter

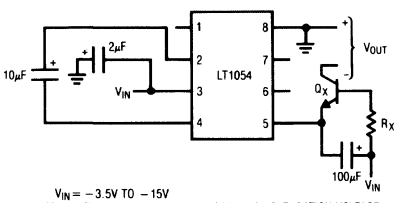


Basic Voltage Inverter/Regulator



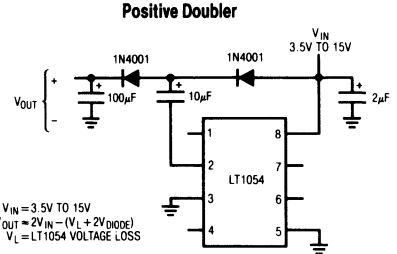
$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) = 20k\left(\frac{|V_{OUT}|}{1.21V} + 1\right)$$

Negative Voltage Doubler



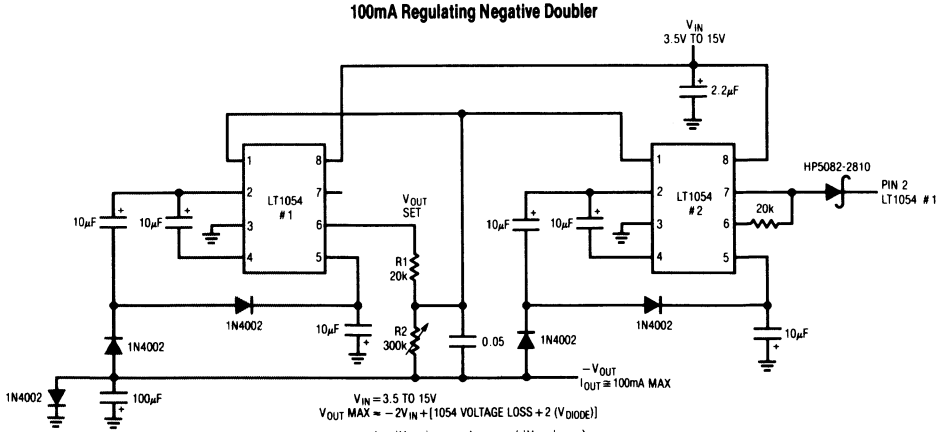
$V_{IN} = -3.5V$ TO $-15V$
$V_{OUT} = 2V_{IN} + (LT1054\ VOLTAGE\ LOSS) + (Q_X\ SATURATION\ VOLTAGE)$

Positive Doubler



$V_{IN} = 3.5V$ TO $15V$
$V_{OUT} \approx 2V_{IN} - (V_L + 2V_{DIODE})$
$V_L = LT1054\ VOLTAGE\ LOSS$

100mA Regulating Negative Doubler

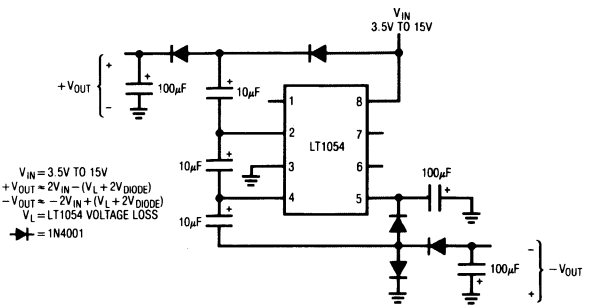


$V_{IN} = 3.5$ TO $15V$
$V_{OUT}\ MAX \approx -2V_{IN} + [1054\ VOLTAGE\ LOSS + 2\ (V_{DIODE})]$

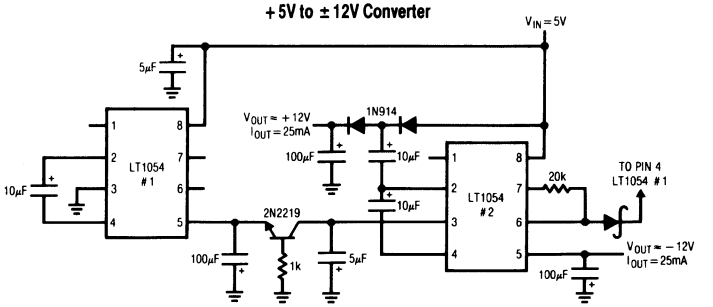
$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21V} + 1\right)$$

TYPICAL APPLICATIONS

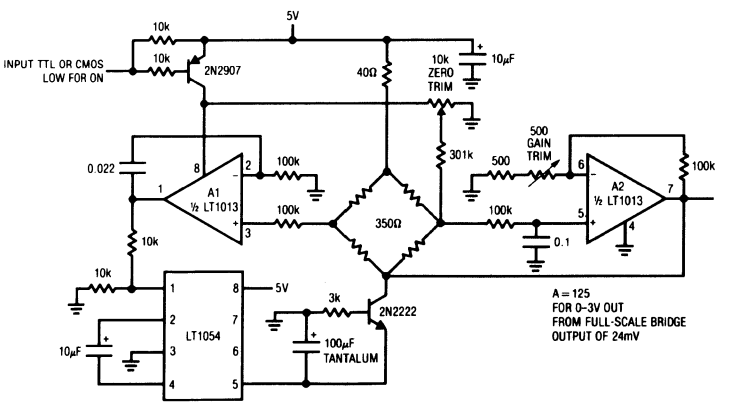
Dual Output Voltage Doubler



+5V to ±12V Converter

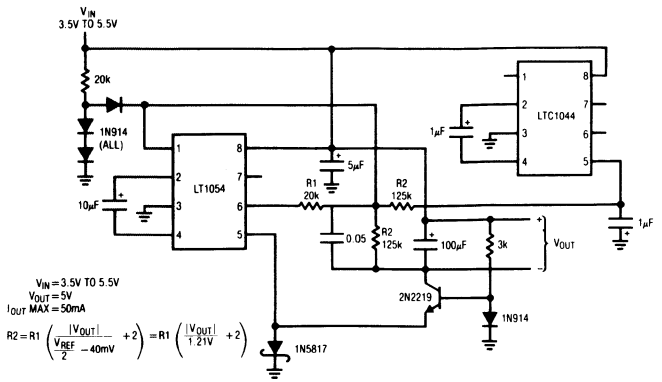


Strain Gage Bridge Signal Conditioner

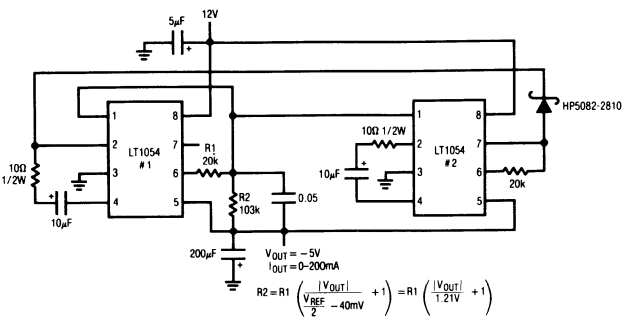


TYPICAL APPLICATIONS

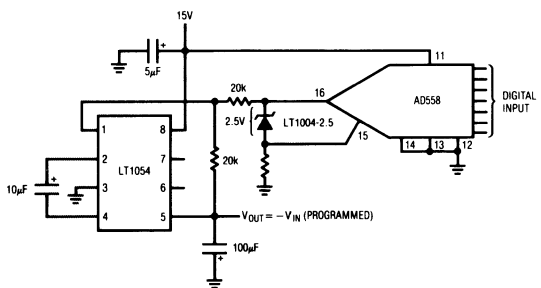
3.5V to 5V Regulator



Regulating 200mA + 12V to −5V Converter

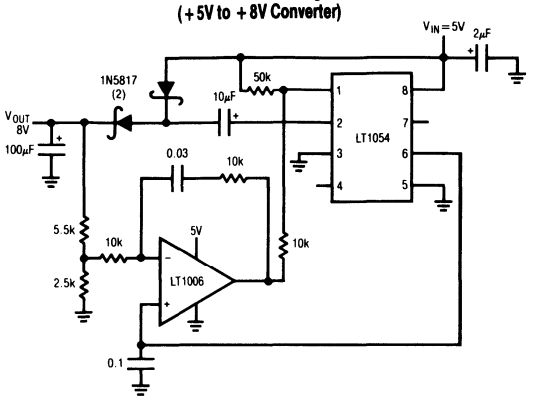


Digitally Programmable Negative Supply

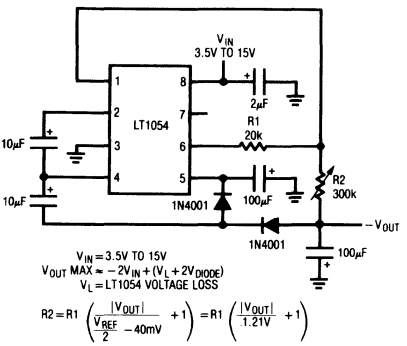


TYPICAL APPLICATIONS

Positive Doubler with Regulation (+5V to +8V Converter)



Negative Doubler with Regulator



V_{IN} = 3.5V TO 15V

V_{OUT} MAX ≈ $-2V_{IN} + (V_L + 2V_{DIODE})$

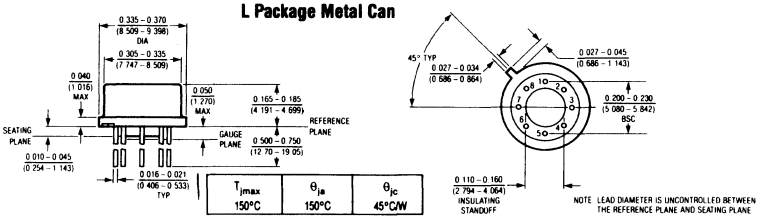
V_L = LT1054 VOLTAGE LOSS

$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21V} + 1\right)$$

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

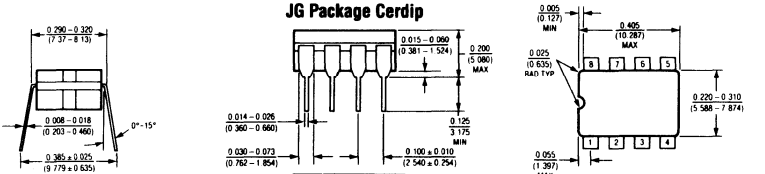
L Package Metal Can



T_{jmax}	θ_{ja}	θ_{jc}
150°C	150°C	45°C/W

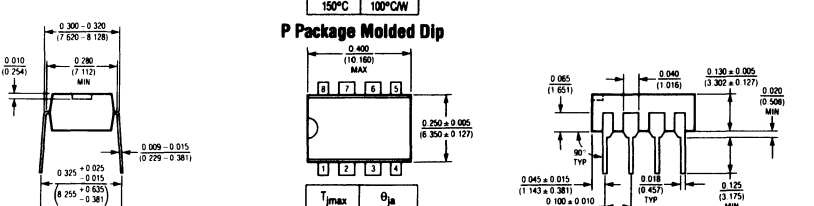
NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE

JG Package Cerdip



T_{jmax}	θ_{ja}
150°C	100°C/W

P Package Molded Dip



T_{jmax}	θ_{ja}
100°C	130°C/W

MAY 1987

FEATURES

- Wide Input Voltage Range 3V-60V
- Low Quiescent Current—6mA
- Internal 5A Switch
- Very Few External Parts Required
- Self-Protected Against Overloads
- Operates in Nearly All Switching Topologies
- Shutdown Mode Draws Only 50μA Supply Current
- Flyback-Regulated Mode has Fully Floating Outputs
- Comes in Standard 5-Pin Packages
- Can be Externally Synchronized (Consult Factory)

APPLICATIONS

- Logic Supply 5V @ 10A
- 5V Logic to ±15V Op Amp Supply
- Offline Converter up to 200W
- Battery Upconverter
- Power Inverter (+ to −) or (− to +)
- Fully Floating Multiple Outputs

USER NOTE:

This data sheet is only intended to provide specifications, graphs, and a general functional description of the LT1070. Application circuits are included to show the capability of the LT1070.

DESCRIPTION

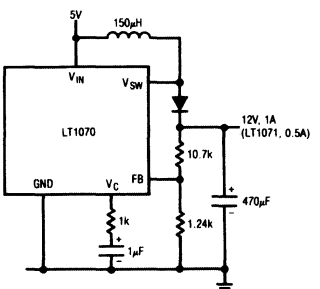
The LT1070 is a monolithic high power switching regulator. It can be operated in all standard switching configurations including buck, boost, flyback, forward, inverting and "Cuk". A high current, high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1070 to be built in a standard 5-pin TO-3 or TO-220 power package. This makes it extremely easy to use and provides "bust proof" operation similar to that obtained with 3-pin linear regulators.

The LT1070 operates with supply voltages from 3V to 60V, and draws only 6mA quiescent current. It can deliver load power up to 100 watts with no external power devices. By utilizing current-mode switching techniques, it provides excellent AC and DC load and line regulation.

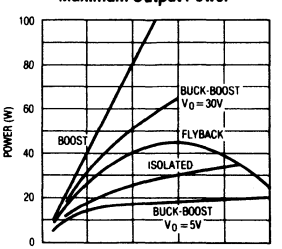
The LT1070 has many unique features not found even on the vastly more difficult to use low power control chips presently available. It uses adaptive anti-sat switch drive to allow very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 50μA typical for standby operation. Totally isolated and regulated outputs can be generated by using the optional "flyback regulation mode" built into the LT1070, without the need for optocouplers or extra transformer windings.

TYPICAL APPLICATION

Boost Converter (5V to 12V)



Maximum Output Power*



*ROUGH GUIDE ONLY. BUCK MODE $P_{OUT} = 5A \times V_{OUT}$. SPECIAL TOPOLOGIES DELIVER MORE POWER.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- LT1070HV (See Note 1) 60V
- LT1070 (See Note 1) 40V

Switch Output Voltage
- LT1070HV (Note 2) 75V
- LT1070 ..... 65V

Feedback Pin Voltage (Transient, 1ms) ..... ±15V

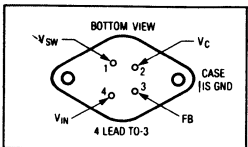
Operating Junction Temperature Range
- LT1070HVM, LT1070M ..... −55°C to + 150°C
- LT1070HVC, LT1070C (Oper.) ..... 0°C to + 100°C
- LT1070HVC, LT1070C (Sh. Ckt.) .. 0°C to + 125°C

Storage Temperature Range ..... −65°C to +150°C

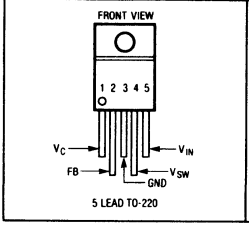
Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1: Minimum switch "on" time for the LT1070 in current limit is ≈1.0μsec. This limits the maximum input voltage during short circuit conditions, *in the buck and inverting modes only*, to ≈35V. Normal (unshorted) conditions are not affected. Mask changes are being implemented which will reduce minimum "on" time to ≤1μsec, increasing maximum short circuit input voltage above 40V. If the present LT1070 (contact factory for package date code) is being operated in the buck or inverting mode at high input voltages and short circuit conditions are expected, a resistor must be placed in series with the inductor, as follows:,

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1070 HVMKJ LT1070MKJ LT1070 HVCKJ LT1070 CKJ



ORDER PART NUMBER
LT1070 HVCKV LT1070 CKV

The value of the resistor is given by:

$$R = \frac{t \bullet f \bullet V_{IN} - Vf}{I_{(LIMIT)}}$$

t = Minimum "on" time of LT1070 in current limit
f = Operating frequency (40kHz)
Vf = Forward voltage of external catch diode at $I_{(LIMIT)}$
$I_{(LIMIT)}$ = Current limit of ≈8A
Please consult factory for additional details.

Note 2: Consult factory for availability of a LT1070HV unit rated at 90V maximum switch voltage.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	Measured at Feedback Pin		1.224	1.244	1.264	V
			●	1.214	1.244	1.274	
I_B	Feedback Input Current	V_{FB} = V_{REF}			350	750	nA
			●			1100	
gm	Error Amplifier Transconductance	ΔI_C = ±25μA		3000	4400	6000	μmho
			●	2400		7000	
	Error Amplifier Source or Sink Current	V_C = 1.5V		150	200	350	μA
			●	120		400	
	Error Amplifier Clamp Voltage	Hi Clamp, V_{FB} = 1V		1.8		2.3	V
		Lo Clamp, V_{FB} = 1.5V		0.25	0.38	0.5	
	Reference Voltage Line Regulation	3V ≤ V_{IN} ≤ V_{MAX}	●			0.03	%/V
A_V	Error Amplifier Voltage Gain	0.7V ≤ V_C ≤ 1.4V		500	800	2000	V/V
	Minimum Input Voltage		●		2.6	3.0	V
I_Q	Supply Current	3V ≤ V_{IN} ≤ V_{MAX}, V_C = 0.6V			6	9	mA
	Control Pin Threshold	Duty Cycle = 0		0.8	0.9	1.05	V
			●	0.6		1.2	
	Normal/Flyback Threshold on Feedback Pin			0.4	0.45	0.52	V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open.

SYMBOL	PARAMETER	CONDITIONS				MIN	TYP	MAX	UNITS
V_{FB}	Flyback Reference Voltage	I_{FB} = 50μA				15	16.3	17.6	V
					●	14		18	
	Change in Flyback Reference Voltage	0.05 ≤ I_{FB} ≤ 1mA				4.5	6.8	8.5	V
	Flyback Reference Voltage Line Regulation	I_{FB} = 50μA 3V ≤ V_{IN} ≤ V_{MAX}					0.01	0.03	%/V
	Flyback Amplifier Transconductance (gm)	ΔI$_C$ = ± 10μA				150	300	500	μmho
	Flyback Amplifier Source and Sink Current	V_C = 1.5V	Source		●	15	32	50	μA
		I_{FB} = 50μA	Sink		●	25	40	70	
BV	Output Switch Breakdown Voltage (Note 2)	3V ≤ V_{IN} ≤ V_{MAX}		LT1070	●	65	90		V
		I_{SW} = 5mA		LT1070HV	●	75	90		
V_{SAT}	Output Switch (Note 1) "On" Resistance	I_{SW} = 5A					0.15	0.24	Ω
	Control Voltage to Switch Current Transconductance	LT1070					8		A/V
I_{LIM}	Switch Current Limit	Duty Cycle = 50%			●	5		13	A
		50% < Duty Cycle = 80%			●	4		10	
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On-Time						25	35	mA/A
f	Switching Frequency					35	40	45	kHz
					●	33		47	
DC (max)	Maximum Switch Duty Cycle					90	92	97	%
	Flyback Sense Delay Time						1.5		μs
	Shutdown Mode Supply Current	3V ≤ V_{IN} ≤ V_{MAX} V_C = 0.05V					100	250	μA
	Shutdown Mode Threshold Voltage	3V ≤ V_{IN} ≤ V_{MAX}				100	150	250	mV
					●	50		300	

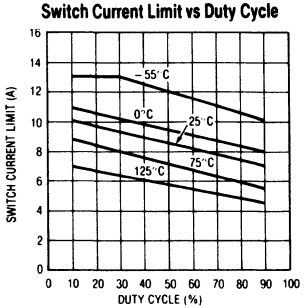
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Measured with V_C in hi clamp, V_{FB} = 0.8V.

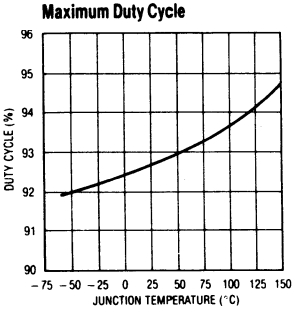
Note 2: Consult factory for availability of LT1070HV units rated at 90V maximum switch voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

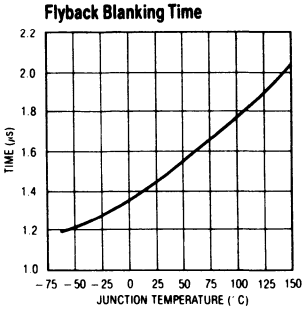
Switch Current Limit vs Duty Cycle



Maximum Duty Cycle

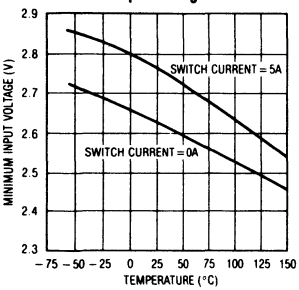


Flyback Blanking Time

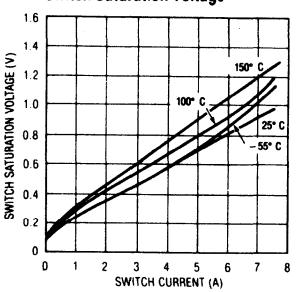


TYPICAL PERFORMANCE CHARACTERISTICS

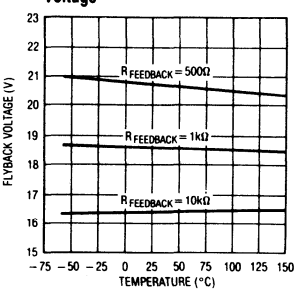
Minimum Input Voltage



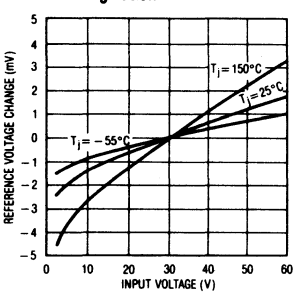
Switch Saturation Voltage



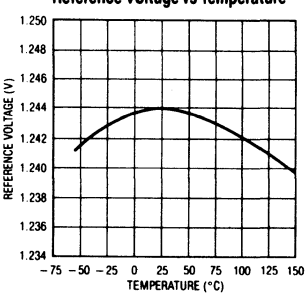
Isolated Mode Flyback Reference Voltage



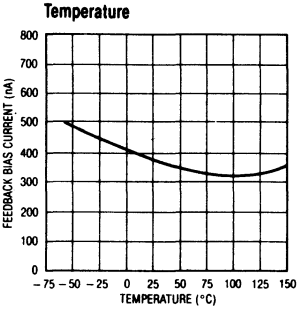
Line Regulation



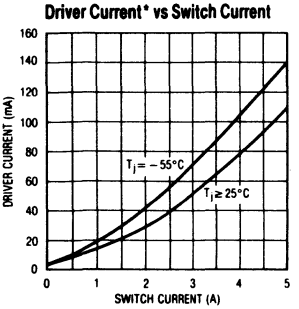
Reference Voltage vs Temperature



Feedback Bias Current vs Temperature

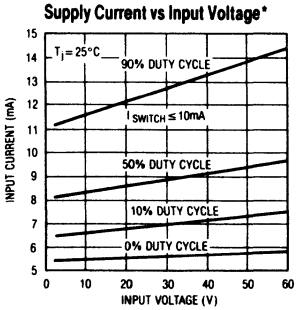


Driver Current* vs Switch Current



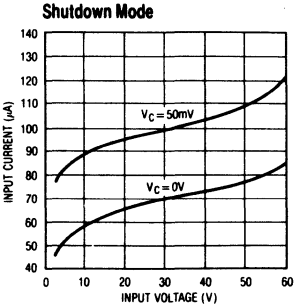
*AVERAGE POWER SUPPLY CURRENT IS FOUND BY MULTIPLYING DRIVER CURRENT BY DUTY CYCLE, THEN ADDING QUIESCENT CURRENT.

Supply Current vs Input Voltage*



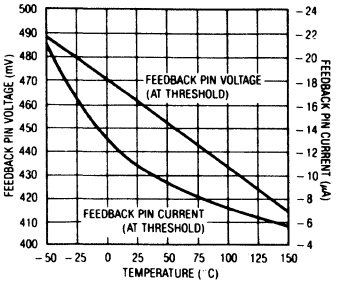
*UNDER VERY LOW OUTPUT CURRENT CONDITIONS, DUTY CYCLE FOR MOST CIRCUITS WILL APPROACH 10% OR LESS.

Supply Current vs Input Voltage Shutdown Mode

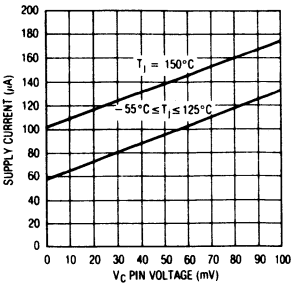


TYPICAL PERFORMANCE CHARACTERISTICS

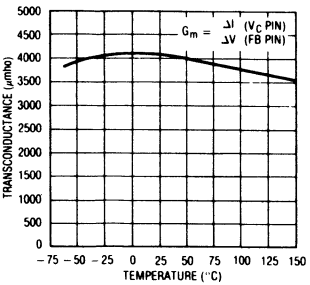
Normal/Flyback Mode Threshold on Feedback Pin



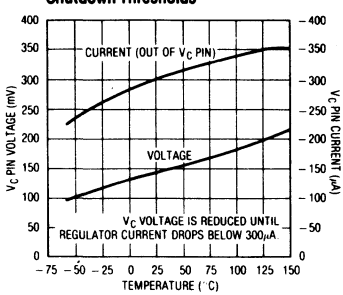
Shutdown Mode Supply Current



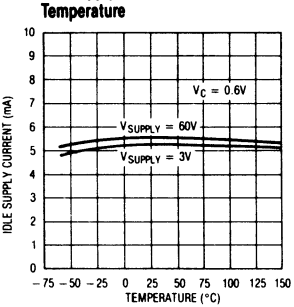
Error Amplifier Transconductance



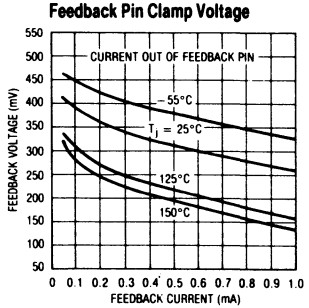
Shutdown Thresholds



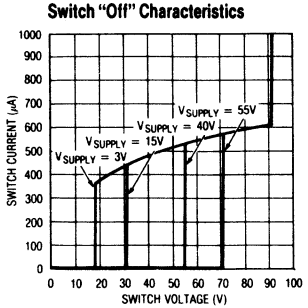
Idle Supply Current vs Temperature



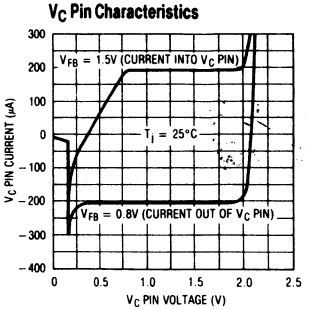
Feedback Pin Clamp Voltage



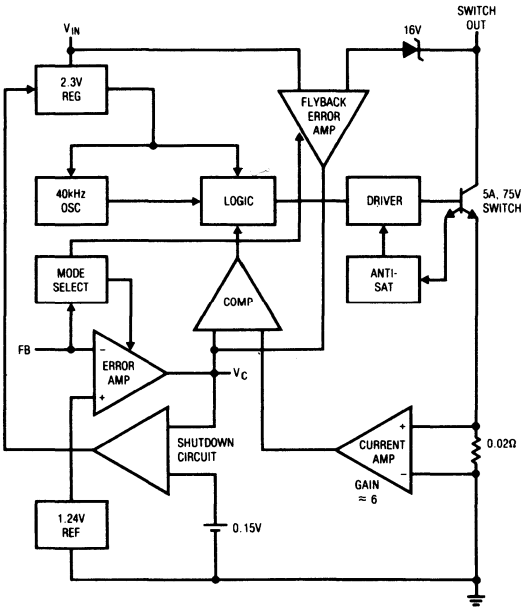
Switch "Off" Characteristics



V_C Pin Characteristics



BLOCK DIAGRAM



LT1070 OPERATION

The LT1070 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the block diagram, the switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at midfrequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low-dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1070. This low-dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Special adaptive anti-sat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second

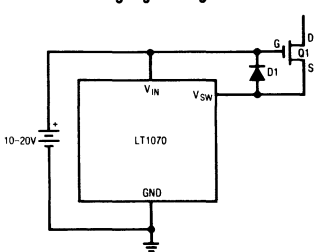
LT1070 OPERATION

function; when pulled low with an external resistor, it programs the LT1070 to disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1070 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1070 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

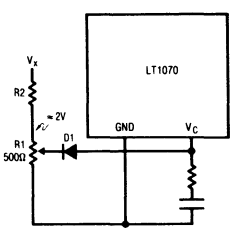
The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1070 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown, with only 50μA supply current for shutdown circuitry biasing.

TYPICAL APPLICATIONS

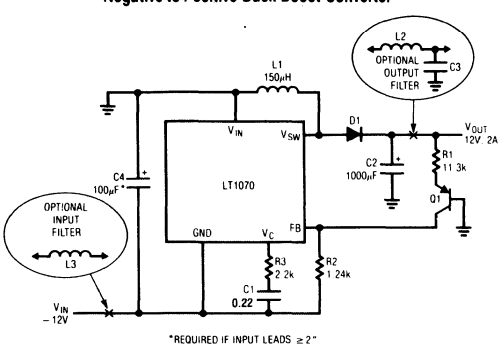
Driving High Voltage FET



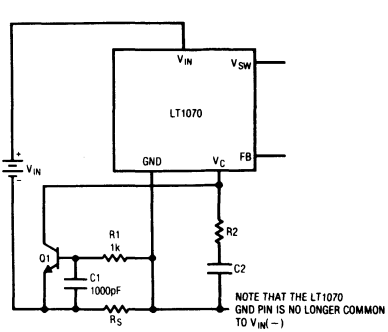
External Current Limit



Negative to Positive Buck-Boost Converter

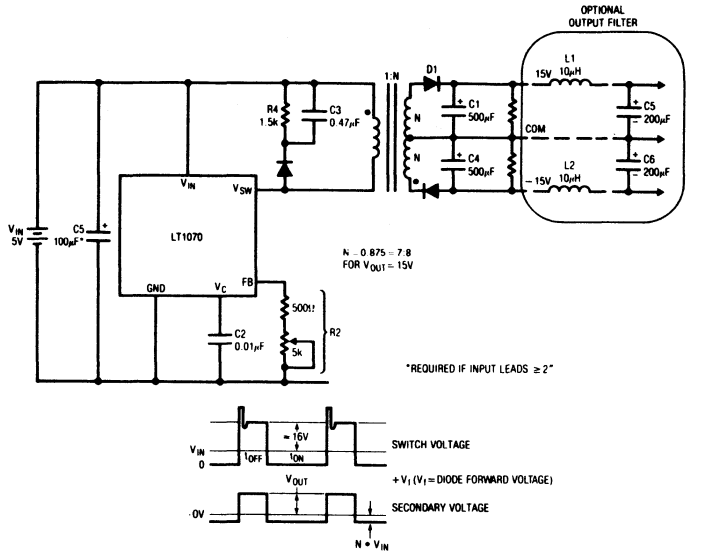


External Current Limit

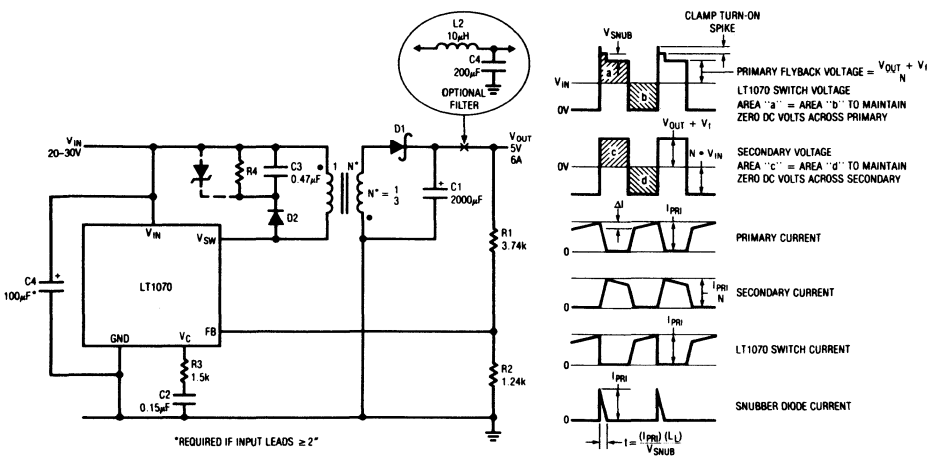


TYPICAL APPLICATIONS

Totally Isolated Converter

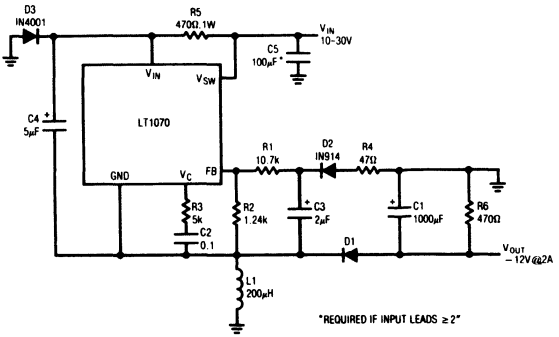


Flyback Converter

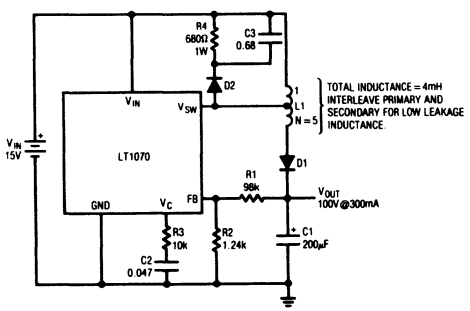


TYPICAL APPLICATIONS

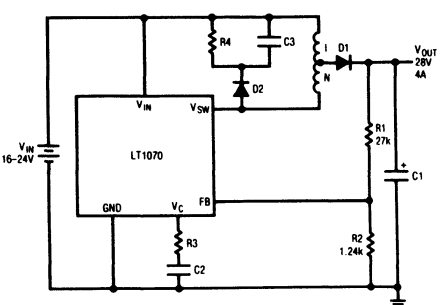
Positive to Negative Buck-Boost Converter



Voltage Boosted Boost Converter

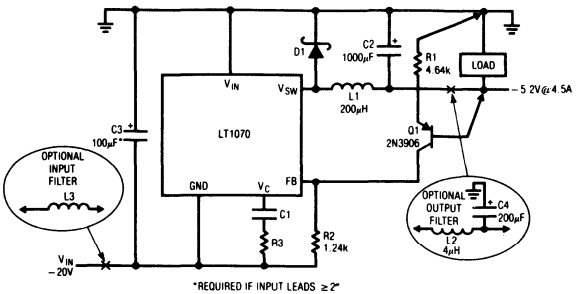


Current Boosted Boost Converter

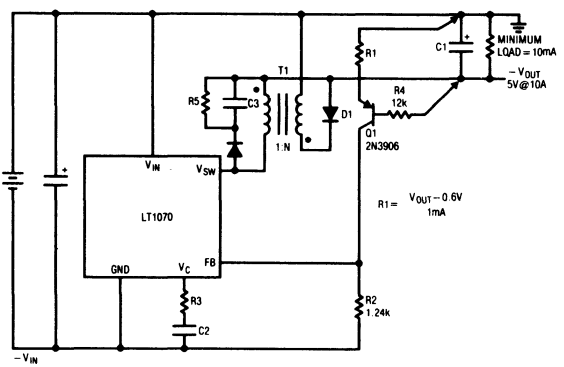


TYPICAL APPLICATIONS

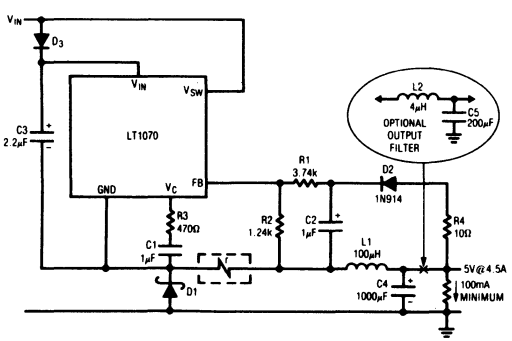
Negative Buck Converter



Negative Current Boosted Buck Converter

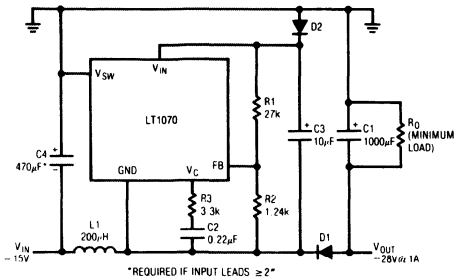


Positive Buck Converter

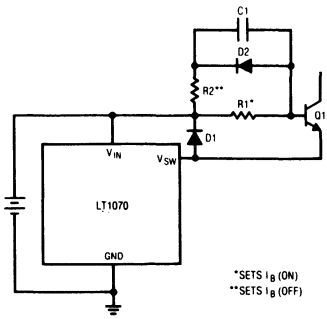


TYPICAL APPLICATIONS

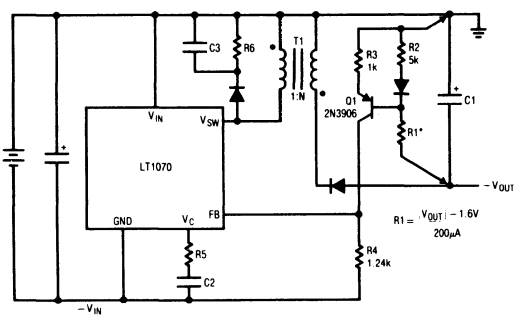
Negative Boost Regulator



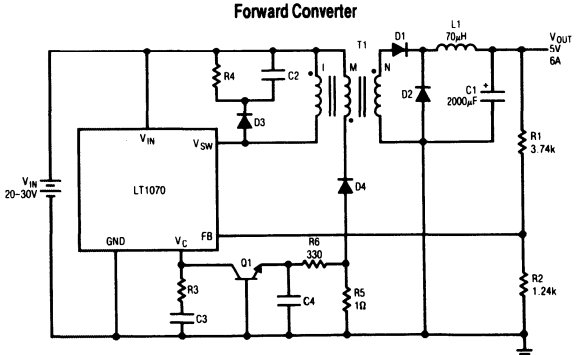
Driving High Voltage NPN



Negative Input-Negative Output Flyback Converter

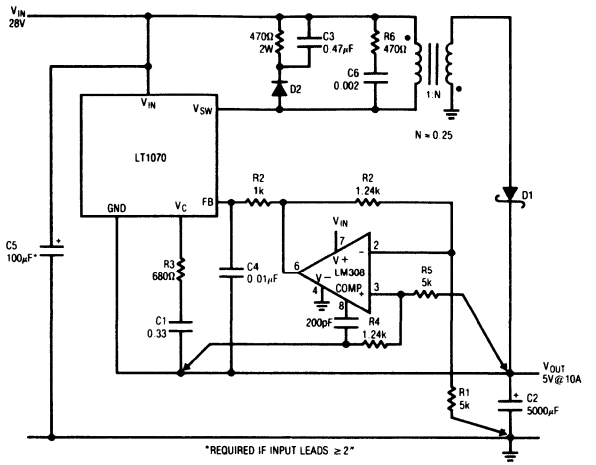


Forward Converter



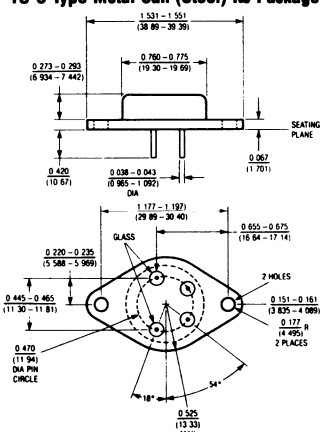
TYPICAL APPLICATIONS

Positive Current Boosted Buck Converter

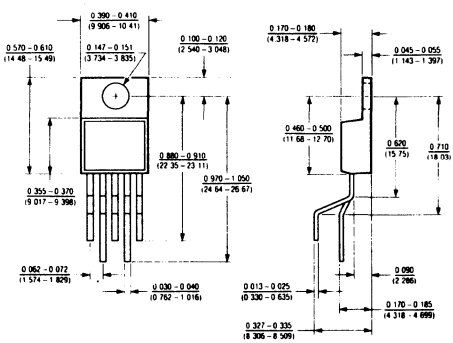


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

TO-3 Type Metal Can (Steel) KJ Package



TO-220 Type Plastic KV Package



	T_{JMAX}	θ_{JC}	θ_{JA}
LT1070MKJ, LT1070HVMKJ	150°C	2°C/W	35°C/W
LT1070CKJ, LT1070HVCKJ	100°C	2°C/W	35°C/W
LT1070CKV, LT1070HVCKV	100°C	2°C/W	75°C/W

JULY 1988

FEATURES

- Three Terminal Adjustable
- Output Current of 5 A
- Operates Down to 1V Dropout
- Dropout Voltage at Multiple Current Levels
- 0.015% Line Regulation
- 0.01% Load Regulation
- 100% Thermal Limit Burn-In

APPLICATIONS

- High Efficiency Linear Regulators
- Post Regulators for Switching Supplies
- Constant Current Regulators
- Battery Chargers

DESCRIPTION

The LT1084 positive adjustable regulator is designed to provide 5 A with higher efficiency than currently available devices. All internal circuitry is designed to operate down to 1V input to output differential and the dropout voltage is fully specified as a function of load current. Dropout is at a maximum of 1.5V at maximum output current, decreasing at lower load currents. On-chip trimming adjusts the reference voltage to 1%. Current limit is also trimmed, minimizing the stress on both the regulator and power source circuitry under overload conditions.

The LT1084 is pin compatible with older 3 terminal regulators. A 10μF output capacitor is required on this new device; however, this is usually included in most regulator designs.

Unlike PNP regulators, where up to 10% of the output current is wasted as quiescent current, the LT1084 quiescent current flows into the load, increasing efficiency.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally Limited
Input to Output Voltage Differential
- "M" Grades 35V
- "C" Grades 30V

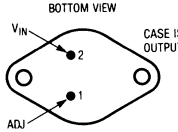
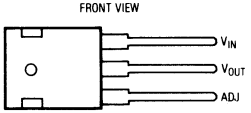
Operating Junction Temperature Range
- "M" Grades
  - Control Section ..... –55°C to 150°C
  - Power Transistor ..... –55°C to 200°C
- "C" Grades
  - Control Section ..... 0°C to 125°C
  - Power Transistor ..... 0°C to 150°C

Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PRECONDITIONING

100% Thermal Limit Burn-In

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
BOTTOM VIEW  KA PACKAGE TO-3 METAL CAN	LT1084CKA LT1084MKA
FRONT VIEW  KK PACKAGE TO-3P PLASTIC	LT1084CKK

ELECTRICAL CHARACTERISTICS (See Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage	I_{OUT} = 10mA, T_j = 25°C, ($V_{IN} - V_{OUT}$) = 3V (KA Package Only) 10mA≤I_{OUT}≤$I_{FULL\ LOAD}$		1.238	1.250	1.262	V
	1.5V≤($V_{IN} - V_{OUT}$)≤25V(Note 3)	●	1.225	1.250	1.270	V
Line Regulation	I_{LOAD} = 10mA, 1.5V≤($V_{IN} - V_{OUT}$)≤15V, T_j = 25°C			0.015	0.2	%
		●		0.035	0.2	%
	M Grade 15V≤($V_{IN} - V_{OUT}$)≤35V	●		0.05	0.5	%
	C Grade 15V≤($V_{IN} - V_{OUT}$)≤30V (Notes 1,2)	●		0.05	0.5	%
Load Regulation	($V_{IN} - V_{OUT}$) = 3V 10mA≤I_{OUT}≤$I_{FULL\ LOAD}$ T_j = 25°C(Notes 1,2,3)			0.1	0.3	%
		●		0.2	0.4	%
Dropout Voltage	ΔV_{REF} = 1%, I_{OUT} = $I_{FULL\ LOAD}$,(Note 4)	●		1.3	1.5	V
Current Limit LT1084	($V_{IN} - V_{OUT}$) = 5V	●	5.5	6.5		A
	($V_{IN} - V_{OUT}$) = 25V	●	0.3	0.6		A
Minimum Load Current	($V_{IN} - V_{OUT}$) = 25V	●		5	10	mA
Thermal Regulation LT1084	T_A = 25°C, 30ms pulse			0.003	0.015	%/W
Ripple Rejection	f = 120Hz C_{ADJ} = 25μF, C_{OUT} = 25μF Tantalum I_{OUT} = $I_{FULL\ LOAD}$, ($V_{IN} - V_{OUT}$) = 3V	●	60	75		dB
Adjust Pin Current	T_j = 25°C			55		μA
		●			120	μA
Adjust Pin Current Change	10mA≤I_{OUT}≤$I_{FULL\ LOAD}$ 1.5V≤($V_{IN} - V_{OUT}$)≤25V	●		0.2	5	μA
Temperature Stability		●		0.5		%
Long Term Stability	T_A = 125°C, 1000 Hrs.			0.3	1	%
RMS Output Noise (% of V_{OUT})	T_A = 25°C 10Hz = ≤f≤10kHz			0.003		%
Thermal Resistance Junction to Case LT1084	KA Package: Control Circuitry/Power Transistor				0.75/2.3	°C/W
	KK Package: Control Circuitry/Power Transistor				0.65/2.3	°C/W

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.

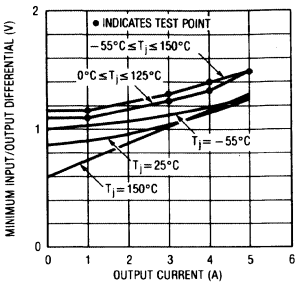
Note 2: Line and load regulation are specified up to the maximum power dissipation, (45W). Power dissipation is determined by the input/output differential and the output current. Maximum power dissipation may not be available over the full input/output voltage range.

Note 3: $I_{FULL\ LOAD}$ is defined in the current limit curves. $I_{FULL\ LOAD}$ curve is defined as the minimum value of current limit as a function of input to output voltage. Note that the 45W power dissipation is only achievable over a limited range of input to output voltage.

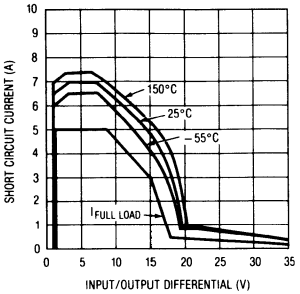
Note 4: Dropout voltage is specified over the full output current range of the device. Test points and limits are shown on the Dropout Voltage curve.

TYPICAL PERFORMANCE CHARACTERISTICS

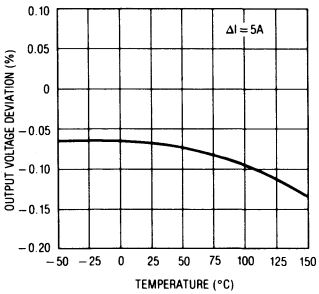
Dropout Voltage



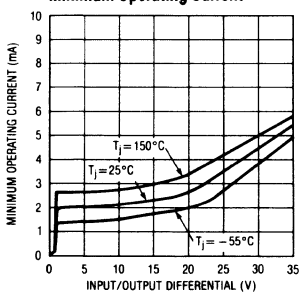
Short Circuit Current



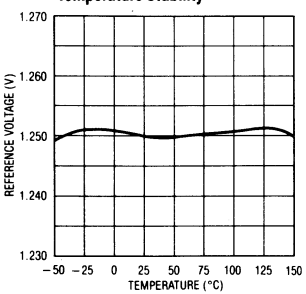
Load Regulation



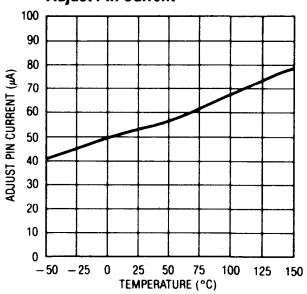
Minimum Operating Current



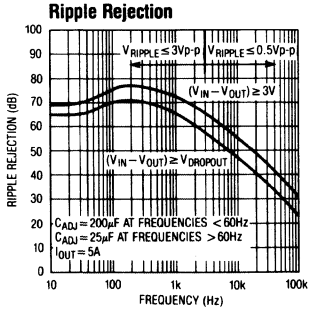
Temperature Stability



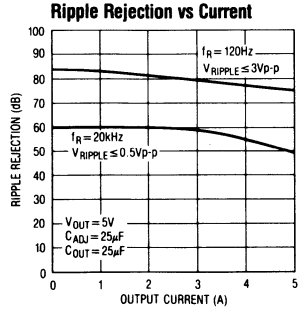
Adjust Pin Current



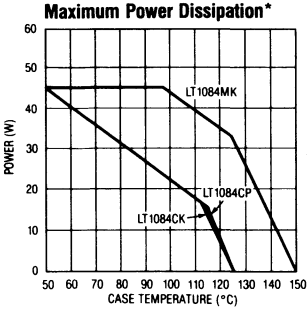
Ripple Rejection



Ripple Rejection vs Current



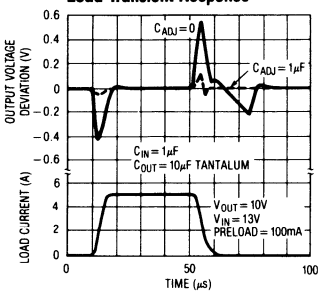
Maximum Power Dissipation*



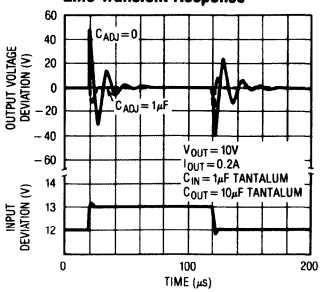
*AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

TYPICAL PERFORMANCE CHARACTERISTICS

Load Transient Response



Line Transient Response



APPLICATION HINTS

The three terminal adjustable regulator is easy to use and has all the protection features that are expected in high performance voltage regulators. It is short circuit protected, has safe area protection as well as thermal shutdown to turn off the regulator should the temperature exceed about 165°C.

This regulator is pin compatible with older three terminal adjustable devices, offers lower dropout voltage and more precise reference tolerance. Further, the reference stability with temperature is improved over older types of regulators. The only circuit difference between using the LT1084 and older regulators is that they require an output capacitor for stability.

Stability

The circuit design used in the LT1084 requires the use of an output capacitor as part of the device frequency compensation. For all operating conditions, the addition of 150μF aluminum electrolytic or a 22μF solid tantalum on the output will ensure stability. Normally, capacitors much smaller than this can be used with the LT1084. Many different types of capacitors with widely varying characteristics are available. These capacitors differ in capacitor tolerance (sometimes ranging up to ±100%), equivalent series resistance, and capacitance temperature coefficient. The 150μF or 22μF values given will ensure stability.

When the adjustment terminal is bypassed to improve the ripple rejection, the requirement for an output capacitor increases. The values of 22μF tantalum or 150μF aluminum cover all cases of bypassing the adjustment terminal. Without bypassing the adjustment terminal, smaller capacitors can be used with equally good results and the table below shows approximately what size capacitors are needed to ensure stability.

Recommended Capacitor Values

Input	Output	Adjustment
10μF	10μF Tantalum, 50μF Aluminum	None
10μF	22μF Tantalum, 150μF Aluminum	20μF

Normally, capacitor values on the order of 100μF are used in the output of many regulators to ensure good transient response with heavy load current changes. Output capacitance can be increased without limit and larger values of output capacitor further improve stability and transient response of the LT1084 regulator.

APPLICATION HINTS

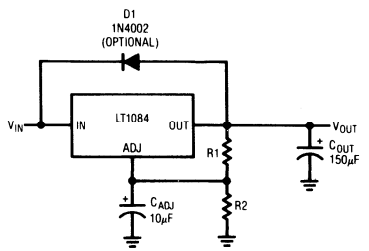
Another possible stability problem that can occur in monolithic IC regulators is current limit oscillations. These can occur because, in current limit, the safe area protection exhibits a negative impedance. The safe area protection decreases the current limit as the input-to-output voltage increases. That is the equivalent of having a negative resistance since increasing voltage causes current to decrease. Negative resistance during current limit is not unique to the LT1084 and has been present on all power IC regulators. The value of the negative resistance is a function of how fast the current limit is folded back as input-to-output voltage increases. This negative resistance can react with capacitors or inductors on the input to cause oscillation during current limiting. Depending on the value of series resistance, the overall circuitry may end up unstable. Since this is a system problem, it is not necessarily easy to solve; however it does not cause any problems with the IC regulator and can usually be ignored.

Protection Diodes

In normal operation, the LT1084 does not need any protection diodes. Older adjustable regulators required protection diodes between the adjustment pin and the output and from the output to the input to prevent overstressing the die. The internal current paths on the LT1084 adjustment pin is limited by internal resistors. Therefore, even with capacitors on the adjustment pin, no protection diode is needed to ensure device safety under short circuit conditions.

Diodes between input and output are usually not needed. The internal diode between the input and the output pins of the LT1084 can handle microsecond surge currents of 50A to 100A. Even with large output capacitances, it is very difficult to get those values of surge currents in normal operations. Only with high value of output capacitors, such as 1000μF to 5000μF and with the input pin instantaneously shorted to ground, can damage occur. A crowbar circuit at the input of the LT1084 can generate those kinds of currents, and a diode from output to input is then recommended. Normal power supply cycling or even plugging and unplugging in the system will not generate current large enough to do any damage.

The adjustment pin can be driven on a transient basis ±25V, with respect to the output without any device degradation. Of course, as with any IC regulator, exceeding the maximum input to output voltage differential causes the internal transistors to break down and none of the protection circuitry is functional.



Overload Recovery

Like any of the IC power regulators, the LT1084 has safe area protection. The safe area protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The LT1084 protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During the start-up, as the input voltage is rising, the input-to-output voltage differential remains small, allowing the regulator to supply large output currents. With high input voltage, a problem can occur wherein removal of an output short will not allow the output voltage to recover. Older regulators, such as the 7800 series, also exhibited this phenomenon, so it is not unique to the LT1084.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low, such as immediately after a removal of a short. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the power supply may need to be cycled down to zero and brought up again to make the output recover.

APPLICATION HINTS

Ripple Rejection

The typical curves for ripple rejection reflect values for a bypassed adjustment pin. This curve will be true for all values of output voltage. For proper bypassing, and ripple rejection approaching the values shown, the impedance of the adjust pin capacitor, at the ripple frequency should equal the value of R1, (normally 100Ω-120Ω). The size of the required adjust pin capacitor is a function of the input ripple frequency. At 120Hz the adjust pin capacitor should be 13μF if R1 = 100Ω. At 10kHz only 0.16μF is needed.

For circuits without an adjust pin bypass capacitor, the ripple rejection will be a function of output voltage. The output ripple will increase directly as a ratio of the output voltage to the reference voltage (V_{OUT}/V_{REF}). For example, with the output voltage equal to 5V, and no adjust pin capacitor, the output ripple will be higher by the ratio of 5V/1.25V or 4 times larger. Ripple rejection will be degraded by 12dB from the value shown on the typical curve.

Output Voltage

The LT1084 develops a 1.25V reference voltage between the output and the adjust terminal (see Figure 1). By placing a resistor, R1, between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is the specified minimum load current of 10mA. Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored.

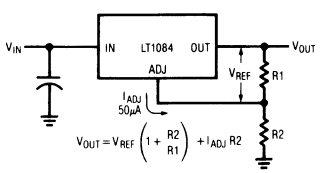


Figure 1. Basic Adjustable Regulator

Load Regulation

Because the LT1084 is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negatived side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider, (R1), is connected *directly* to the case *not to the load.* This is illustrated in Figure 2. If R1 were connected to the load, the effective resistance between the regulator and the load would be

$$R_p \times \left(\frac{R2 + R1}{R1}\right), R_p = \text{Parasitic Line Resistance.}$$

Connected as shown, R_p is not multiplied by the divider ratio. R_p is about 0.004Ω per foot using 16 gauge wire. This translates to 4mV/ft at 1A load current, so it is important to keep the positive lead between regulator and load as short as possible, and use large wire or PC board traces.

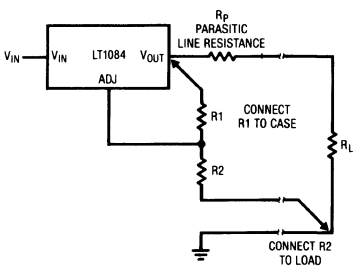


Figure 2. Connections for Best Load Regulation

Thermal Considerations

The LT1084 regulator has internal power and thermal limiting circuitry designed to protect the device under overload conditions. For continuous normal load conditions however, maximum junction temperature ratings must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. This includes junction to case, case to heat sink interface, and heat sink resistance itself. New thermal resistance specifications have been developed to more accurately reflect

APPLICATION HINTS

device temperature and ensure safe operating temperatures. The data section for these new regulators provides a separate thermal resistance and maximum junction temperature for both the *Control Section* and the *Power Transistor.* Previous regulators, with a single junction to case thermal resistance specification, used an average of the two values provided here and therefore could allow excessive junction temperatures under certain conditions of ambient temperature and heat sink resistance. To avoid this possibility, calculations should be made for both sections to ensure that both thermal limits are met.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly below the die. This is the lowest resistance path for heat flow. Proper mounting is required to ensure the best possible thermal flow from this area of the package to the heat sink. Thermal compound at the case-to-heat-sink interface is strongly recommended. If the case of the device must be electrically isolated, a thermally conductive spacer can be used, as long as its added contribution to thermal resistance is considered. Note that the case of all devices in this series is electrically connected to the output.

For example, using a LT1084CKA (TO-3, Commercial) and assuming:

V_{IN} (max continuous) = 9V, V_{OUT} = 5V, I_{OUT} = 6A,
$T_{AMBIENT}$ = 75°C, $\theta_{HEAT\ SINK}$ = 1°C/W,

$\theta_{CASE\text{-}TO\text{-}HEAT\text{-}SINK}$ = 0.2°C/W for KA package with thermal compound.

Power dissipation under these conditions is equal to:

$$P_D = (V_{IN} - V_{OUT})(I_{OUT}) = 24W$$

Junction temperature will be equal to:

$$T_j = T_{AMBIENT} + P_D(\theta_{HEAT\text{-}SINK} + \theta_{CASE\text{-}TO\text{-}HEAT\text{-}SINK} + \theta_{jc})$$

For the Control Section:

$T_j = 75°C + 24W(1°C/W + 0.2°C/W + 0.6°C/W) = 118°C$
$118°C < 125°C = T_{jmax}$ (Control Section Commercial Range)

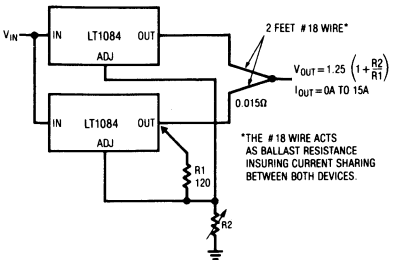
For the Power Transistor:

$T_j = 75°C + 24W(1°C/W + 0.2°C/W + 1.6°C/W) = 142°C$
$142°C < 150°C = T_{jmax}$ (Power Transistor Commercial Range)

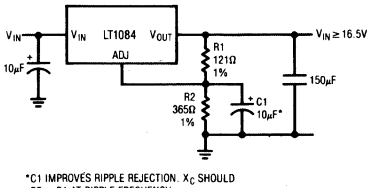
In both cases the junction temperature is below the maximum rating for the respective sections, ensuring reliable operation.

TYPICAL APPLICATIONS

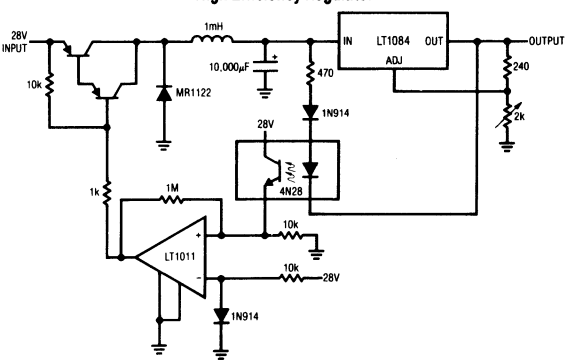
Paralleling Regulators



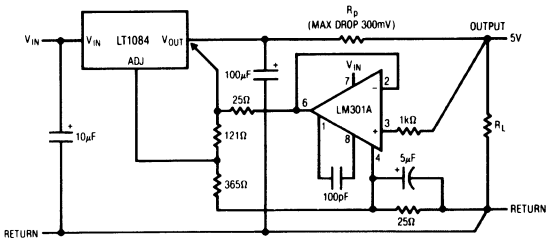
Improving Ripple Rejection



High Efficiency Regulator

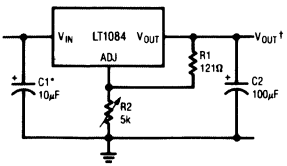


Remote Sensing



TYPICAL APPLICATIONS

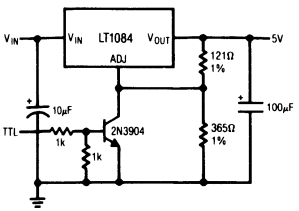
1.2V–15V Adjustable Regulator



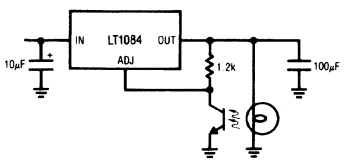
*NEEDED IF DEVICE IS FAR FROM FILTER CAPACITORS

†$V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right)$

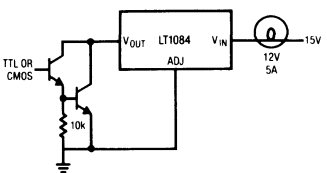
5V Regulator with Shutdown



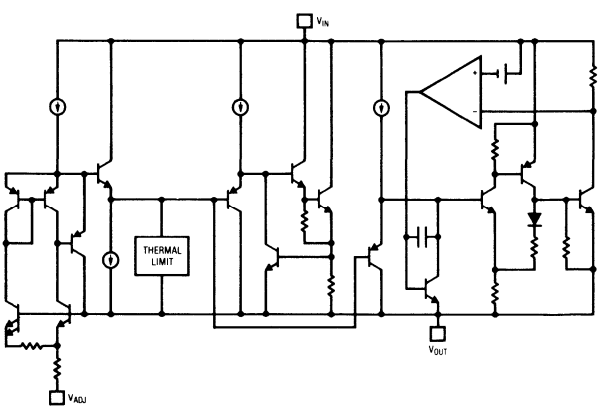
Automatic Light Control



Protected High Current Lamp Driver

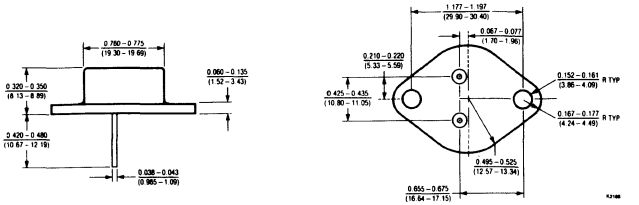


BLOCK DIAGRAM

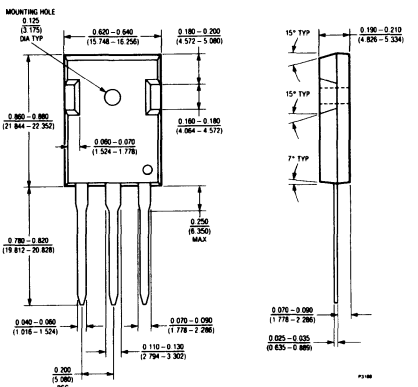


PACKAGE DESCRIPTIONS Dimensions in inches (millimeters) unless otherwise noted.

KA Package
TO-3 Metal Can



KK Package
TO-3P Plastic



Voltage Regulators

6

TEXAS INSTRUMENTS

MAY 1987

FEATURES

- Plug-In Compatible with 7660 with These Additional Features:
  - Operation to 9V, with No External Diode, Over Full Temperature Range
  - Boost Pin (Pin 1) for Higher Switching Frequency
  - Lower Quiescent Power
  - Efficient Voltage Doubler
- 200μA *Max.* No Load Supply Current at 5V
- 97% *Min.* Open Circuit Voltage Conversion Efficiency
- 95% *Min.* Power Conversion Efficiency
- Wide Operating Supply Voltage Range, 1.5V to 9V
- Easy to Use
- Commercial Device Operates Over −40°C to 85°C Temperature Range

APPLICATIONS

- Conversion of +5V to ±5V Supplies
- Precise Voltage Division, $V_{OUT} = V_{IN}/2 \pm 20ppm$
- Voltage Multiplication, $V_{OUT} = \pm nV_{IN}$
- Supply Splitter, $V_{OUT} = \pm V_S/2$

DESCRIPTION

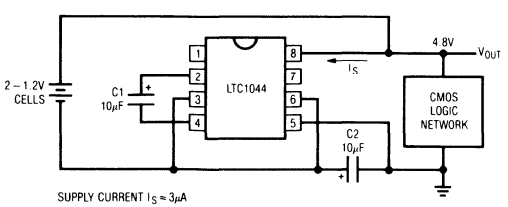
The LTC1044 is a monolithic CMOS switched capacitor voltage converter which is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. The LTC1044 provides several voltage conversion functions: the input voltage can be inverted ($V_{OUT} = -V_{IN}$), doubled ($V_{OUT} = 2V_{IN}$), divided ($V_{OUT} = V_{IN}/2$) or multiplied ($V_{OUT} = \pm nV_{IN}$).

Designed to be pin-for-pin and functionally compatible with the popular 7660, the LTC1044 provides significant features and improvements over earlier 7660 designs. These improvements include: full 1.5V to 9V supply operation over the entire operating temperature range, without the need for external protection diodes; 2½ times lower quiescent current for greater power conversion efficiency; and a "boost" function which is available to raise the internal oscillator frequency to optimize performance in specific applications.

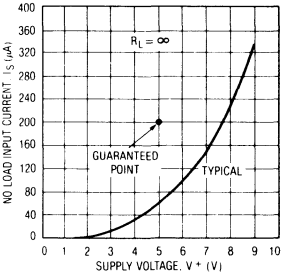
Although the LTC1044 provides significant design and performance advantages over the earlier 7660 device, it still maintains its compatibility with existing 7660 designs.

LTCMOS™ is a trademark of Linear Technology Corp.

Generating CMOS Logic Supply from 2 Mercury Batteries



Supply Current vs Supply Voltage

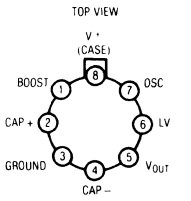


ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage 9.5V
Input Voltage on Pins 1, 6 and 7
(Note 2) ..... $-0.3V \leq V_{IN} \leq V^+ + 0.3V$
Current into Pin 6 ..... 20μA
Output Short Circuit Duration
($V^+ \leq 5.5V$) ..... Continuous
Operating Temperature Range
LTC1044C ..... $-40°C \leq T_A \leq 85°C$
LTC1044M ..... $-55°C \leq T_A \leq 125°C$
Storage Temperature Range..... $-65°C$ to $+150°C$
Lead Temperature (Soldering, 10 sec.) .....300°C

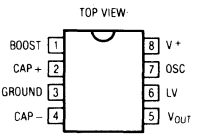
PACKAGE/ORDER INFORMATION



METAL CAN L PACKAGE

ORDER PART NUMBER

LTC1044CL
LTC1044ML



HERMETIC DIP JG PACKAGE
PLASTIC DIP P PACKAGE

LTC1044CJG
LTC1044CP
LTC1044MJG

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $T_A = 25°C$, Test Circuit Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC1044M MIN	LTC1044M TYP	LTC1044M MAX	LTC1044C MIN	LTC1044C TYP	LTC1044C MAX	UNITS
I_S	Supply Current	$R_L = \infty$, Pins 1 and 7 No Connection			60	200		60	200	μA
		$R_L = \infty$, Pins 1 and 7 $V^+ = 3V$			20			20		μA
V^+_L	Minimum Supply Voltage	$R_L = 10k$	●	1.5			1.5			V
V^+_H	Maximum Supply Voltage	$R_L = 10k$ (Note 3)	●			9			9	V
R_{OUT}	Output Resistance	$I_L = 20mA$, $f_{OSC} = 5kHz$				100			100	Ω
			●			150			130	Ω
		$V^+ = 2V$, $I_L = 3mA$, $f_{OSC} = 1kHz$	●			400			325	Ω
f_{OSC}	Oscillator Frequency	$C_{OSC} = 1pF$ (Note 4)								
		$V^+ = 5V$	●	5			5			kHz
		$V^+ = 2V$	●	1			1			kHz
P_{EFF}	Power Efficiency	$R_L = 5k\Omega$, $f_{OSC} = 5kHz$		95	98		95	98		%
V_{OUTEFF}	Voltage Conversion Efficiency	$R_L = \infty$		97	99.9		97	99.9		%
I_{OSC}	Oscillator Sink or Source Current	$V_{OSC} = 0V$ or V^+								
		Pin 1 = 0V	●			3			3	μA
		Pin 1 = V^+	●			20			20	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

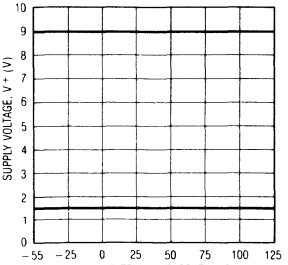
Note 2: Connecting any input terminal to voltages greater than V^+ or less than ground may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to power-up of the LTC1044.

Note 3: The LTC1044 operates with alkaline, mercury or NiCad 9V batteries, even when the initial battery voltage is slightly higher than 9.0V.

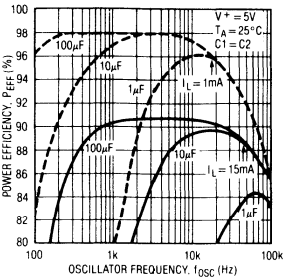
Note 4: f_{OSC} is tested with $C_{OSC} = 100pF$ to minimize the effects of test fixture capacitance loading. The 1pF frequency is correlated to this 100pF test point, and is intended to simulate the capacitance at pin 7 when the device is plugged into a test socket and no external capacitor is used.

TYPICAL PERFORMANCE CHARACTERISTICS (Using Test Circuit Shown in Figure 1)

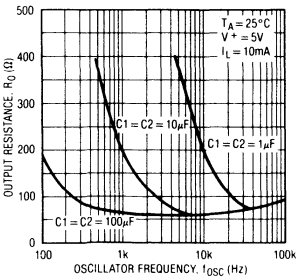
Operating Voltage Range vs Temperature



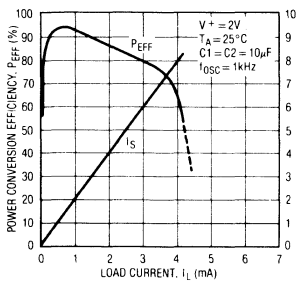
Power Efficiency vs Oscillator Frequency



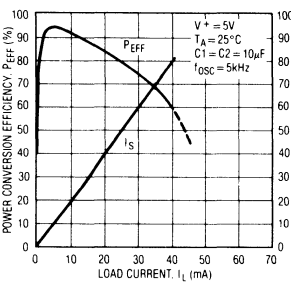
Output Resistance vs Oscillator Frequency



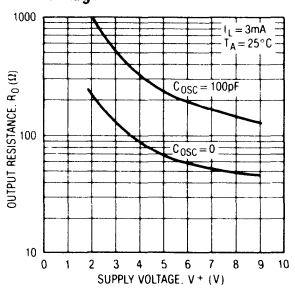
Power Conversion Efficiency vs Load Current for V+ = 2V



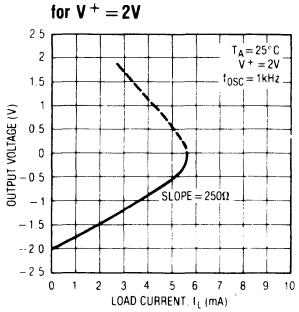
Power Conversion Efficiency vs Load Current for V+ = 5V



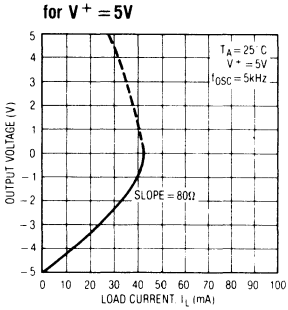
Output Resistance vs Supply Voltage



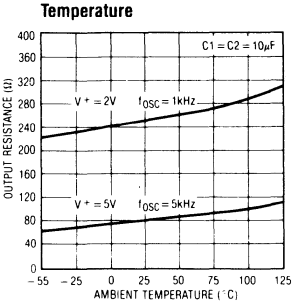
Output Voltage vs Load Current for V+ = 2V



Output Voltage vs Load Current for V+ = 5V

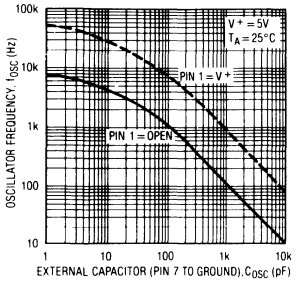


Output Resistance vs Temperature

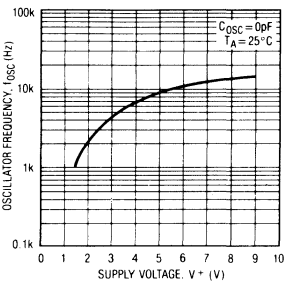


TYPICAL PERFORMANCE CHARACTERISTICS (Using Test Circuit Shown in Figure 1)

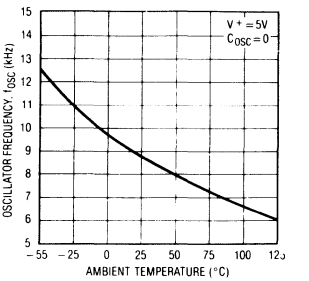
Oscillator Frequency as a Function of C_{OSC}



Oscillator Frequency vs Supply Voltage



Oscillator Frequency vs Temperature



TEST CIRCUIT

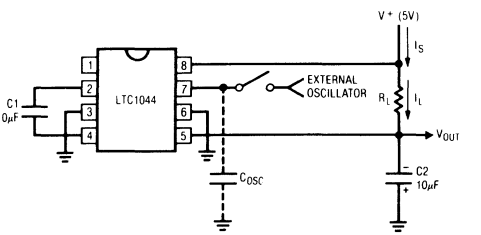


Figure 1

APPLICATIONS INFORMATION

Theory of Operation

To understand the theory of operation of the LTC1044, a review of a basic switched capacitor building block is helpful.

In Figure 2, when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be $q1 = C1V1$. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time, the charge on C1 is $q2 = C1V2$. Note that charge has been transferred from the source, V1, to the output, V2. The amount of charge transferred is:

$$\Delta q = q1 - q2 = C1(V1 - V2).$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is:

$$I = f \times \Delta q = f \times C1(V1 - V2).$$

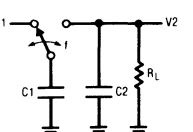


Figure 2. Switched Capacitor Building Block

APPLICATIONS INFORMATION

Rewriting in terms of voltage and impedance equivalence,

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}}.$$

A new variable, R_{EQUIV}, has been defined such that $R_{EQUIV} = 1/fC1$. Thus, the equivalent circuit for the switched capacitor network is as shown in Figure 3.

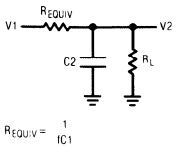


Figure 3. Switched Capacitor Equivalent Circuit

Examination of Figure 4 shows that the LTC1044 has the same switching action as the basic switched capacitor building block. With the addition of finite switch on-resistance and output voltage ripple, the simple theory, although not exact, provides an intuitive feel for how the device works.

For example, if you examine power conversion efficiency as a function of frequency (see typical curve), this simple theory will explain how the LTC1044 behaves. The loss, and hence the efficiency, is set by the output impedance. As frequency is decreased, the output impedance will eventually be dominated by the 1/fC1 term and power efficiency will drop. The typical curves for power efficiency versus frequency show this effect for various capacitor values.

Note also that power efficiency decreases as frequency goes up. This is caused by internal switching losses which occur due to some finite charge being lost on each switching cycle. This charge loss per unit cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency this loss becomes significant and the power efficiency starts to decrease.

LV (Pin 6)

The internal logic of the LTC1044 runs between V^+ and LV (pin 6). For V^+ greater than or equal to 3V, an internal switch shorts LV to GND (pin 3). For V^+ less than 3V, the LV pin should be tied to GND. For V^+ greater than or equal to 3V, the LV pin can be tied to GND or left floating.

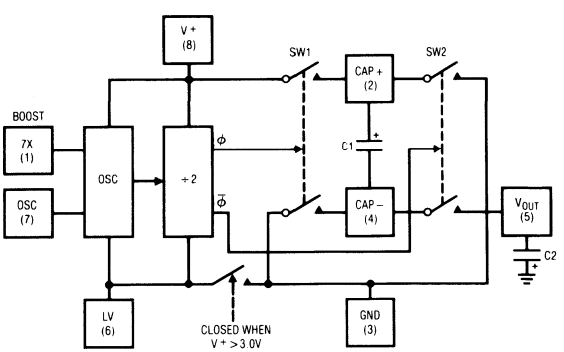


Figure 4. LTC1044 Switched Capacitor Voltage Converter Block Diagram

APPLICATIONS INFORMATION

OSC (Pin 7) and Boost (Pin 1)

The switching frequency can be raised, lowered or driven from an external source. Figure 5 shows a functional diagram of the oscillator circuit.

By connecting the boost pin (pin 1) to V^+, the charge and discharge current is increased and, hence, the frequency is increased by approximately 7 times. Increasing the frequency will decrease output impedance and ripple for higher load currents.

Loading pin 7 with more capacitance will lower the frequency. Using the boost (pin 1) in conjunction with external capacitance on pin 7 allows user selection of the frequency over a wide range.

Driving the LTC1044 from an external frequency source can be easily achieved by driving pin 7 and leaving the boost pin open, as shown in Figure 6. The output current from pin 7 is small, typically 0.5μA, so a logic gate is capable of driving this current. The choice of using a CMOS logic gate is best because it can operate over a wide supply voltage range (3V to 15V) and has enough voltage swing to drive the internal Schmitt trigger shown in Figure 5. For 5V applications, a TTL logic gate can be used by simply adding an external pull-up resistor (see Figure 6).

External Diode (D_X)

Previous circuits of this type have required a diode between V_{OUT} (pin 5) and the external capacitor, C2, for voltages above 6.5V (5V for military temperature range). Because of improvements which have been made in the LTC1044 circuit design and Linear Technology's silicon gate CMOS process, this diode is no longer required. The LTC1044 will operate from 1.5V to 9V, without the protection diode, over all temperature ranges.

It should, however, be noted that the LTC1044 will operate without any problems in existing 7660 designs which use the protection diode, as long as the maximum operating voltage (V^+) of 9V is not exceeded.

Capacitor Selection

External capacitors C1 and C2 are not critical. Matching is not required, nor do they have to be high quality or tight tolerance. Aluminum or tantalum electrolytics are excellent choices, with cost and size being the only consideration.

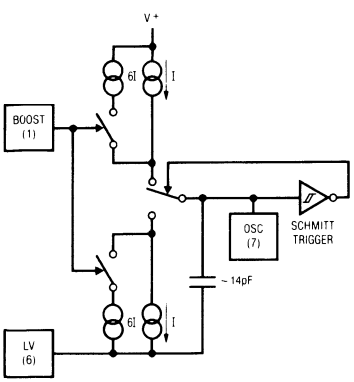


Figure 5. Oscillator

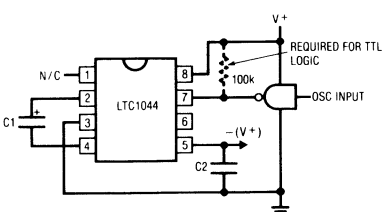


Figure 6. External Clocking

TYPICAL APPLICATIONS

Negative Voltage Converter

Figure 7 shows a typical connection which will provide a negative supply from an available positive supply. This circuit operates over full temperature and power supply ranges *without* the need of any external diodes. The LV pin (pin 6) is shown grounded, but for $V^+ \geq 3V$ it may be "floated", since LV is internally switched to ground (pin 3) for $V^+ \geq 3V$.

The output voltage (pin 5) characteristics of the circuit are those of a nearly ideal voltage source in series with an 80Ω resistor. The 80Ω output impedance is composed of two terms: 1) the equivalent switched capacitor resistance (see Theory of Operation) and 2) a term related to the on-resistance of the MOS switches.

At an oscillator frequency of 10kHz and $C1 = 10\mu F$, the first term is:

$$R_{EQUIV} = \frac{1}{(f_{OSC}/2) \times C1} =$$

$$\frac{1}{5 \times 10^3 \times 10 \times 10^{-6}} = 20\Omega.$$

Notice that the above equation for R_{EQUIV} is *not* a capacitive reactance equation ($X_C = 1/\omega C$) and does not contain a 2π term.

The exact expression for output impedance is extremely complex, but the dominant effect of the capacitor is clearly shown on the typical curves of output impedance and power efficiency versus frequency. For $C1 = C2 = 10\mu F$, the output impedance goes from 60Ω at $f_{OSC} = 10kHz$ to 200Ω at $f_{OSC} = 1kHz$. As the $1/fC$ term becomes large compared to the switch on-resistance term, the output resistance is determined by $1/fC$ only.

Voltage Doubling

Figure 8 shows two methods of voltage doubling. In Figure 8a doubling is achieved by simply rearranging the connection of the two external capacitors. When the input voltage is less than 3V, an external 1MΩ resistor is required to ensure the oscillator will start. It is not required for higher input voltages.

In this application the ground input (pin 3) is taken above V^+ (pin 8) during turn-on, making it prone to latch-up. The latch-up is not destructive but simply prevents the circuit from doubling. Resistor R1 is added to eliminate the problem. In most cases 200Ω is sufficient. It may be necessary in a particular application to increase this value to guarantee start-up.

The voltage drop across R1 is : $V_{R1} = 2 \times I_{OUT} \times R1$. If this voltage exceeds two diode drops (1.4V for silicon, 0.8V for Schottky), the circuit in Figure 8a is recommended. This circuit will never have a start-up problem.

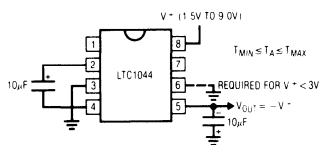
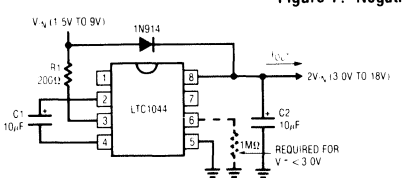
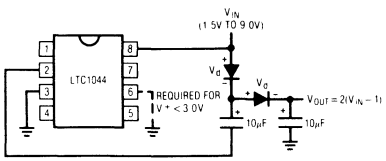


Figure 7. Negative Voltage Converter



(a)



(b)

Figure 8. Voltage Doubler

TYPICAL APPLICATIONS

Ultra Precision Voltage Divider

An ultra precision voltage divider is shown in Figure 9. To achieve the 0.0002% accuracy indicated, the load current should be kept below 100nA. However, with a slight loss in accuracy, the load current can be increased.

Battery Splitter

A common need in many systems is to obtain (+) and (−) supplies from a single battery or single power supply system. Where current requirements are small, the circuit shown in Figure 10 is a simple solution. It provides symmetrical ± output voltages, both equal to one half the input voltage. The output voltages are both referenced to pin 3 (output common). If the input voltage between pin 8 and pin 5 is less than 6V, pin 6 should also be connected to pin 3, as shown by the dashed line.

Paralleling for Lower Output Resistance

Additional flexibility of the LTC1044 is shown in Figures 11, 12 and 13.

Figure 11 shows two LTC1044s connected in parallel to provide a lower effective output resistance. If, however, the output resistance is dominated by 1/fC1, increasing the capacitor size (C1) or increasing the frequency will be of more benefit than the paralleling circuit shown.

Figures 12 and 13 make use of "stacking" two LTC1044s to provide even higher voltages. In Figure 12, a negative voltage doubler or tripler can be achieved, depending upon how pin 8 of the second LTC1044 is connected, as shown schematically by the switch. Figure 13 indicates a similar circuit which can be used to obtain positive tripling, or even quadrupling (the doubler circuit appears in Figure 8a. In both of these circuits, the available output current will be dictated/decreased by the product of the individual power conversion efficiencies and the voltage step-up ratio.

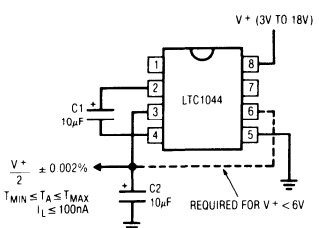


Figure 9. Ultra Precision Voltage Divider

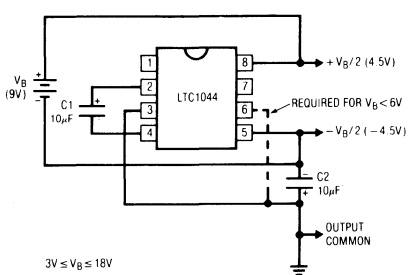
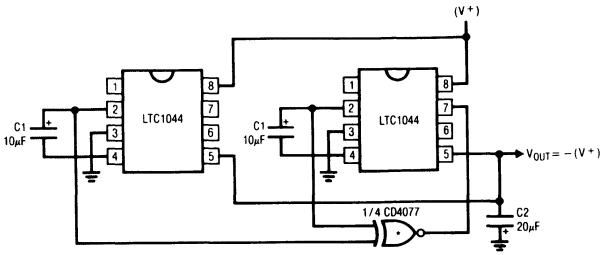


Figure 10. Battery Splitter

TYPICAL APPLICATIONS



*THE EXCLUSIVE NOR GATE SYNCHRONIZES BOTH LTC1044s TO MINIMIZE RIPPLE

Figure 11. Paralleling for Lower Output Resistance

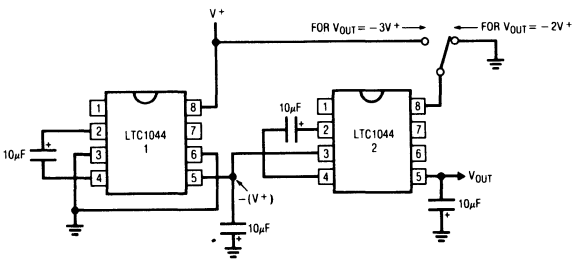
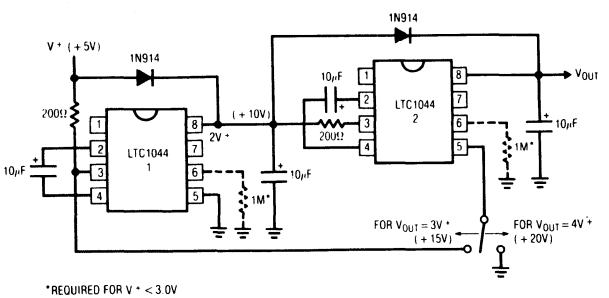


Figure 12. Stacking for Higher Voltage



*REQUIRED FOR V+ < 3.0V

Figure 13. Voltage Tripler/Quadrupler

TYPICAL APPLICATIONS

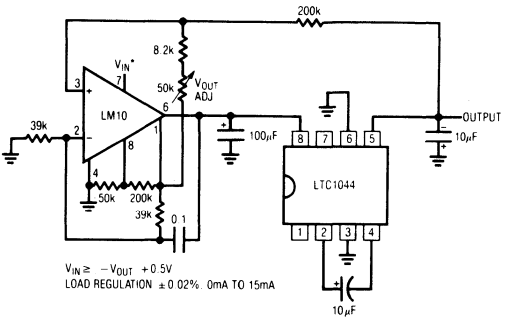


Figure 14. Low Output Impedance Voltage Converter

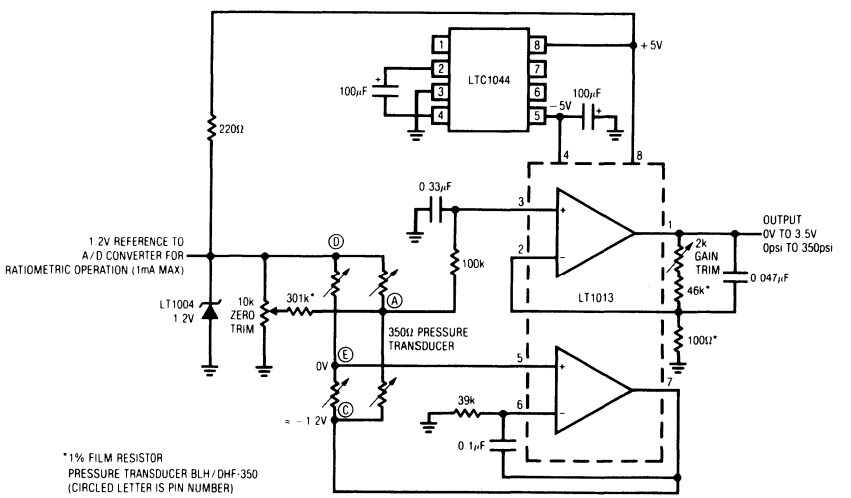


Figure 15. Single 5V Strain Gauge Bridge Signal Conditioner

TYPICAL APPLICATIONS

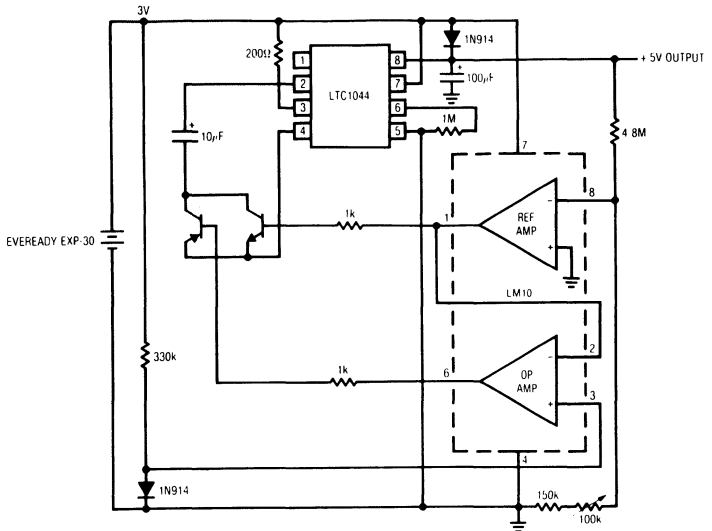


Figure 16. Regulated Output +3V to +5V Converter

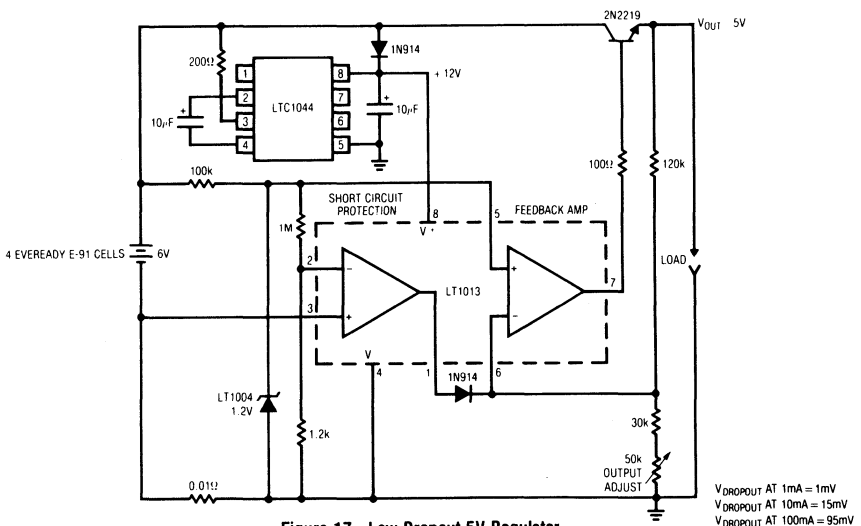
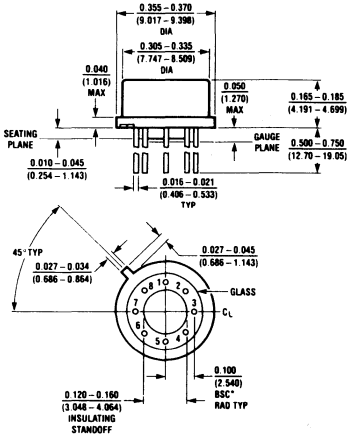


Figure 17. Low Dropout 5V Regulator

PACKAGE DESCRIPTION

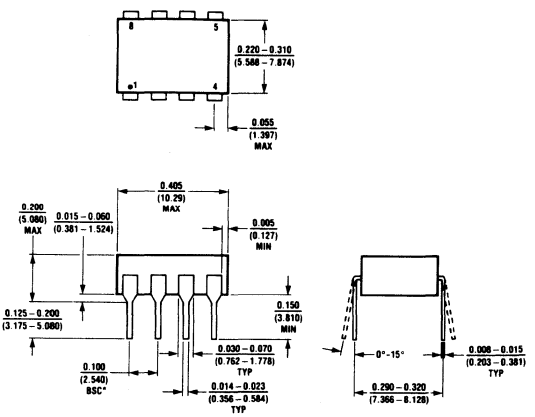
L Package
Metal Can



NOTE: DIMENSIONS IN INCHES (MILLIMETERS)

$T_j$max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

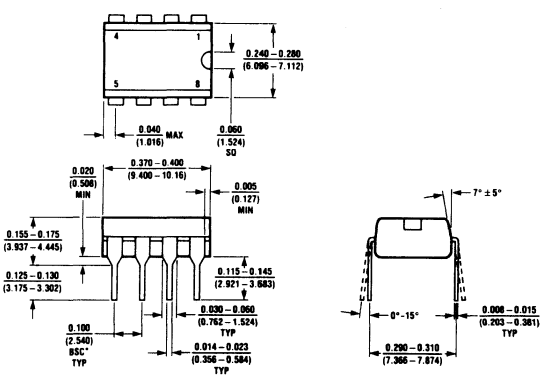
JG Package
8 Lead Hermetic DIP



NOTE: DIMENSIONS IN INCHES (MILLIMETERS) UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
150°C	100°C/W

P Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES (MILLIMETERS) UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

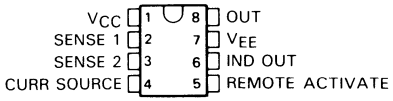
$T_j$max	θ_{ja}
100°C	130°C/W

TYPE MC3423
OVERVOLTAGE-SENSING CIRCUIT

D2439, APRIL 1978 – REVISED JANUARY 1983

- **Separate Outputs for "Crowbar" and Logic Circuitry**
- **Programmable Time Delay to Eliminate Noise Triggering**
- **TTL-Level Activation Isolated from Voltage-Sensing Inputs**
- **2.6-Volt Internal Voltage Reference with Temperature Coefficient Typically 0.08%/°C**

MC3423 . . . . . JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)

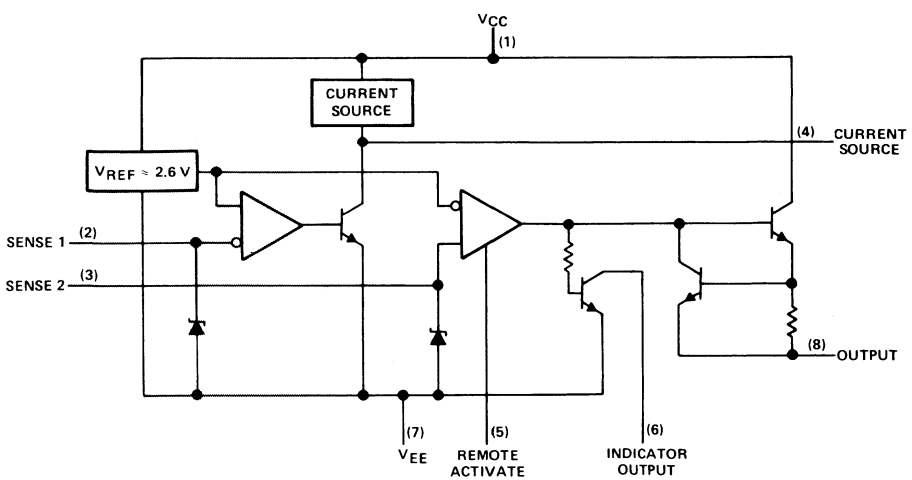


description

The MC3423 overvoltage-sensing circuit is designed to protect sensitive electronic circuitry by monitoring the supply rail and triggering an external "crowbar" SCR in the event of a voltage transient or loss of regulation. The protective mechanism may be activated by an overvoltage condition at the Sense 2 input or by application of a TTL high level to the Remote Activate terminal. Separate outputs are available to trigger the crowbar circuit and to provide a logic pulse to indicator or power supply control circuitry. The Sense 2 input provides a direct control of the output circuitry. The Sense 1 input controls an internal current source that may be utilized to implement a delayed trigger by connecting its output to an external capacitor and the Sense 2 input. This protects against false triggering due to noise at the Sense 1 input.

The MC3423 is characterized for operation from 0°C to 70°C.

functional block diagram



absolute maximum ratings

Supply voltage, V_{CC} (see Note 1) . . . . . 40 V
Sense 1 voltage . . . . . 6.5 V
Sense 2 voltage . . . . . 6.5 V
Remote activate input voltage . . . . . 7 V
Output current, I_O . . . . . 300 mA
Continuous dissipation at (or below) 25°C free-air temperature (see Note 2): JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are measured with respect to the V_{EE} terminal.
2. For operating above 25°C free-air temperature, refer to the Dissipation Derating Table. In the JG package, MC3423 chips are glass-mounted.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
JG (Glass-Mounted Chip)	825 mW	6.6 mW/°C	25°C
P	1000 mW	8 mW/°C	25°C

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	4.5	40	V
High-level input voltage, remote activate input	2		V
Low-level input voltage, remote activate input		0.5	V

electrical characteristics over operating free-air temperature range, V_{CC} = 5 V to 36 V (unless otherwise noted)

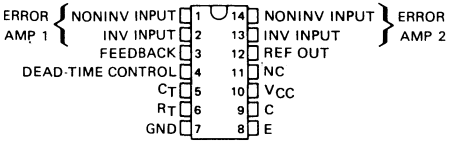
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	Remote Activate at 2 V, I_O = 100 mA	$V_{CC}-2.2$	$V_{CC}-1.8$		V
Indicator low-level output voltage	Remote Activate at 2 V, I_O = 1.6 mA		0.1	0.4	V
Threshold voltage of either sense input	T_A = 25°C	2.45	2.6	2.75	V
Temperature coefficient of input threshold voltage			0.06		%/°C
Source current (pin 4)	Sense 1 at 3 V, Pin 4 at 1.3 V	0.1	0.22	0.3	mA
High-level input current, Remote Activate input	V_{CC} = 5 V, V_I = 2 V		5	40	μA
Low-level input current, Remote Activate input	T_{CC} = 5 V, V_I = 0.8 V		−120	−180	μA
Supply current	Outputs open		6	10	mA
Propagation delay time, Remote Activate input to Output	T_A = 25°C		0.5		μs
Output current rate of rise	T_A = 25°C		400		mA/μs

TYPES MC35060, MC34060
PULSE-WIDTH-MODULATION CONTROL CIRCUITS

D2714, MARCH 1983

- Complete PWM Power Control Circuitry
- Uncommitted Output for 200-mA Sink or Source Current
- Variable Dead-Time Provides Control Over Total Range
- Internal Regulator Provides a Stable 5-V Reference Supply
- Circuit Architecture Provides Easy Synchronization
- Direct Replacements for Motorola MC35060 and MC34060

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



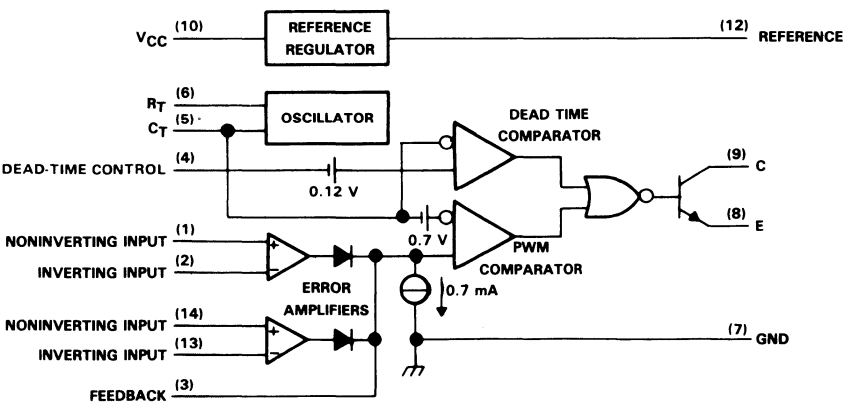
NC – No internal connections

description

The MC35060 and MC34060 incorporate on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, each of the devices contains an on-chip 5-volt regulator, two error amplifiers, an adjustable oscillator, and a dead-time control comparator. The uncommitted output transistor provides either common-emitter or emitter-follower output capability. The internal amplifiers exhibit a common-mode voltage range from −0.3 volt to V_{CC} − 2 volts. The dead-time control comparator has a fixed offset that provides approximately 5% dead time unless externally altered. The on-chip oscillator may be bypassed by terminating R_T (pin 6) to the reference output and providing a sawtooth input to C_T (pin 5), or it may be used to drive the common MC35060 or MC34060 circuitry and provide a sawtooth input for associated control circuitry in multiple rail power supplies.

The MC35060 is characterized for operation over the full military temperature range of −55°C to 125°C. The MC34060 is characterized for operation from 0°C to 70°C.

functional block diagram



All voltage and current values shown are nominal.

absolute maximum ratings over operation temperature range (unless otherwise noted)

	MC35060	MC34060	UNIT
Supply voltage, V_{CC} (see Note 1)	42	42	V
Amplifier input voltages	$V_{CC}+0.3$	$V_{CC}+0.3$	V
Collector output voltage	42	42	V
Collector output current	250	250	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1000	1000	mW
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package		260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Table. In the J package, MC35060 chips are alloy-mounted and MC34060 chips are glass-mounted.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J (Alloy-Mounted Chip)	1000 mW	11.0 mW/°C	59°C
J (Glass-Mounted Chip)	1000 mW	8.2 mW/°C	28°C
N	1000 mW	9.2 mW	41°C

recommended operating conditions

	MC35060		MC34060		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	7	40	7	40	V
Amplifier input voltages, V_I	−0.3	$V_{CC}-2$	−0.3	$V_{CC}-2$	V
Collector output voltage, V_O		40		40	V
Collector output current (each transistor)		200		200	mA
Reference output current		10		10	mA
Current into feedback terminal		0.3		0.3	mA
Timing capacitor, C_T	0.47	10 000	0.47	10 000	nF
Timing resistor, R_T	1.8	500	1.8	500	kΩ
Oscillator frequency	1	200	1	200	kHz
Operating free-air temperature, T_A	−55	125	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†	MC35060			MC34060			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Output voltage (V_{ref})	I_O = 1 mA	4.75	5	5.25	4.75	5	5.25	V
Input regulation	V_{CC} = 7 V to 40 V, T_A = 25°C		2	25		2	25	mV
Output regulation	I_O = 1 to 10 mA, T_A = 25°C		1	15		1	15	mV
Output voltage change with temperature*	ΔT_A = MIN to MAX		0.2	2		0.2	2.6	%
Short-circuit output current§	V_{ref} = 0	10	35	50		35		mA

oscillator section

PARAMETER	TEST CONDITIONS†	MC35060			MC34060			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Frequency	C_T = 0.001 μF, R_T = 47 kΩ		25			25		kHz
Standard deviation of frequency¶	C_T = 0.001 μF, R_T = 47 kΩ		3			3		%
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		0.1			0.1		%
Frequency change with temperature*	C_T = 0.001 μF, R_T = 47 kΩ, ΔT_A = MIN to MAX			4			2	%

dead-time control-section (see figure 1)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Input bias current (pin 4)	V_I = 0 to 5.25 V			−2	−10	μA
Maximum duty cycle*	$V_{I\ (pin\ 4)}$ = 0	C_T = 0.1 μF, R_T = 12 kΩ	90	96	100	%
		C_T = 0.1 μF, R_T = 47 kΩ		92	100	
Input threshold voltage (pin 4)*	Zero duty cycle			3	3.3	V
	Maximum duty cycle		0			

error-amplifier sections

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input offset voltage	$V_{O\ (pin\ 3)}$ = 2.5 V		2	10	mV
Input offset current	$V_{O\ (pin\ 3)}$ = 2.5 V		25	250	nA
Input bias current	$V_{O\ (pin\ 3)}$ = 2.5 V		0.2	1	μA
Common-mode input voltage range	V_{CC} = 7 V to 40 V	−0.3 to V_{CC} − 2			V
Open-loop voltage amplification	ΔV_O = 3 V, R_L = 2 kΩ, V_O = 0.5 V to 3.5 V	70	95		dB
Unit-gain bandwidth			800		kHz
Common-mode rejection ratio	V_{CC} = 40 V	65	80		dB
Output sink current (pin 3)	V_{ID} = −15 mV to −5 V, $V_{(pin\ 3)}$ = 0.5 V	0.3	0.7		mA
Output source current (pin 3)	V_{ID} = 15 mV to 5 V, $V_{(pin\ 3)}$ = 3.5 V	−2			mA

output section

PARAMETER		TEST CONDITIONS		MC35060			MC34060			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Collector off-state current		V_{CE} = 40 V,	V_{CC} = 40 V		2	100		2	100	μA
Emitter off-state current		V_{CC} = V_C = 40 V,	V_E = 0			−150			−100	μA
Collector-emitter saturation voltage	Common-emitter	V_E = 0,	I_C = 200 mA		1.1	1.5		1.1	1.3	V
	Emitter follower	V_C = 15 V,	I_E = −200 mA		1.5	2.5		1.5	2.5	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions.

‡All typical values except for temperature coefficients are at T_A = 25°C.

§Duration of the short-circuit should not exceed one second.

¶Standard deviation is a measure of the statistical distribution about the mean as derived from the formula $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \bar{x})^2}{N-1}}$

*For MC35060 these parameters are guaranteed but not tested.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

pwm comparator section (see figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Input threshold voltage (pin 3)*	Zero duty cycle		4	4.5	V
Input sink current (pin 3)	$V_{(pin\ 3)}$ = 0.7 V	0.3	0.7		mA

total device

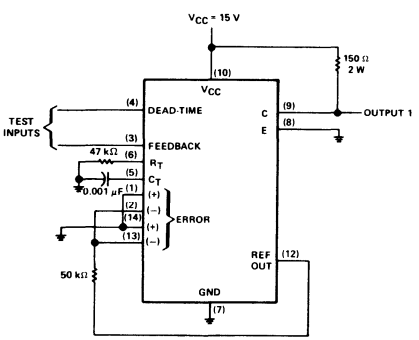
PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
Standby supply current	Pin 6 at V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		6	10	mA
		V_{CC} = 40 V		9	15	
Average supply current	$V_{(pin\ 4)}$ = 2 V,	See Figure 1		7.5		mA

switching characteristics, T_A = 25°C

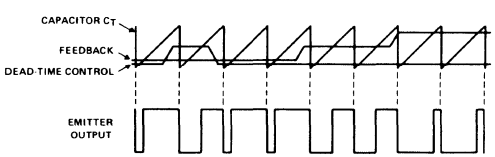
PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Output voltage rise time*	Common-emitter configuration,		100	200	ns
Output voltage fall time*	See Figure 3		25	100	ns
Output voltage rise time*	Emitter-follower configuration,		100	200	ns
Output voltage fall time*	See Figure 4		40	100	ns

‡All typical values except for temperature coefficients are at T_A = 25°C.
*For MC35060 these parameters are guaranteed but not tested.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



TIMING WAVEFORMS

FIGURE 1 — DEAD-TIME AND FEEDBACK CONTROL

PARAMETER MEASUREMENT INFORMATION

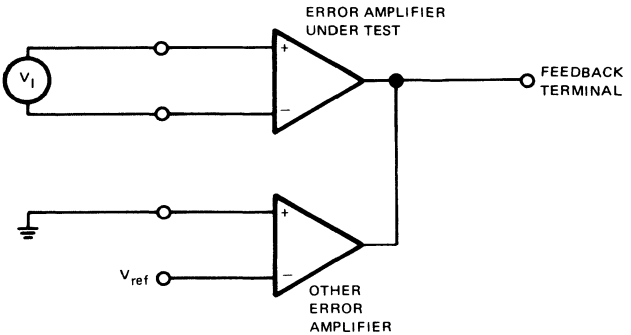
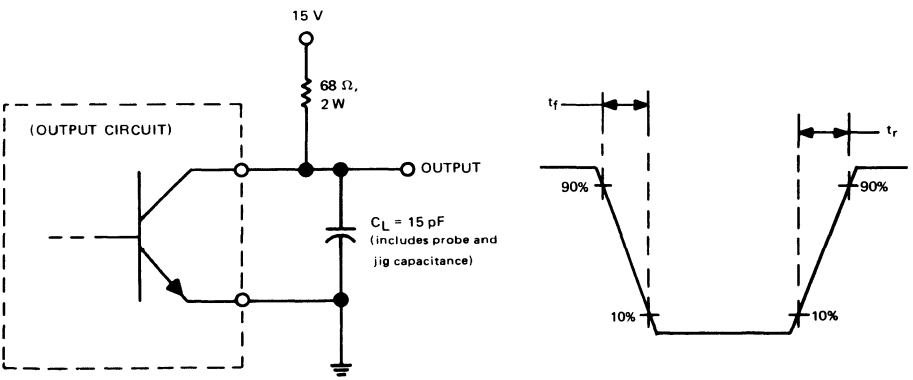


FIGURE 2 — ERROR-AMPLIFIER CHARACTERISTICS



TEST CIRCUIT

OUTPUT VOLTAGE WAVEFORM

FIGURE 3 — COMMON-EMITTER CONFIGURATION

PARAMETER MEASUREMENT INFORMATION

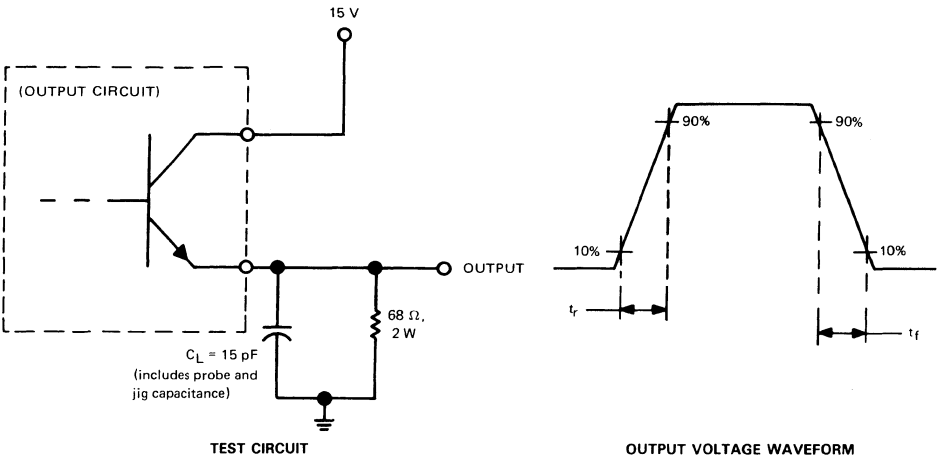


FIGURE 4 — EMITTER-FOLLOWER CONFIGURATION

TYPICAL CHARACTERISTICS

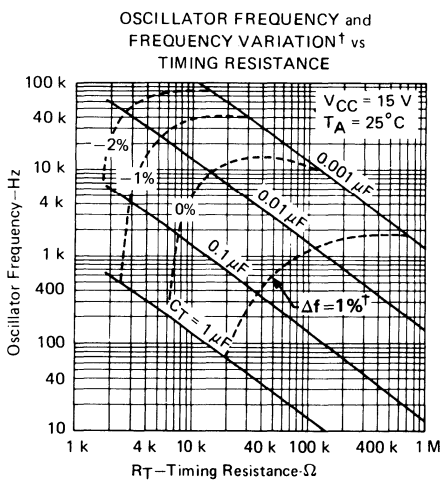


FIGURE 5

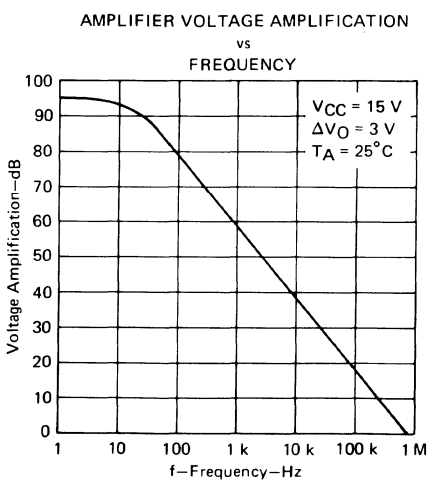


FIGURE 6

†Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

SERIES MC79L00
NEGATIVE-VOLTAGE REGULATORS

D2656, OCTOBER 1982

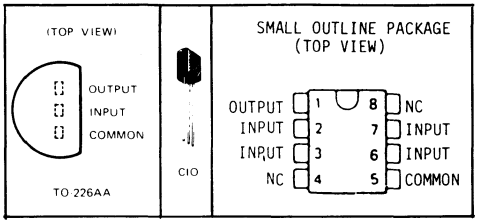
- 3-Terminal Regulators
- Output Current up to 100 mA
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Direct Replacement for Motorola MC79L00 Series
- Available in 5% or 10% Selections

NOMINAL OUTPUT VOLTAGE	5% OUTPUT VOLTAGE TOLERANCE	10% OUTPUT VOLTAGE TOLERANCE
−5 V	MC79L05AC	MC79L05C
−12 V	MC79L12AC	MC79L12C
−15 V	MC79L15AC	MC79L15C

description

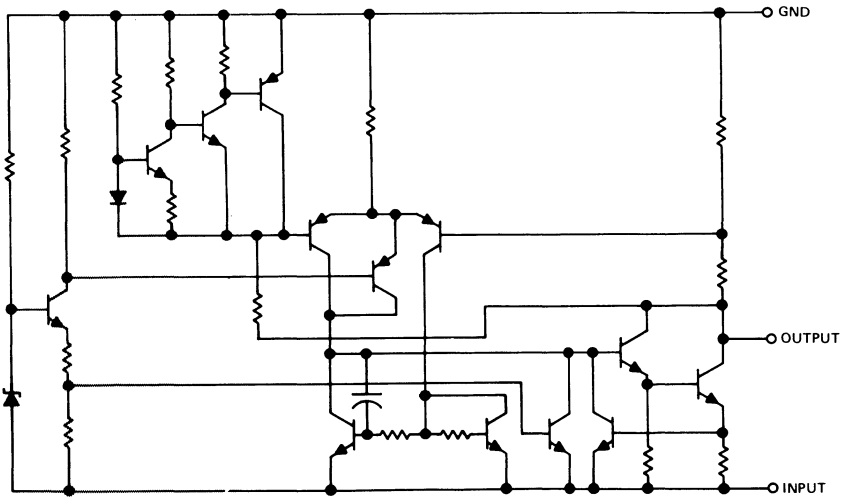
This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used to control series pass elements to make high-current voltage-regulator circuits. One of these regulators can deliver up to 100 mA of output current. The internal current-limiting and thermal-shutdown features make them essentially immune to overload. When used as a replacement for a Zener-diode and resistor combination, these devices can provide an effective improvement in output impedance of two orders of magnitude and lower bias current.

LP SILECT PACKAGE — MC79L00 ... D



NC - NO INTERNAL CONNECTION

schematic



absolute maximum ratings over operating temperature range (unless otherwise noted)

	MC79L05	MC79L12 MC79L15	UNIT
Input voltage	–30	–35	V
Continuous total dissipation at 25°C free-air temperature (see Note 1)	775	775	mW
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)	1600	1600	mW
Operating free-air, case, or virtual junction temperature range	0 to 150	0 to 150	°C
Storage temperature range	–65 to 150	–65 to 150	°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds	260	260	°C

NOTE 1: For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Figure 1 and Figure 2.

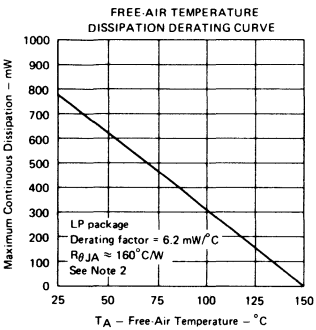


FIGURE 1

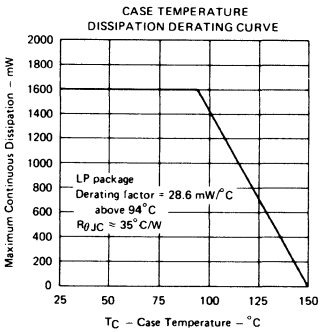


FIGURE 2

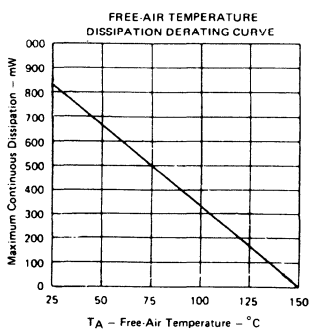


FIGURE 1

NOTE 2: This curve for the LP package is based on thermal resistance, $R_{\theta JA}$, measured in still air with the device mounted in an Augat socket. The bottom of the package was 3/8 inch above the socket.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	MC79L05	–7	–20	V
	MC79L12	–14.5	–27	
	MC79L15	–17.5	–30	
Output current, I_O			100	mA
Operating virtual junction temperature, T_J		0	125	°C

MC79L05 electrical characteristics at specified virtual junction temperature, V_I = –10 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MC79L05C			MC79L05AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage*		25°C	–4.6	–5	–5.4	–4.8	–5	–5.2	V
	V_I = –7 V to –20 V, I_O = 1 mA to 40 mA	0°C to 125°C	–4.5		–5.5	–4.75		–5.25	
	V_I = –10 V, I_O = 1 mA to 70 mA	0°C to 125°C	–4.5		–5.5	–4.75		–5.25	
Input regulation	V_I = –7 V to –20 V	25°C			200			150	mV
	V_I = –8 V to –20 V				150			100	
Ripple rejection	V_I = –8 V to –18 V, f = 120 Hz	25°C	40	49		41	49		dB
Output regulation	I_O = 1 mA to 100 mA	25°C			60			60	mV
	I_O = 1 mA to 40 mA				30			30	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		40			40		μV
Dropout voltage	I_O = 40 mA	25°C		1.7			1.7		V
Bias current		25°C			6			6	mA
		125°C			5.5			5.5	
Bias current change	V_I = –8 V to –20 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

MC79L12 electrical characteristics at specified virtual junction temperature, V_I = –19, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MC79L12C			MC79L12AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage*		25°C	–11.1	–12	–12.9	–11.5	–12	–12.5	V
	V_I = –14.5 to –27 V, I_O = 1 mA to 40 mA	0°C to 125°C	–10.8		–13.2	–11.4		–12.6	
	V_I = –19 V, I_O = 1 mA to 70 mA	0°C to 125°C	–10.8		–13.2	–11.4		–12.6	
Input regulation	V_I = –14.5 to –27 V	25°C			250			250	mV
	V_I = –16 V to –27 V				200			200	
Ripple rejection	V_I = –15 V to –25 V, f = 120 Hz	25°C	36	42		37	42		dB
Output regulation	I_O = 1 mA to 100 mA	25°C			100			100	mV
	I_O = 1 mA to 40 mA				50			50	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		80			80		μV
Dropout voltage	I_O = 40 mA	25°C		1.7			1.7		V
Bias current		25°C			6.5			6.5	mA
		125°C			6			6	
Bias current change	V_I = –16 V to –27 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

†All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for dc power dissipation permitted by absolute ratings.

MC79L15 electrical characteristics at specified virtual junction temperature, V_I = −23 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MC79L15C			MC79L15AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage *		25°C	−13.8	−15	−16.2	−14.4	−15	−15.6	V
	V_I = −17.5 V to −30 V, I_O = 1 mA to 40 mA	0°C to 125°C	−13.5		−16.5	−14.25		−15.75	
	V_I = −23 V, I_O = 1 mA to 70 mA	0°C to 125°C	−13.5		−16.5	−14.25		−15.75	
Input regulation	V_I = −17.5 V to −30 V	25°C			300			300	mV
	V_I = −20 V to −30 V				250			250	
Ripple rejection	V_I = −18.5 V to −28.5 V, f = 120 Hz	25°C	33	39		34	39		dB
Output regulation	I_O = 1 mA to 100 mA	25°C			150			150	mV
	I_O = 1 mA to 40 mA				75			75	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		90			90		μV
Dropout voltage	I_O = 40 mA	25°C		1.7			1.7		V
Bias current		25°C			6.5			6.5	mA
		125°C			6			6	
Bias current change	V_I = −20 V to −30 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

†All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

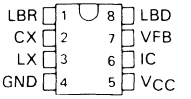
*This specification applies only for dc power dissipation permitted by absolute maximum ratings.

TYPES RM4193, RC4193
MICROPOWER SWITCHING REGULATOR

D2718, SEPTEMBER 1983

- High Efficiency . . . 80% Typ
- Low Bias Current . . . 135 μA
- Adjustable Output . . . 2.5 V to 24 V
- Output Current . . . 150 mA
- Internal Reference . . . 1.3 V ±5%
- Remote Shutdown Capabilities
- Interchangeable with Raytheon RM4193 and RC4193

RM4193 . . . JG
RC4193 . . . JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The RM4193 and RC4193 are monolithic micropower switching regulators designed to provide all the functions required to make a complete low-power switching regulator primarily for battery operated instruments. The RM4193 and RC4193 offer the system designer the flexibility of tailoring the circuit to the application. Typical applications include step-up switching regulation, step-down switching regulation, and inverting switch regulation. The devices each contain a 1.3-volt temperature-compensated band-gap reference, an adjustable free-running oscillator, voltage comparator, low battery detection circuitry, and a 150-milliampere output-switch transistor.

FUNCTION TABLE

PIN	FUNCTION	DESCRIPTION
1	LBR	Low battery resistor
2	CX	External capacitor
3	LX	External inductor
4	GND	Ground
5	V_{CC}	Supply voltage
6	IC	Reference set control
7	VFB	Feedback voltage
8	LBD	Low battery detector

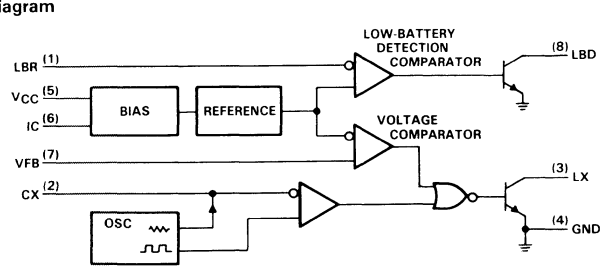
For most applications, these regulators can achieve up to 80% efficiency while operating over a wide supply voltage range from 2.4 volts to 24 volts at an ultra-low bias current drain of 135 microamperes. The RM4193 and RC4193 have an adjustable 100-hertz to 160-kilohertz free-running oscillator that provides the drive circuitry for the on-chip 150-milliampere output-switch transistor. An external capacitor on pin 2 determines the oscillator frequency.

The low-battery detection circuitry contains an open-collector output transistor that can be used to activate a liquid crystal display whenever the battery voltage drops below a programmed level. This programmed level is determined by the selection of external resistors connected to pin 1.

The regulator will shut off when pin 6 (IC) is below 0.5 volt. The shut-off feature is useful in battery-backup applications requiring operation only when the line power is removed. Another use of this feature is connecting a zener diode between pin 6 and the battery line to shut down the regulator whenever the battery voltage drops below a predetermined level.

The RM4193 will be characterized for operation over the full military temperature range of −55°C to 125°C. The RC4193 will be characterized for operation from 0°C to 70°C.

functional block diagram



PRODUCT PREVIEW

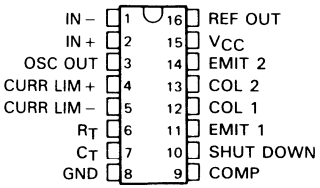
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TYPES SG1524, SG2524, SG3524
REGULATING PULSE WIDTH MODULATORS

D2294, APRIL 1977 – REVISED DECEMBER 1982

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for Single-Ended or Push-Pull Applications
- Low Standby Current . . . 8 mA Typ
- Interchangeable With Silicon General SG1524, SG2524, and SG3524

SG1524 . . . J
SG2524, SG3524 . . . J OR LN
DUAL-IN-LINE PACKAGE
(TOP VIEW)

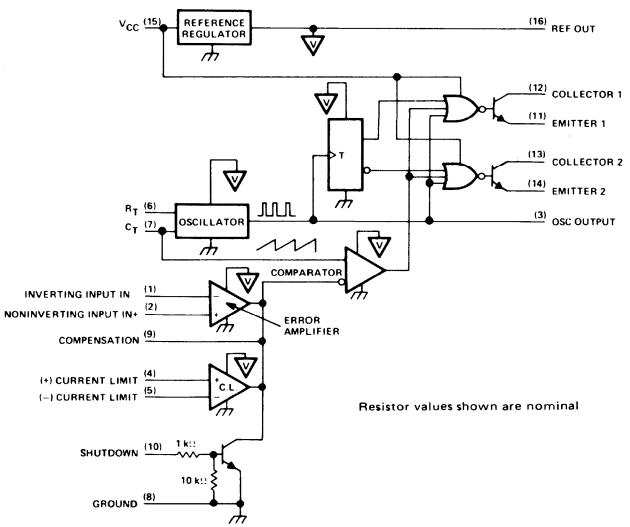


description

The SG1524, SG2524, and SG3524 incorporate on single monolithic chips all the functions required in the construction of a regulating power supply, inverter, or switching regulator. They can also be used as the control element for high-power-output applications. The SG1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers, and polarity converter applications employing fixed-frequency, pulse-width-modulation techniques. The complementary output allows either single-ended or push-pull application. Each device includes an on-chip regulator, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted pass transistors, a high-gain comparator, and current-limiting and shut-down circuitry.

The SG1524 is characterized for operation over the full military temperature range of −55°C to 125°C. The SG2524 is characterized for operation from −25°C to 85°C, and the SG3524 is characterized for operation from 0°C to 70°C.

functional block diagram



Resistor values shown are nominal

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (see Notes 1 and 2) . . . . . 40 V
Collector Output Current . . . . . 100 mA
Reference Output Current . . . . . 50 mA
Current Through C_T Terminal . . . . . −5 mA
Continuous Total Dissipation at (or below) 25°C Free-Air Temperature (See Note 3) . . . . . 1000 mW
Operating Free-Air Temperature Range: SG1524 . . . . . −55°C to 125°C
SG2524 . . . . . −25°C to 85°C
SG3524 . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. The reference regulator may be bypassed for operation from a fixed 5-volt supply by connecting the V_{CC} and reference output pins both to the supply voltage. In this configuration the maximum supply voltage is 6 volts.
3. For operation above 25°C free-air temperature refer to Figures 16 and 17. In the J package, SG1524 chips are alloy mounted; SG2524 and SG3524 chips are glass mounted.

recommended operating conditions

	SG1524		SG2524		SG3524		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	8	40	8	40	8	40	V
Reference output current	0	50	0	50	0	50	mA
Current thru C_T terminal	−0.03	−2	−0.03	−2	−0.03	−2	mA
Timing resistor, R_T	1.8	100	1.8	100	1.8	100	kΩ
Timing capacitor, C_T	0.001	0.1	0.001	0.1	0.001	0.1	μF
Operating free-air temperature	−55	125	−25	85	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 20 V, f = 20 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†	SG1524			SG2524			SG3524			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Output voltage		4.8	5	5.2	4.8	5	5.2	4.6	5	5.4	V
Input regulation	V_{CC} = 8 to 40 V		10	20		10	20		10	30	mV
Ripple rejection	f = 120 Hz		66			66			66		dB
Output regulation	I_O = 0 to 20 mA		20	50		20	50		20	50	mV
Output voltage change with temperature*	T_A = MIN to MAX		0.6	2		0.3	1		0.3	1	%
Short-circuit output current §	V_{ref} = 0		100			100			100		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except output voltage change with temperature are at T_A = 25°C.
§ Duration of the short-circuit should not exceed one second.
*For SG1524 this parameter is guaranteed but not tested.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 20 V, f = 20 kHz (unless otherwise noted)

oscillator section

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
Frequency	C_T = 0.001 μF, R_T = 2 kΩ		450		kHz
Standard deviation of frequency§	All values of voltage, temperature, resistance, and capacitance constant		5		%
Frequency change with voltage	V_{CC} = 8 to 40 V, T_A = 25°C			1	%
Frequency change with temperature	T_A = MIN to MAX			2	%
Output amplitude at pin 3			3.5		V
Output pulse width at pin 3	C_T = 0.01 μF		0.5		μs

error amplifier section

PARAMETER	TEST CONDITIONS	SG1524, SG2524			SG3524			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Input offset voltage	V_{IC} = 2.5 V		0.5	5		2	10	mV
Input bias current	V_{IC} = 2.5 V		2	10		2	10	μA
Open-loop voltage amplification		72	80		60	80		dB
Common-mode input voltage range	T_A = 25°C	1.8 to 3.4			1.8 to 3.4			V
Common-mode rejection ratio			70			70		dB
Unity-gain bandwidth			3			3		MHz
Output swing	T_A = 25°C	0.5		3.8	0.5		3.8	V

output section

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Collector-emitter breakdown voltage		40			V
Collector off-state current	V_{CE} = 40 V		0.01	50	μA
Collector-emitter saturation voltage	I_C = 50 mA		1	2	V
Emitter output voltage	V_C = 20 V, I_E = −250 μA	17	18		V
Turn-off voltage rise time	R_C = 2 kΩ		0.2		μs
Turn-on voltage fall time	R_C = 2 kΩ		0.1		μs

comparator section

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Maximum duty cycle, each output*		45			%
Input threshold voltage at pin 9	Zero duty cycle		1		V
	Maximum duty cycle		3.5		
Input bias current			−1		μA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values except for temperature coefficients are at T_A = 25°C.

§Standard deviation is a measure of the statistical distribution about the mean as derived from the formula $\sigma = \sqrt{\frac{\sum (X_n - \bar{X})^2}{N-1}}$

*For SG1524 this parameter is guaranteed but not tested.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 20 V, f = 20 kHz (unless otherwise noted)

current limiting section

PARAMETER	TEST CONDITIONS	SG1524, SG2524			SG3524			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Input voltage range (either input)		−1 to +1			−1 to +1			V
Sense voltage at T_A = 25°C	$V_{(pin\ 2)} - V_{(pin\ 1)}$ = 50 mV, $V_{(pin\ 9)}$ = 2 V	190	200	210	180	200	220	mV
Temperature coefficient of sense voltage			0.2			0.2		mV/°C

total device

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
Standby current	V_{CC} = 40 V, Pin 2 at 2 V,	Pins 1,4,7,8,9,11,14 grounded, All other inputs and outputs open		8	10	mA

‡All typical values except for temperature coefficients are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

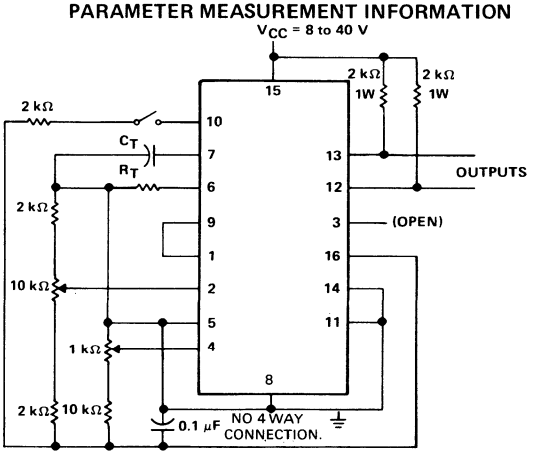


FIGURE 1–GENERAL TEST CIRCUIT

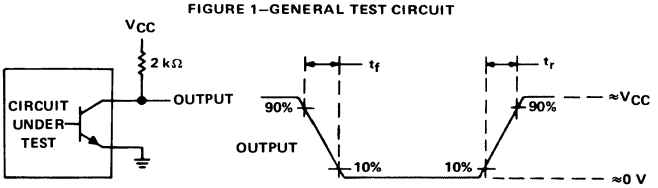


FIGURE 2–SWITCHING TIMES

TYPICAL CHARACTERISTICS

OPEN-LOOP VOLTAGE AMPLIFICATION
OF ERROR AMPLIFIER
vs
FREQUENCY

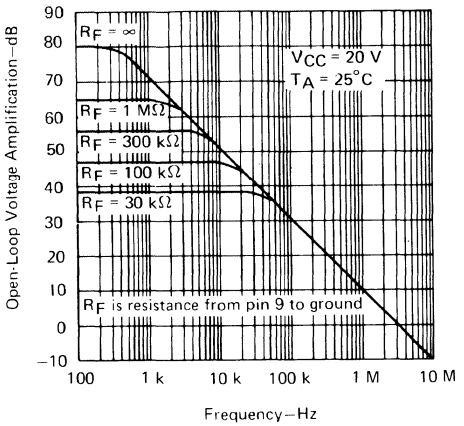


FIGURE 3

OSCILLATOR FREQUENCY
vs
TIMING RESISTANCE

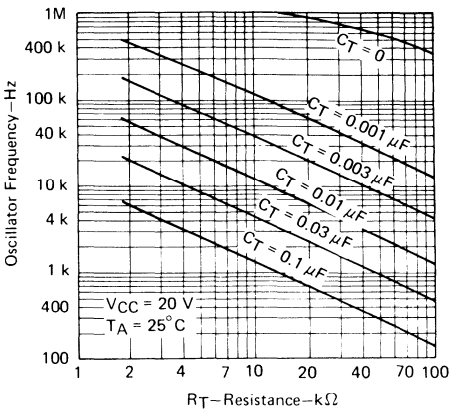


FIGURE 4

OUTPUT DEAD TIME
vs
TIMING CAPACITANCE VALUE

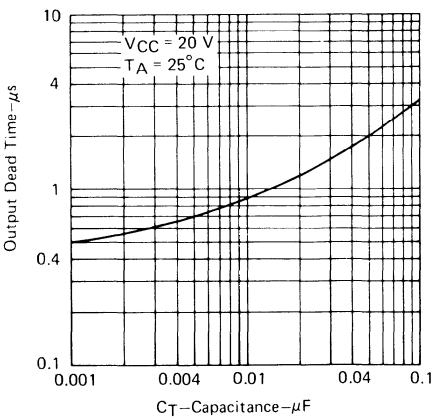


FIGURE 5

PRINCIPLES OF OPERATION

The SG1524† is a fixed-frequency pulse-width-modulation voltage-regulator control circuit. The regulator operates at a fixed frequency that is programmed by one timing resistor R_T and one timing capacitor C_T. R_T establishes a constant charging current for C_T. This results in a linear voltage ramp at C_T, which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The SG1524 contains an on-board 5-volt regulator that serves as a reference as well as supplying the SG1524's internal regulator control circuitry. The internal reference voltage is divided externally by a resistor ladder network to provide a reference within the common-mode range of the error amplifier as shown in Figure 6, or an external reference may be used. The output is sensed by a second resistor divider network and the error signal is amplified. This voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor (Q1 or Q2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of C_T. The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current-limiting and shut-down circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier, or to provide additional control to the regulator.

TYPICAL APPLICATION DATA

oscillator

The oscillator controls the frequency of the SG1524 and is programmed by R_T and C_T as shown in Figure 4.

$$f \approx \frac{1.15}{R_T C_T}$$

where R_T is in kilohms
C_T is in microfarads
f is in kilohertz

Practical values of C_T fall between 0.001 and 0.1 microfarad. Practical values of R_T fall between 1.8 and 100 kilohms. This results in a frequency range typically from 140 hertz to 500 kilohertz.

blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T as shown in Figure 5. If small values of C_T are required, the oscillator output pulse width may still be maintained by applying a shunt capacitance from pin 3 to ground.

synchronous operation

When an external clock is desired, a clock pulse of approximately 3 volts can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 kilohms. In this configuration R_T C_T must be selected for a clock period slightly greater than that of the external clock.

If two or more SG1524 regulators are to be operated synchronously, all oscillator output terminals should be tied together. The oscillator programmed for the minimum clock period will be the master from which all the other SG1524's operate. In this application, the C_T R_T values of the slaved regulators must be set for a period approximately 10% longer than that of the master regulator. In addition, C_T (master) = 2 C_T (slave) to ensure that the master output pulse, which occurs first, has a wider pulse width and will subsequently reset the slave regulators.

† Throughout these discussions, references to SG1524 apply also to SG2524 and SG3524.

TYPICAL APPLICATION DATA

voltage reference

The 5-volt internal reference may be employed by use of an external resistor divider network to establish a reference within the error amplifiers common-mode voltage range (1.8 to 3.4 volts) as shown in Figure 6, or an external reference may be applied directly to the error amplifier. For operation from a fixed 5-volt supply, the internal reference may be bypassed by applying the input voltage to both the V_{CC} and V_{REF} terminals. In this configuration, however, the input voltage is limited to a maximum of 6 volts.

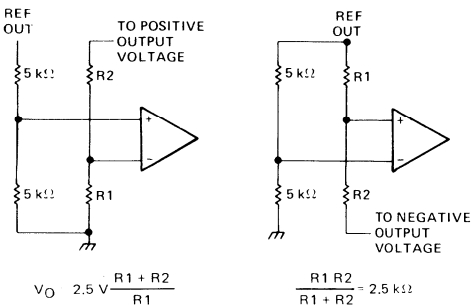


FIGURE 6–ERROR AMPLIFIER BIAS CIRCUITS

error amplifier

The error amplifier is a differential-input transconductance amplifier. The output is available for dc gain control or ac phase compensation. The compensation node (pin 9) is a high-impedance node (R_L = 5 megohms). The gain of the amplifier is $A_V = (0.002\ \Omega^{-1})\ R_L$ and can easily be reduced from a nominal 10,000 by an external shunt resistance from pin 9 to ground. Refer to Figure 3 for data.

compensation

Pin 9, as discussed above, is made available for compensation. Since most output filters will introduce one or more additional poles at frequencies below 200 hertz, which is the pole of the uncompensated amplifier, introduction of a zero to cancel one of the output filter poles is desirable. This can best be accomplished with a series RC circuit from pin 9 to ground in the range of 50 kilohms and 0.001 microfarads. Other frequencies can be canceled by use of the formula $f \approx 1/RC$.

shut down circuitry

Pin 9 can also be employed to introduce external control of the SG1524. Any circuit that can sink 200 microamperes can pull the compensation terminal to ground and thus disable the SG1524.

In addition to constant-current limiting, pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse should transformer saturation occur. Pin 5 may also be grounded to convert pin 4 into an additional shutdown terminal.

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TYPICAL APPLICATION DATA

current limiting

A current-limiting sense amplifier is provided in the SG1524. The current-limiting sense amplifier exhibits a threshold of 200 millivolts and must be applied in the ground line since the voltage range of the inputs is limited to +1 volt to −1 volt. Caution should be taken to ensure the −1-volt limit is not exceeded by either input, otherwise damage to the device may result.

Fold-back current limiting can be provided with the network shown in Figure 7. The current-limit schematic is shown in Figure 8.

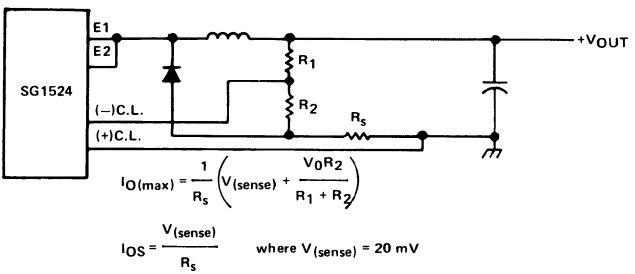


FIGURE 7–FOLDBACK CURRENT LIMITING FOR SHORTED OUTPUT CONDITIONS

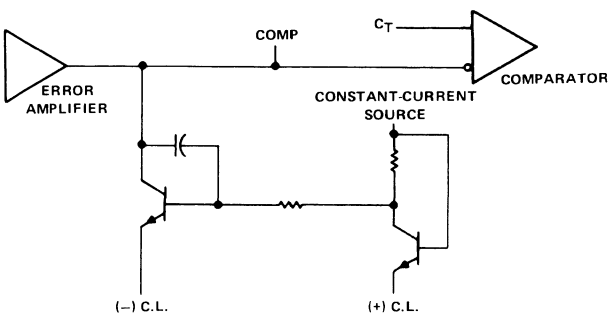


FIGURE 8–CURRENT-LIMIT SCHEMATIC

output circuitry

The SG1524 contains two identical n-p-n transistors the collectors and emitters of which are uncommitted. Each transistor has antisaturation circuitry that limits the current through that transistor to a maximum of 100 milliamperes for fast response.

TYPICAL APPLICATION DATA

general

There are a wide variety of output configurations possible when considering the application of the SG1524 as a voltage regulator control circuit. They can be segregated into three basic categories:

1. Capacitor-diode-coupled voltage multipliers
2. Inductor-capacitor-implemented single-ended circuits
3. Transformer-coupled circuits

Examples of these categories are shown in Figures 9, 10 and 11, respectively. Detailed diagrams of specific applications are shown in Figures 12 through 15.

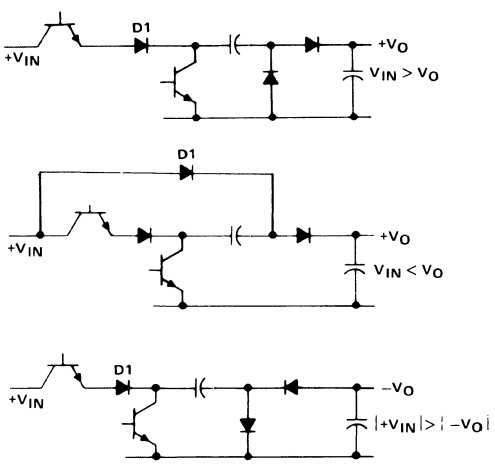


FIGURE 9–CAPACITOR-DIODE-COUPLED VOLTAGE-MULTIPLIER OUTPUT STAGES

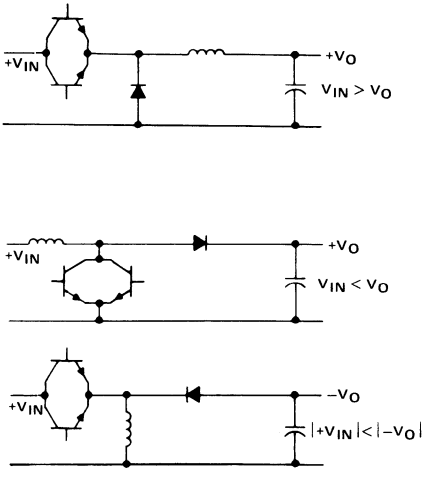
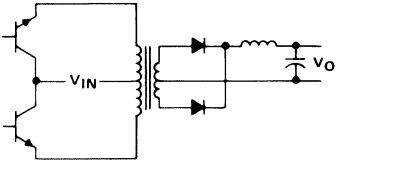
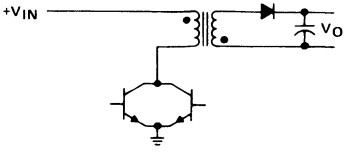


FIGURE 10–SINGLE-ENDED INDUCTOR CIRCUIT



PUSH PULL



FLYBACK

FIGURE 11–TRANSFORMER-COUPLED OUTPUTS

TYPICAL APPLICATION DATA

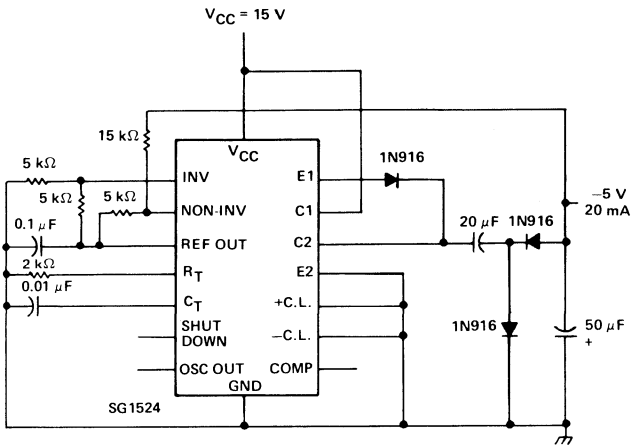


FIGURE 12–CAPACITOR-DIODE OUTPUT CIRCUIT

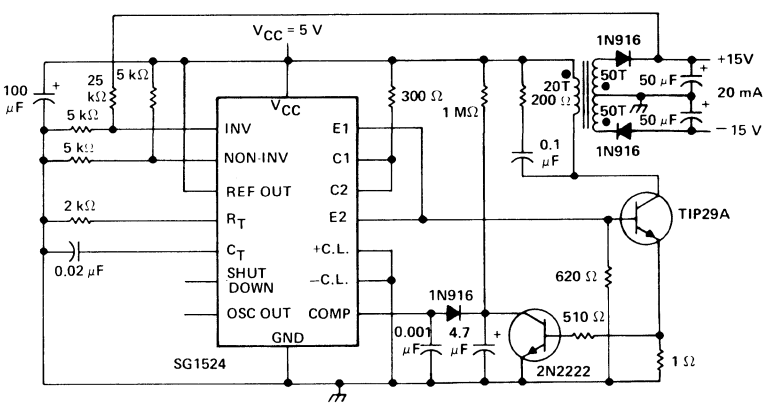


FIGURE 13 – FLYBACK CONVERTER CIRCUIT

TYPICAL APPLICATION DATA

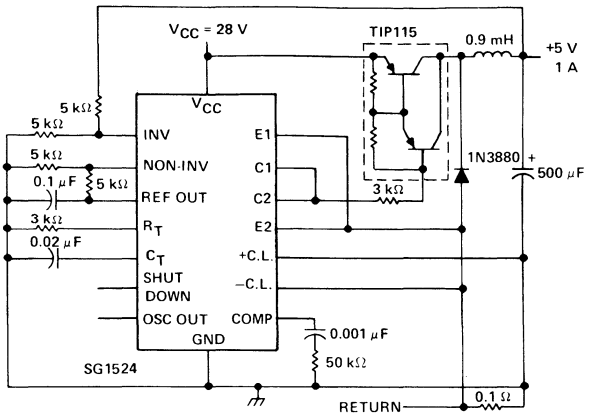


FIGURE 14–SINGLE-ENDED LC CIRCUIT

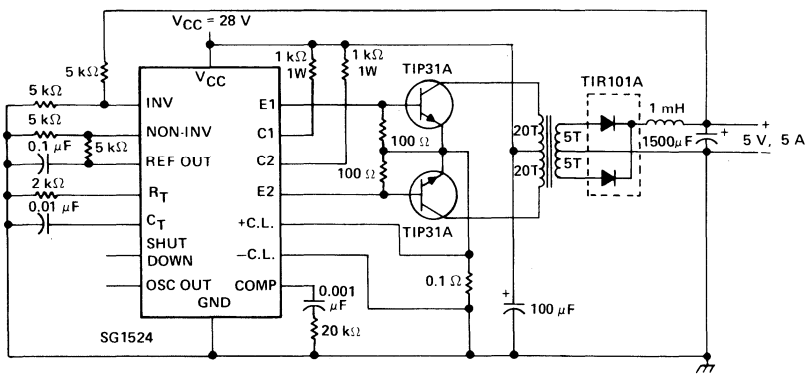


FIGURE 15–PUSH-PULL TRANSFORMER-COUPLED CIRCUIT

THERMAL INFORMATION

J PACKAGE FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

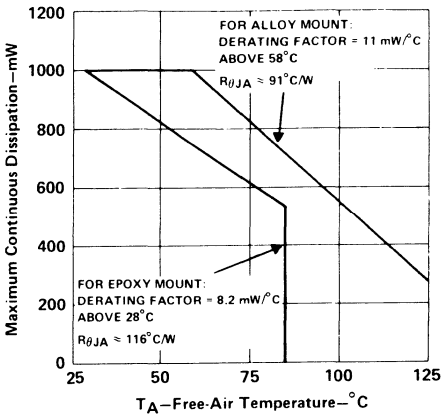


FIGURE 16

N PACKAGE FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

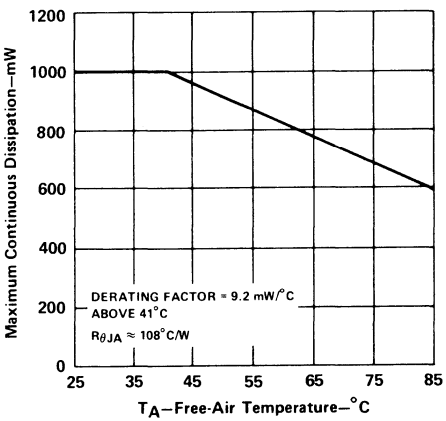
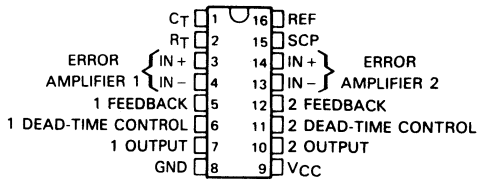


FIGURE 17

D2730, FEBRUARY 1983 – REVISED APRIL 1988

- Complete PWM Power Control Circuitry
- Completely Synchronized Operation
- Internal Undervoltage Lockout Protection
- Wide Supply Voltage Range
- Internal Short-Circuit Protection
- Oscillator Frequency . . . 500 kHz Max
- Variable Dead Time Provides Control Over Total Range
- Internal Regulator Provides a Stable 2.5-V Reference Supply

D OR N PACKAGE
(TOP VIEW)



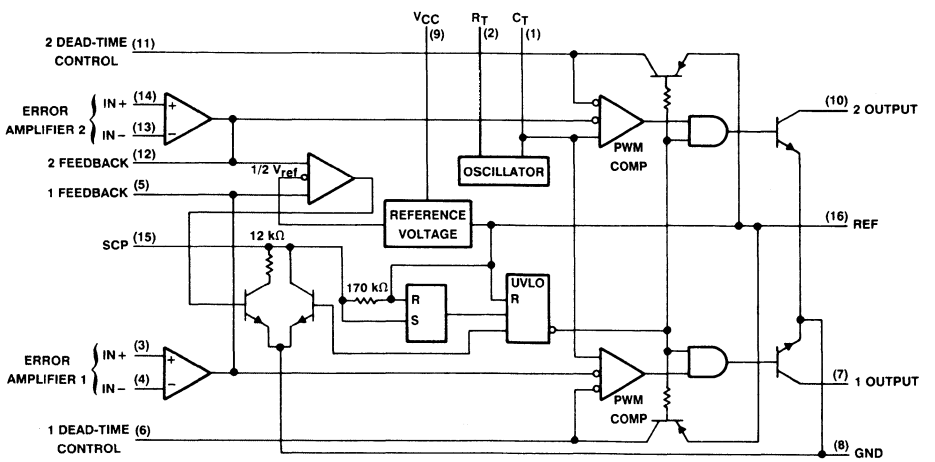
description

The TL1451AC incorporates on a single monolithic chip all the functions required in the construction of two pulse-width-modulation control circuits. Designed primarily for power supply control, the TL1451AC contains an on-chip 2.5-V regulator, two error amplifiers, an adjustable oscillator, two dead-time comparators, undervoltage lockout circuitry, and dual common-emitter output transistor circuits.

The uncommitted output transistors provide common-emitter output capability for each controller. The internal amplifiers exhibit a common-mode voltage range from 1.04 V to 1.45 V. The dead-time control comparator has no offset unless externally altered and may be used to provide 0% to 100% dead time. The on-chip oscillator may be operated by terminating R_T (pin 2) and C_T (pin 1). During low V_{CC} conditions, the undervoltage lockout control circuit feature locks the outputs off until the internal circuitry is operational.

The TL1451AC is characterized for operation from −20°C to 85°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 41 V
Amplifier input voltage . . . . . 20 V
Collector output voltage . . . . . 41 V
Collector output current . . . . . 21 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . −20°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	500 mW	4.0 mW/°C	320 mW	260 mW
N	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	3.6	40	V
Amplifier input voltage, V_I	1.05	1.45	V
Collector output voltage, V_O		40	V
Collector output current		20	mA
Current into feedback terminal		45	µA
Feedback resistor, R_F	100		kΩ
Timing capacitor, C_T	150	15000	pF
Timing resistor, R_T	5.1	100	kΩ
Oscillator frequency	1	500	kHz
Operating free-air temperature, T_A	−20	85	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 200 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output voltage (pin 16)	I_O = 1 mA	2.4	2.5	2.6	V
Output voltage change with temperature	T_A = −20°C to 25°C		−0.1%	±1%	
	T_A = 25°C to 85°C		−0.2%	±1%	
Input regulation	V_{CC} = 3.6 V to 40 V		2	12.5	mV
Output regulation	I_O = 0.1 mA to 1 mA		1	7.5	mV
Short-circuit output current	V_O = 0	3	10	30	mV

undervoltage lockout section

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Upper threshold voltage (pin 9)	I_{Oref} = 0.1 mA,	T_A = 25°C		2.72		V
Lower threshold voltage (pin 9)	I_{Oref} = 0.1 mA,	T_A = 25°C		2.6		V
Hysteresis (pin 9)	I_{Oref} = 0.1 mA,	T_A = 25°C	80	120		mV
Reset threshold voltage (pin 9)	I_{Oref} = 0.1 mA,	T_A = 25°C	1.5	1.8		V

† All typical values are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 200 kHz (unless otherwise noted) (continued)

protection control section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage (pin 15)	T_A = 25°C	0.65	0.7	0.75	V
Standby voltage (pin 15)	No pullup	140	185	230	mV
Latched input voltage (pin 15)	No pullup		60	120	mV
Input (source) current	V_I = 0.7 V, T_A = 25°C	−10	−15	−20	µA
Comparator threshold voltage (pins 5 and 12)			1.18		V

oscillator section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Frequency	C_T = 330 pF, R_T = 10 kΩ		200		kHz
Standard deviation of frequency	C_T = 330 pF, R_T = 10 kΩ		10%		
Frequency change with voltage	V_{CC} = 3.6 V to 40 V		1%		
Frequency change with temperature	T_A = −20°C to 25°C		−0.4%	±2%	
	T_A = 25°C to 85°C		−0.2%	±2%	

dead-time control section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input bias current (pins 6 and 11)				1	µA
Latch mode (source) current (pins 6 and 11)	T_A = 25°C	−80	−145		µA
Latched input voltage (pins 6 and 11)	I_O = 40 µA	2.3			V
Input threshold voltage at f = 10 kHz (pins 6 and 11)	Zero duty cycle		2.05	2.25	V
	Maximum duty cycle	1.2	1.45		

error-amplifier section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input offset voltage	V_O (pins 5 and 12) = 1.25 V			±6	mV
Input offset current	V_O (pins 5 and 12) = 1.25 V			±100	nA
Input bias current	V_O (pins 5 and 12) = 1.25 V		160	500	nA
Common-mode input voltage range	V_{CC} = 3.6 V to 40 V	1.05 to 1.45			V
Open-loop voltage amplification	R_F = 200 kΩ	70	80		dB
Unity-gain bandwidth			1.5		MHz
Common-mode rejection ratio		60	80		dB
Positive output voltage swing		V_{ref}−0.1			V
Negative output voltage swing				1	V
Output (sink) current (pins 5 and 12)	V_{ID} = −0.1 V, V_O = 1.25 V	0.5	1.6		mA
Output (source) current (pins 5 and 12)	V_{ID} = 0.1 V, V_O = 1.25 V	−45	−70		µA

† All typical values are at T_A = 25°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 200 kHz (unless otherwise noted) (continued)

output section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Collector off-state current	V_O = 40 V			10	μA
Output saturation voltage	I_O = 10 mA		1.2	2	V
Short-circuit output current	V_O = 6 V		90		mA

pwm comparator section

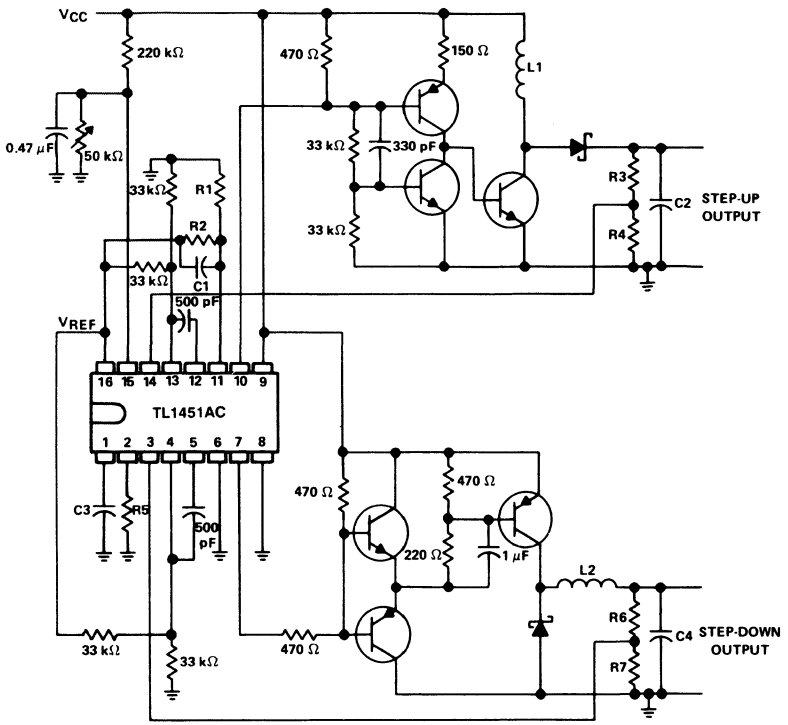
PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage	Zero duty cycle		2.05	2.25	V
at f = 10 kHz (pins 5 and 12)	Maximum duty cycle	1.2	1.45		
Input (sink) current (pins 5 and 12)	V_I = 1.25 V	0.5	1.6		mA
Input (source) current (pins 5 and 12)	V_I = 1.25 V	−45	−70		μA

total device

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Standby supply current	Off-state		1.3	1.8	mA
Average supply current	R_T = 10 kΩ		1.7	2.4	mA

† All typical values are at T_A = 25°C.

TYPICAL APPLICATION DATA



Values for R1 through R7, C1 through C4, and L1 and L2 depend upon inidividual application.

TYPE TL317M, TL317C
3-TERMINAL ADJUSTABLE REGULATOR

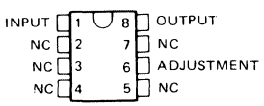
D2527, APRIL 1979 REVISED JANUARY 1983

- Output Voltage Range Adjustable from 1.2 V to 32 V
- Guaranteed Output Current Capability of 100 mA
- Input Regulation Typically 0.01% Per Input-Volt Change
- Output Regulation Typically 0.5%
- Ripple Rejection Typically 80 dB

terminal assignments

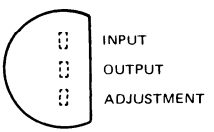
TL317M . . . JG PACKAGE

(TOP VIEW)



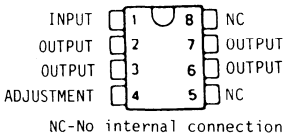
TL317C . . . LP SILECT PACKAGE

(TOP VIEW)



TL317C . . . D

SMALL OUTLINE PACKAGE
(TOP VIEW)



NC-No internal connection

NC – No internal connection

description

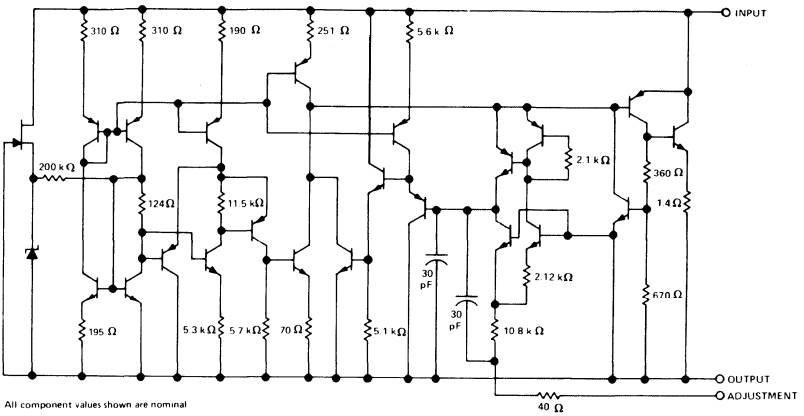
The TL317 is an adjustable 3-terminal positive-voltage regulator capable of supplying 100 milliamperes over an output-voltage range of 1.2 volts to 32 volts. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Both input and output regulation are better than standard fixed regulators. The device is packaged in standard packages that are easily mounted and handled.

In addition to higher performance than fixed regulators, this regulator offers full overload protection available only in integrated circuits. Included on the chip are current limit and thermal overload protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected. Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection, which is difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the regulator is useful in a wide variety of other applications. Since the regulator is floating and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded. Its primary application is that of a programmable output regulator, but by connecting a fixed resistor between the adjustment terminal and the output terminal, this device can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground, which programs the output to 1.2 volts where most loads draw little current.

The TL317M is characterized for operation over the full military temperature range from −55°C to 125°C. The TL317C is characterized for operation from 0°C to 125°C.

schematic



absolute maximum ratings over operation temperature range (unless otherwise noted)

Input-to-output differential voltage, $V_I - V_O$	35 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1): D package	833 mW
JG package	1050 mW
LP package	775 mW
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)	1600 mW
Operating free-air, case, or virtual junction temperature range: TL317M	−55°C to 150°C
TL317C	0°C to 150°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or LP package	260°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Dissipation Derating Table.

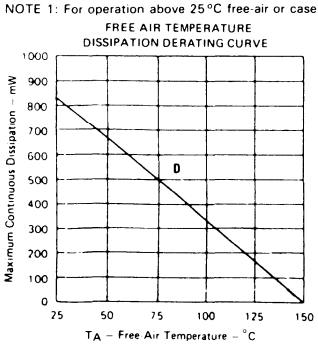


FIGURE 1

DISSIPATION DERATING TABLE

PACKAGE	REFERENCE POINT	POWER RATING	DERATING FACTOR	ABOVE (T_A OR T_C)
JG	Free-air	1050 mW	8.4 mW/°C	25°C
	Case	1600 mW	38.4 mW/°C	108°C
LP	Free-air	775 mW	6.2 mW/°C	25°C
	Case	1600 mW	28.6 mW/°C	94°C

recommended operating conditions

	TL317M		TL317C		UNIT
	MIN	MAX	MIN	MAX	
Output current, I_O	2.5	100	2.5	100	mA
Operating virtual junction temperature, T_J	−55	125	0	125	°C

electrical characteristics over recommended ranges of operating virtual junction temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Input regulation (see Note 2)	$V_I - V_O$ = 3 V to 35 V, See Note 3	T_J = 25°C		0.01	0.02	%/V
		I_O = 2.5 mA to 100 mA		0.02	0.05	
Ripple rejection	V_O = 10 V,	f = 120 Hz		65		dB
	V_O = 10 V, 10-μF capacitor between ADJ and ground	f = 120 Hz,	66	80		
Output regulation	I_O = 2.5 mA to 100 mA, T_J = 25°C, See Note 3	$V_O \leq$ 5 V		25		mV
		$V_O \geq$ 5 V		0.5		%
	I_O = 2.5 mA to 100 mA, See Note 3	$V_O \leq$ 5 V		50		mV
		$V_O \geq$ 5 V		1		%
Output voltage change with temperature	T_J = 0°C to 125°C			1		%
Output voltage long-term drift (see Note 4)	After 1000 h at T_J = 125°C and $V_I - V_O$ = 35 V			0.3	1	%
Output noise voltage	f = 10 Hz to 10 kHz,	T_J = 25°C		0.003		%
Minimum output current to maintain regulation	$V_I - V_O$ = 35 V			1.5	2.5	mA
Peak output current	$V_I - V_O \leq$ 35 V		100	200		mA
Adjustment-terminal current				50	100	μA
Change in adjustment-terminal current	$V_I - V_O$ = 2.5 V to 35 V,	I_O = 2.5 mA to 100 mA		0.2	5	μA
Reference voltage (output to ADJ)	$V_I - V_O$ = 3 V to 35 V, P ≤ rated dissipation	I_O = 2.5 mA to 100 mA,	1.2	1.25	1.3	V

†Unless otherwise noted, these specifications apply for the following test conditions: $V_I - V_O$ = 5 V and I_O = 2.5 mA.

NOTES: 2. Input regulation is expressed here as the percentage change in output voltage per 1-volt change at the input.

3. Input regulation and output regulation are measured using pulse techniques ($t_w \leq 10$ μs, duty cycle ≤ 5%) to limit changes in average internal dissipation. Output voltage changes due to large changes in internal dissipation must be taken into account separately.

4. Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

TYPICAL APPLICATION DATA

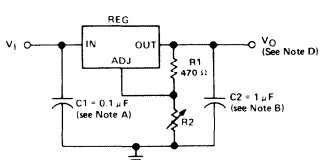


FIGURE 1–ADJUSTABLE VOLTAGE REGULATOR

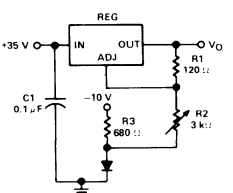
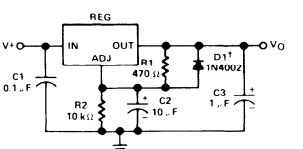


FIGURE 2–0-V to 30-V REGULATOR CIRCUIT



†D1 discharges C2 if output is shorted to ground.

FIGURE 3–ADJUSTABLE REGULATOR CIRCUIT WITH IMPROVED RIPPLE REJECTION

NOTES: A. Use of an input bypass capacitor is recommended if regulator is far from filter capacitors.

B. Use of an output capacitor improves transient response but is optional.

C. V_{ref} equals the difference between the output and adjustment terminal voltages.

D. Output voltage is calculated from the equation: $V_O = V_{ref}\left(1 + \frac{R2}{R1}\right)$

TYPICAL APPLICATION DATA

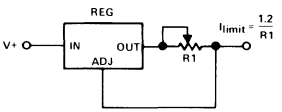


FIGURE 4–PRECISION CURRENT LIMITER CIRCUIT

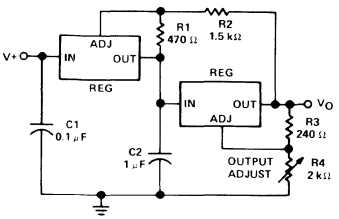


FIGURE 5–TRACKING PREREGULATOR CIRCUIT

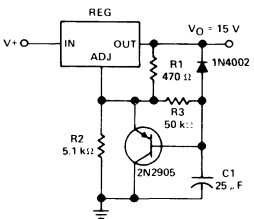


FIGURE 6–SLOW-TURN-ON 15-V REGULATOR CIRCUIT

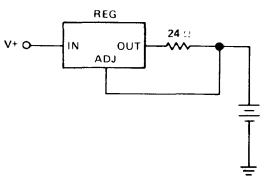
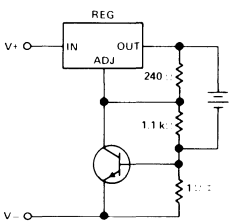
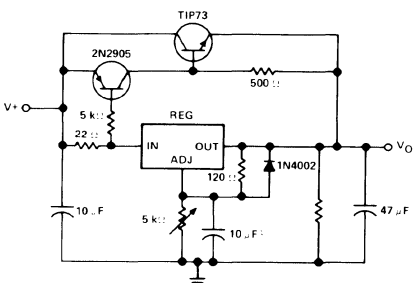


FIGURE 7–50-mA CONSTANT-CURRENT BATTERY CHARGER CIRCUIT



‡This resistor sets peak current (100 mA for 6 Ω).

FIGURE 8–CURRENT-LIMITED 6-V CHARGER



¶Minimum load current is 30 mA.
§Optional capacitor improves ripple rejection

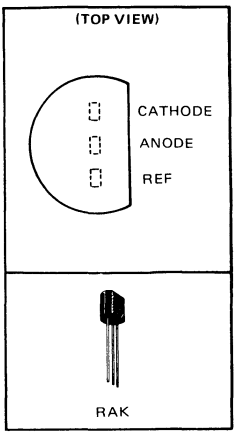
FIGURE 9–HIGH-CURRENT ADJUSTABLE REGULATOR

TYPES TL430I, TL430C
ADJUSTABLE SHUNT REGULATORS

D2165, JUNE 1976—REVISED DECEMBER 1982

- **Temperature Compensated**
- **Programmable Output Voltage**
- **Low Output Resistance**
- **Low Output Noise**
- **Sink Capability to 100 mA**

LP
SILECT PACKAGE
(TOP VIEW)

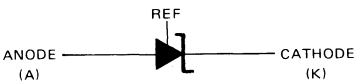


description

The TL430 is a three-terminal adjustable shunt regulator featuring excellent temperature stability, wide operating current range, and low output noise. The output voltage may be set by two external resistors to any desired value between 3 volts and 30 volts. The TL430 can replace zener diodes in many applications providing improved performance.

The TL430I is characterized for operation from −25 °C to 85 °C, and the TL430C is characterized for operating from 0 °C to 70 °C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Regulator voltage (see Note 1)	30 V
Continuous regulator current	150 mA
Continuous dissipation at (or below) 25 °C free-air temperature (see Note 2)	775 mW
Operating free-air temperature range: TL430I	−40 °C to 85 °C
TL430C	0 °C to 70 °C
Storage temperature range	−65 °C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260 °C

recommended operating conditions

	MIN	MAX	UNIT
Regulator Voltage, V_Z	V_{ref}	30	V
Regulator current, I_Z	2	100	mA

NOTES: 1. All voltage values are with respect to the anode terminal.
2. For operation above 25 °C free-air temperature, refer to Dissipation Derating Curves, Figure 5.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		TL430I			TL430C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{ref}	Reference input voltage	1	$V_Z = V_{ref}$,	I_Z = 10 mA	2.6	2.75	2.9	2.5	2.75	3	V
αV_{ref}	Temperature coefficient of reference input voltage	1	$V_Z = V_{ref}$, T_A = 0°C to 70°C	I_Z = 10 mA,		+120	+200		+120		ppm/°C
I_{ref}	Reference input current	2	I_Z = 10 mA, R2 = ∞	R1 = 10 kΩ,		3	10		3	10	μA
I_{ZK}	Regulator current near lower knee of regulation range	1	$V_Z = V_{ref}$			0.5	2		0.5	2	mA
I_{ZM}	Regulator current at maximum limit of regulation range	1	$V_Z = V_{ref}$		50			50			mA
		2	V_Z = 5 V to 30 V,	See Note 3	100			100			
r_z	Differential regulator resistance (see Note 4)	1	$V_Z = V_{ref}$, ΔI_Z = (52–2) mA			1.5	3		1.5	3	Ω
V_{nz}	Noise voltage	2	f = 0.1 Hz to 10 Hz	V_Z = 3 V		50			50		μV
				V_Z = 12 V		200			200		
				V_Z = 30 V		650			650		

NOTES: 3. The average power dissipation, $V_Z \cdot I_Z$ • duty cycle, must not exceed the maximum continuous rating in any 10-ms interval.

4. The regulator resistance for $V_Z > V_{ref}$, r_z', is given by:

$$r_z' = r_z\left(1 + \frac{R1}{R2}\right)$$

PARAMETER MEASUREMENT INFORMATION

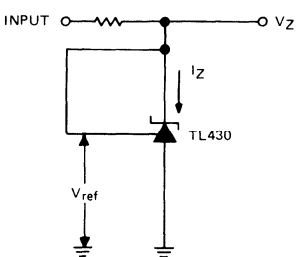
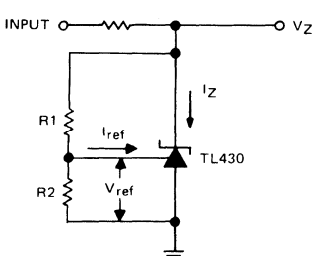


FIGURE 1–TEST CIRCUIT FOR $V_Z = V_{ref}$



$$V_Z = V_{ref}\left(1 + \frac{R1}{R2}\right) + I_{ref} \bullet R1$$

FIGURE 2–TEST CIRCUIT FOR $V_Z > V_{ref}$

TYPICAL CHARACTERISTICS

SMALL-SIGNAL REGULATOR IMPEDANCE
vs
FREQUENCY

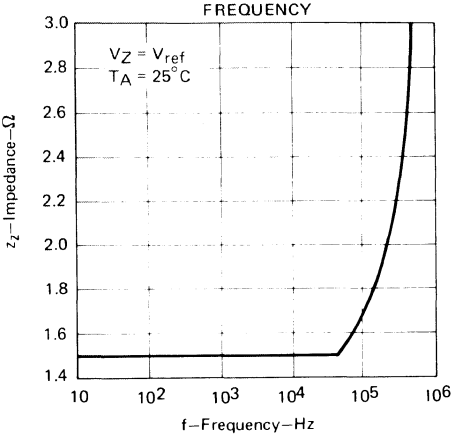


FIGURE 3

CURRENT
vs
VOLTAGE

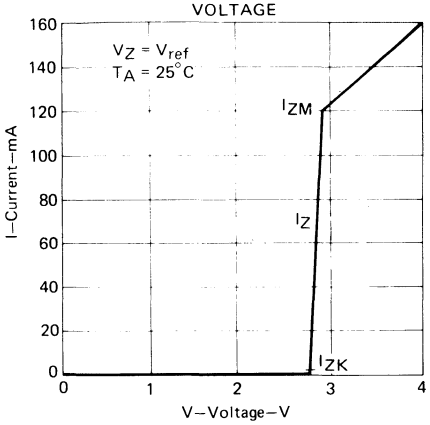


FIGURE 4

THERMAL INFORMATION

LP PACKAGE
DISSIPATION DERATING CURVE

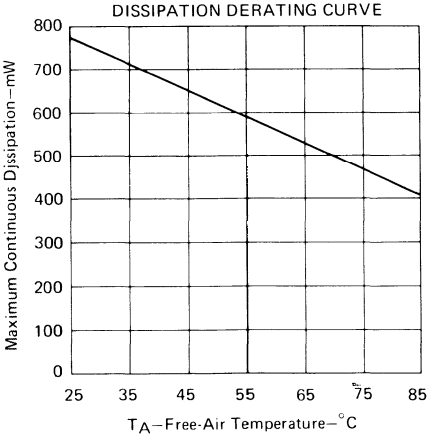


FIGURE 5

TYPICAL APPLICATION DATA

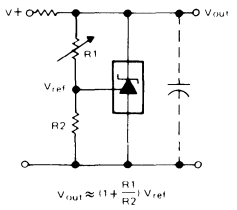


FIGURE 6—SHUNT REGULATOR

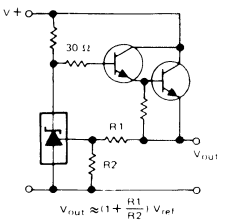


FIGURE 7—SERIES REGULATOR

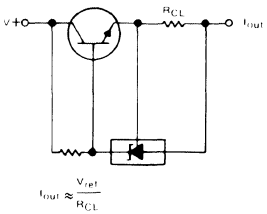


FIGURE 8—CURRENT LIMITER

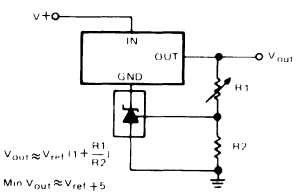


FIGURE 9—OUTPUT CONTROL OF A THREE-THERMAL FIXED REGULATOR

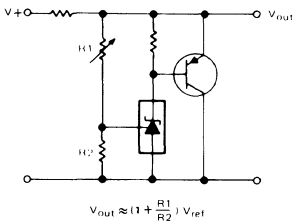


FIGURE 10—HIGHER-CURRENT APPLICATIONS

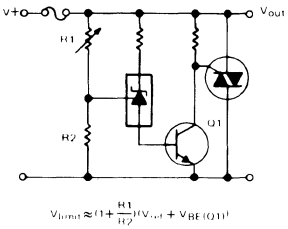


FIGURE 11—CROW BAR

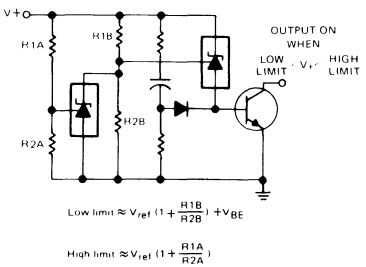


FIGURE 12—OVER-VOLTAGE/UNDER-VOLTAGE PROTECTION CIRCUIT

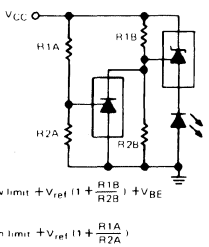


FIGURE 13—V_{CC} MONITOR

TYPES TL431M, TL431I, TL431C
ADJUSTABLE PRECISION SHUNT REGULATORS

D2410, JULY 1978–REVISED DECEMBER 1982

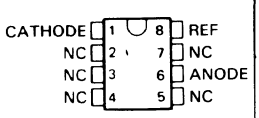
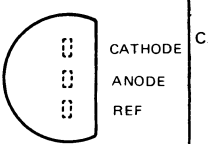
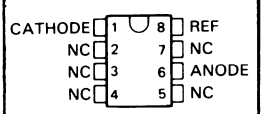
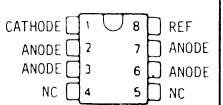
- Equivalent Full-Range Temperature Coefficient . . . 30 ppm/°C Typ
- Temperature Compensated for Operation Over Full Rated Operating Temperature Range
- Adjustable Output Voltage
- Fast Turn-On Response
- Sink Current Capability . . . 1 mA to 100 mA
- Low (0.2-Ω Typ) Dynamic Output Impedance
- Low Output Noise Voltage

description

The TL431 is a three-terminal adjustable regulator series with guaranteed thermal stability over applicable temperature ranges. The output voltage may be set to any value between V_{ref} (approximately 2.5 volts) and 36 volts with two external resistors (see Figure 16). These devices have a typical dynamic output impedance of 0.2 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for zener diodes in many applications.

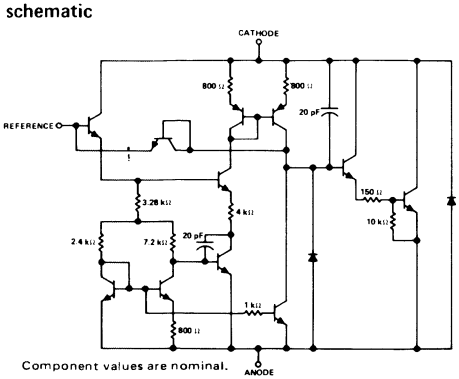
The TL431M is characterized for operation over the full military temperature range of −55°C to 125°C. The TL431I is characterized for operation from −40°C to 85°C, and the TL431C from 0°C to 70°C.

terminal assignments

TL431M . . . JG DUAL-IN-LINE PACKAGE	TL431I, TL431C . . . LP SILECT PACKAGE	TL431I, TL431C . . . P DUAL-IN-LINE PACKAGE	TL431I, TL431C . . . D
(TOP VIEW)	(TOP VIEW)	(TOP VIEW)	SMALL OUTLINE PACKAGE (TOP VIEW)
			
			

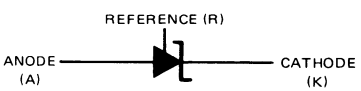
NC—No internal connection

schematic



Component values are nominal.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Cathode voltage (see Note 1) . . . . . 37 V
Continuous cathode current range . . . . . −100 mA to 150 mA
Reference input current range . . . . . −50 μA to 10 mA
Continuous power dissipation at (or below) 25°C free-air temperature (see Note 2): D package . . . . . 833 mW
JG package . . . . . 1050 mW
LP package . . . . . 775 mW
P package . . . . . 1000 mW
Operating free-air temperature range: TL431C . . . . . 0°C to 70°C
TL431I . . . . . −40°C to 85°C
TL431M . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: LP, P or D package . . . . . 260°C

NOTES: 1. Voltage values are with respect to the anode terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
JG	1050 mW	8.4 mW/°C	25°C
LP	775 mW	6.2 mW/°C	25°C
P	1000 mW	8.0 mW/°C	25°C

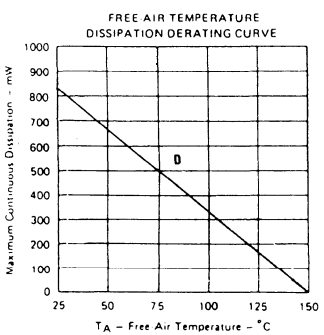


FIGURE 1

recommended operating conditions

	MIN	MAX	UNIT
Cathode voltage, V_{KA}	V_{ref}	36	V
Cathode current, I_K, (for regulation)	1	100	mA

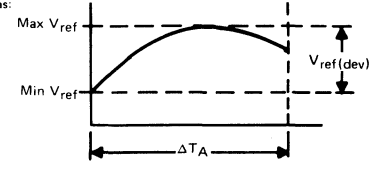
electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CIRCUIT	TEST CONDITIONS		TL431M			TL431I			TL431C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{ref}	Reference input voltage	1	$V_{KA} = V_{ref}$, I_K = 10 mA		2440	2495	2550	2440	2495	2550	2440	2495	2550	mV
$V_{ref(dev)}$	Deviation of reference input voltage over full temperature range‡	1	$V_{KA} = V_{ref}$, I_K = 10 mA, T_A = full range†		22	44		15	30		8	17		mV
$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage*	2	I_K = 10 mA	ΔV_{KA} = 10 V − V_{ref}		−1.4	−2.7		−1.4	−2.7		−1.4	−2.7	mV
				ΔV_{KA} = 36 V − 10 V		−1	−2		−1	−2		−1	−2	V
I_{ref}	Reference input current*	2	I_K = 10 mA, R1 = 10 kΩ, R2 = ∞			2	4		2	4		2	4	μA
$I_{ref(dev)}$	Deviation of reference input current over full temperature range‡*	2	I_K = 10 mA, R1 = 10 kΩ, R2 = ∞, T_A = full range†			1	3		0.8	2.5		0.4	1.2	μA
I_{min}	Minimum cathode current for regulation	1	$V_{KA} = V_{ref}$			0.4	1		0.4	1		0.4	1	mA
I_{off}	Off-state cathode current	3	V_{KA} = 36 V, V_{ref} = 0			0.1	1		0.1	1		0.1	1	μA
$\lvert z_{ka} \rvert$	Dynamic impedance§	1	$V_{KA} = V_{ref}$, I_K = 1 mA to 100 mA, f ≤ 1 kHz			0.2	0.5		0.2	0.5		0.2	0.5	Ω

†Full temperature range is −55°C to 125°C for the TL431M, −40°C to 85°C for the TL431I, and 0°C to 70°C for the TL431C.

‡The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The equivalent full-range temperature coefficient of the reference input voltage, αV_{ref}, is defined as:

$$\left|\alpha V_{ref}\right| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{ref(dev)}}{V_{ref\ @\ 25°C}}\right) \times 10^6}{\Delta T_A}$$



where ΔT_A is the rated operating free-air temperature range of the device.

αV_{ref} can be positive or negative depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature (see Figure 8).

Example: Max V_{ref} = 2500 mV @ 30°C, Min V_{ref} = 2492 mV @ 0°C, V_{ref} = 2495 mV @ 25°C, ΔT_A = 70°C for TL431C

$$\left|\alpha_{Vref}\right| = \frac{\left(\frac{8\ mV}{2495\ mV}\right) \times 10^6}{70°C} = 46\ ppm/°C$$

Because minimum V_{ref} occurs at the lower temperature, the coefficient is positive.

§The dynamic impedance is defined as:

$$\left|z_{ka}\right| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is operated with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:

$$\left|z'\right| = \frac{\Delta V}{\Delta I} \approx \left|z_{ka}\right| \left(1 + \frac{R1}{R2}\right)$$

*For M-suffix devices these parameters are guaranteed but not tested.

PARAMETER MEASUREMENT INFORMATION

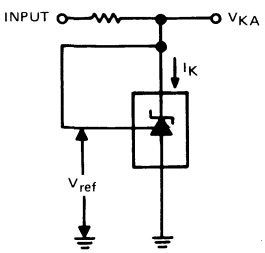


FIGURE 1–TEST CIRCUIT FOR $V_{KA} = V_{ref}$

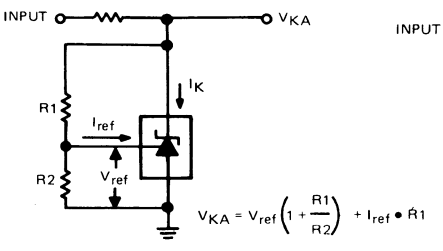


FIGURE 2–TEST CIRCUIT FOR $V_{KA} > V_{ref}$

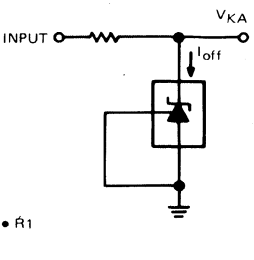


FIGURE 3–TEST CIRCUIT FOR I_{off}

TYPICAL CHARACTERISTICS

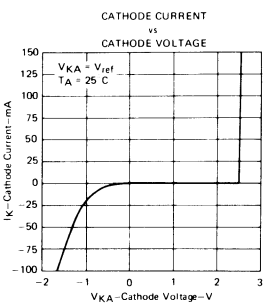


FIGURE 4

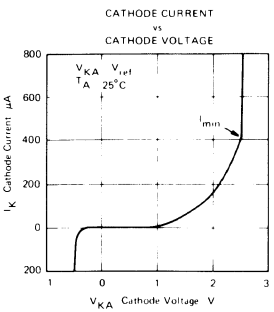


FIGURE 5

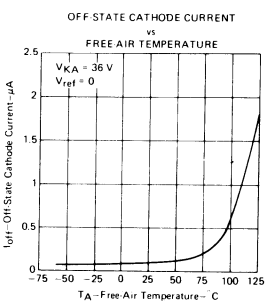


FIGURE 6

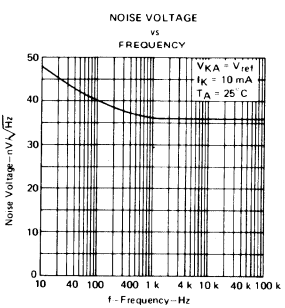


FIGURE 7

TYPICAL CHARACTERISTICS

REFERENCE INPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

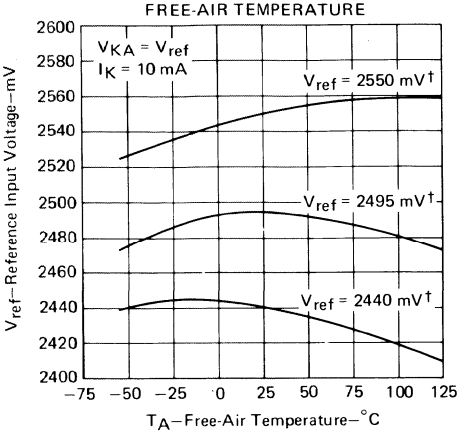


FIGURE 8

REFERENCE INPUT CURRENT
vs
FREE-AIR TEMPERATURE

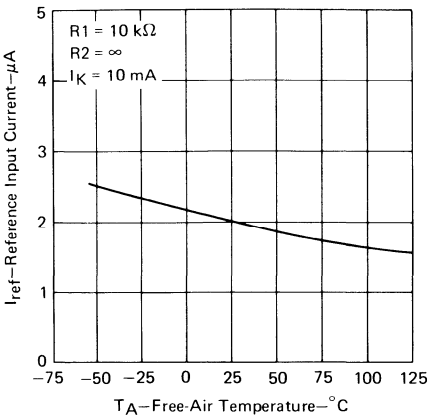


FIGURE 9

CHANGE IN REFERENCE INPUT VOLTAGE
vs
CATHODE VOLTAGE

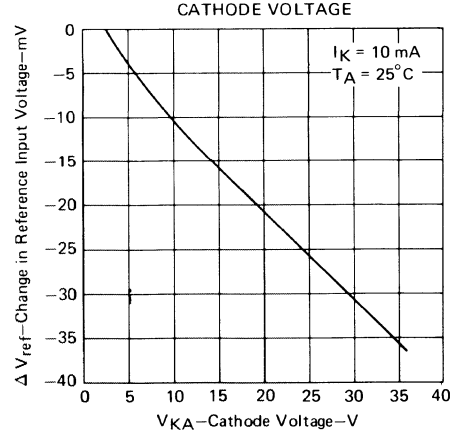


FIGURE 10

DYNAMIC IMPEDANCE
vs
FREE-AIR TEMPERATURE

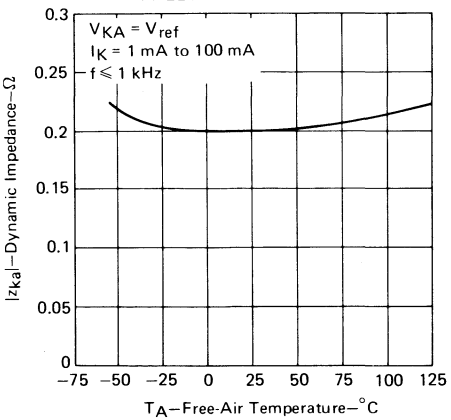


FIGURE 11

†Data is for devices having the indicated value of V_{ref} at I_K = 10 mA, T_A = 25°C.

TYPICAL CHARACTERISTICS

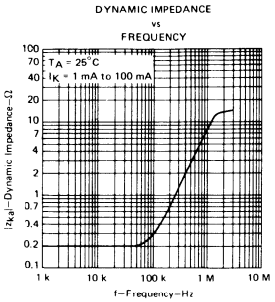
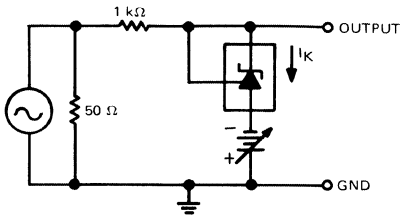


FIGURE 12



TEST CIRCUIT FOR DYNAMIC IMPEDANCE

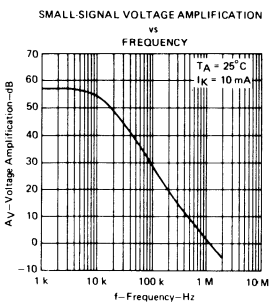
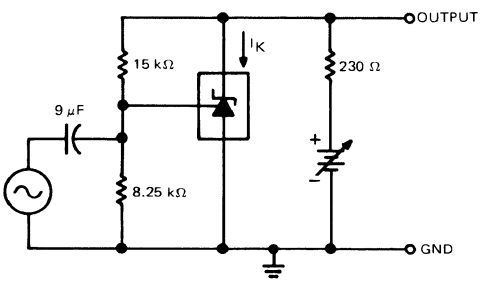


FIGURE 13



TEST CIRCUIT FOR VOLTAGE AMPLIFICATION

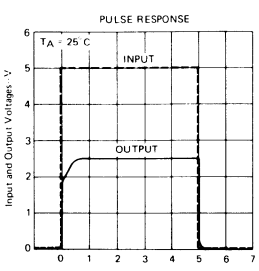
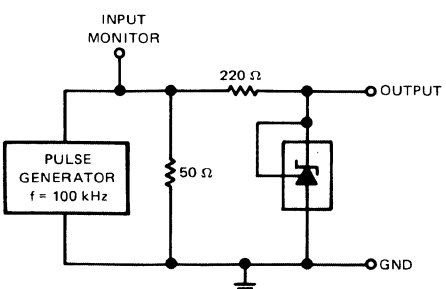
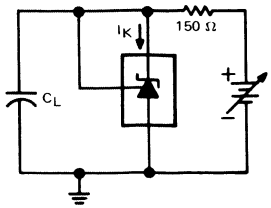


FIGURE 14

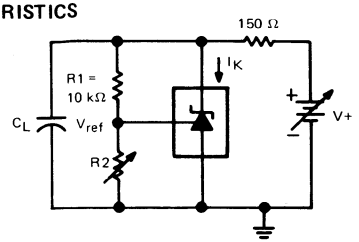


TEST CIRCUIT FOR PULSE RESPONSE

TYPICAL CHARACTERISTICS



TEST CIRCUIT FOR CURVE A BELOW



TEST CIRCUIT FOR CURVES B, C, AND D BELOW

STABILITY BOUNDARY CONDITIONS

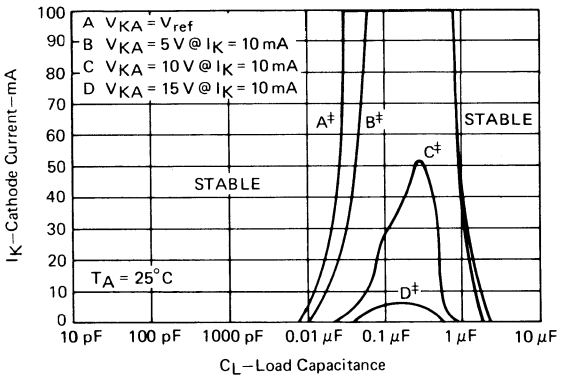


FIGURE 15

‡The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V+ were adjusted to establish the initial V_{KA} and I_K conditions with C_L = 0. V+ and C_L were then adjusted to determine the ranges of stability.

TYPICAL APPLICATIONS

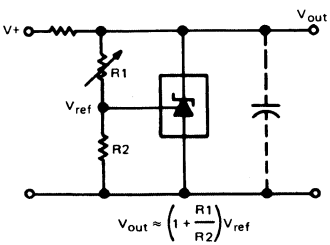


FIGURE 16—SHUNT REGULATOR

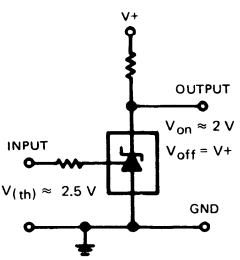


FIGURE 17—SINGLE-SUPPLY COMPARATOR WITH TEMPERATURE-COMPENSATED THRESHOLD

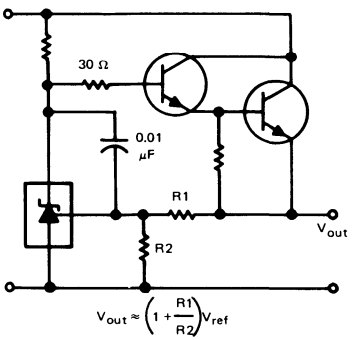


FIGURE 18—SERIES REGULATOR

TYPICAL APPLICATIONS

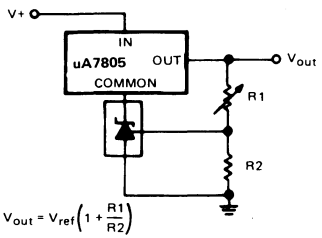


FIGURE 19– OUTPUT CONTROL OF A THREE-TERMINAL FIXED REGULATOR

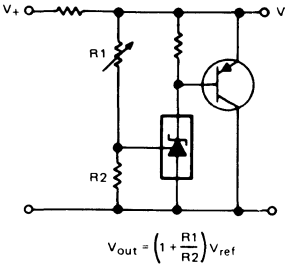


FIGURE 20–HIGHER-CURRENT SHUNT REGULATOR

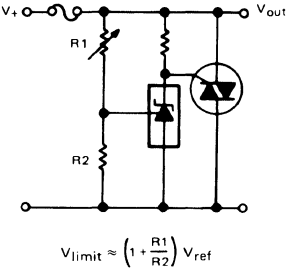


FIGURE 21–CROW BAR

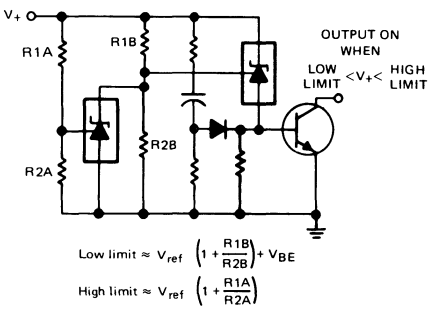


FIGURE 22–OVER-VOLTAGE/UNDER-VOLTAGE PROTECTION CIRCUIT

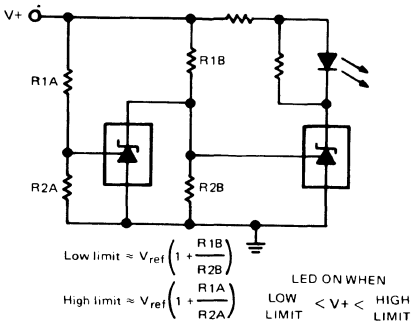


FIGURE 23–VOLTAGE MONITOR

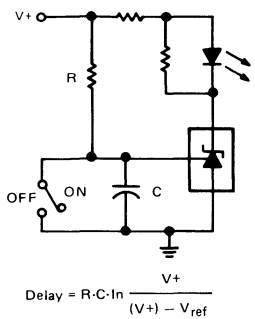


FIGURE 24–DELAY TIMER

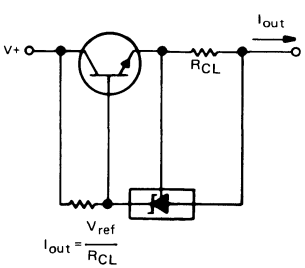


FIGURE 25–CURRENT LIMITER OR CURRENT SOURCE

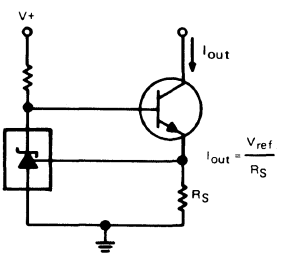


FIGURE 26–CONSTANT-CURRENT SINK

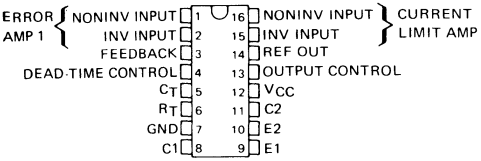
TYPES TL493, TL494, TL495
PULSE-WIDTH-MODULATION CONTROL CIRCUITS

D2535, JANUARY 1983 – REVISED SEPTEMBER 1983

- **Complete PWM Power Control Circuitry**
- **Uncommitted Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Single-Ended or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead-Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply Trimmed to 1%**
- **Circuit Architecture Allows Easy Synchronization**
- **TL493 Has Output Current-Limit Sensing**
- **TL495 Has On-Chip 39-V Zener and External Control of Output Steering**

TL493C . . . N

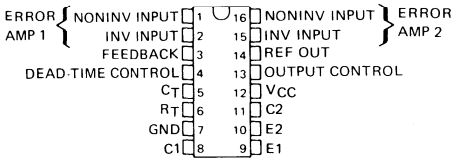
DUAL-IN-LINE PACKAGE (TOP VIEW)



TL494M . . . J

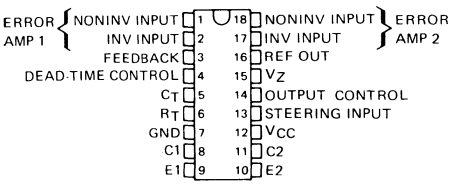
TL494I, TL494C . . . J OR N

DUAL-IN-LINE PACKAGE (TOP VIEW)



TL495C . . . N

DUAL-IN-LINE PACKAGE (TOP VIEW)



DEVICE TYPES, SUFFIX VERSIONS, AND PACKAGES

	TL493	TL494	TL495
TL49–M	*	J	*
TL49–I	*	J,N	*
TL49–C	N	J,N	N

*These combinations are not defined by this data sheet.

description

The TL493, TL494, and TL495 each incorporate on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, these devices offer the systems engineer the flexibility to tailor the power supply control circuitry to his application.

The TL493 contains an error amplifier, current-limiting amplifier, an on-chip adjustable oscillator, a dead-time control comparator, pulse-steering control flip-flop, a 5-volt, 1%-precision regulator, and output-control circuits.

The error amplifier exhibits a common-mode voltage range from −0.3 volts to V_{CC} − 2 volts. The current-limit amplifier exhibits a common-mode voltage range from −0.3 volts to 3 volts with an offset voltage of approximately 80 millivolts in series with the inverting input to ease circuit design requirements. The dead-time control comparator has a fixed offset that provides approximately 5% dead time when externally altered. The on-chip oscillator may be bypassed by terminating R_T (pin 6) to the reference output and providing a sawtooth input to C_T (pin 5), or it may be used to drive the common circuits in synchronous multiple-rail power supplies.

FUNCTION TABLE

INPUTS		OUTPUT FUNCTION
OUTPUT CONTROL	STEERING INPUT (TL495 only)	
$V_I \leq 0.4$ V	Open	Single-ended or parallel output
$V_I \geq 2.4$ V	Open	Normal push-pull operation
$V_I \geq 2.4$ V	$V_I \leq 0.4$ V	PWM Output at Q1
$V_I \geq 2.4$ V	$V_I \geq 2.4$ V	PWM Output at Q2

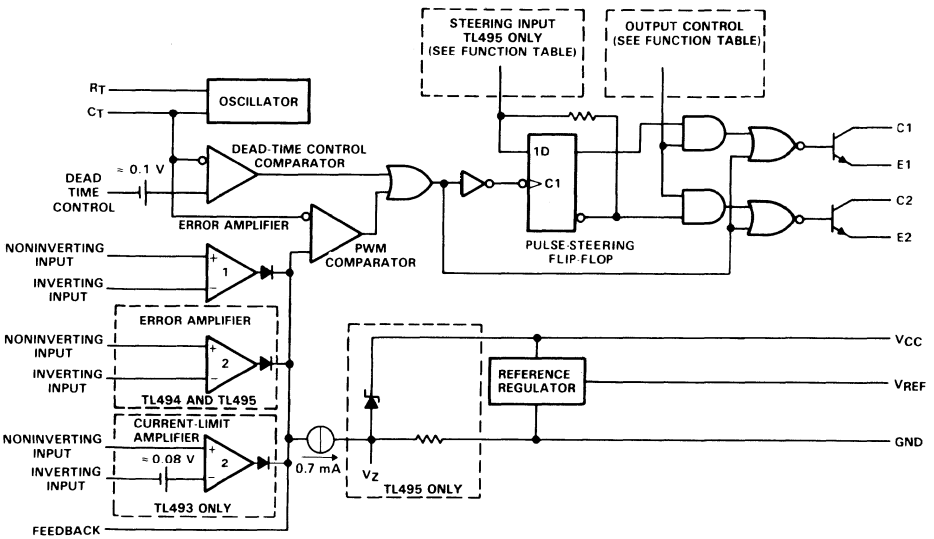
description (continued)

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. Each device provides for push-pull or single-ended output operation, which may be selected through the output-control function. The architecture of these devices prohibits the possibility of either output being pulsed twice during push-pull operation.

The TL493 and TL494 are similar except that an additional error amplifier is included in the TL494 instead of a current-limiting amplifier. The TL495 provides the identical functions found in the TL494. In addition, it contains an on-chip 39-volt zener diode for high-voltage applications where V_{CC} is greater than 40 volts, and an output-steering control that overrides the internal control of the pulse-steering flip-flop.

The TL494M is characterized for operation over the full military temperature range from −55°C to 125°C. The TL494I is characterized for operation from −25°C to 85°C. The TL493C, TL494C, and TL495C are characterized for operation from 0°C to 70°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TL494M	TL494I	TL493C TL494C TL495C	UNIT
Supply voltage, V_{CC} (see Note 1)	41	41	41	V
Amplifier input voltages	$V_{CC}+0.3$	$V_{CC}+0.3$	$V_{CC}+0.3$	V
Collector output voltage	41	41	41	V
Collector output current	250	250	250	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1000	1000	1000	mW
Operating free-air temperature range	−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Table. In the J package, TL494M chips are alloy-mounted; TL494I and TL494C chips are glass mounted.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J (Alloy-Mounted Chip)	1000 mW	11.0 mW/°C	59°C
J (Glass-Mounted Chip)	1000 mW	8.2 mW/°C	28°C
N	1000 mW	9.2 mW/°C	41°C

recommended operating conditions

	TL494M		TL494I		TL493C TL494C TL495C		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	7	40	7	40	7	40	V
Amplifier input voltages, V_I	−0.3	$V_{CC}-2$	−0.3	$V_{CC}-2$	−0.3	$V_{CC}-2$	V
Collector output voltage, V_O		40		40		40	V
Collector output current (each transistor)		200		200		200	mA
Current into feedback terminal		0.3		0.3		0.3	mA
Timing capacitor, C_T	0.47	10 000	0.47	10 000	0.47	10 000	nF
Timing resistor, R_T	1.8	500	1.8	500	1.8	500	kΩ
Oscillator frequency	1	300	1	300	1	300	kHz
Operating free-air temperature, T_A	−55	125	−25	85	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†	TL494M			TL493C, TL494I, TL494C, TL495C			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Output voltage (V_{ref})	I_O = 1 mA	4.75	5	5.25	4.75	5	5.25	V
Input regulation	V_{CC} = 7 V to 40 V		2	25		2	25	mV
Output regulation	I_O = 1 to 10 mA		1	15		1	15	mV
Output voltage change with temperature*	ΔT_A = MIN to MAX		0.2	1		0.2	1	%
Short-circuit output current§	V_{ref} = 0	10	35	50		35		mA

oscillator section (see Figure 1)

PARAMETER	TEST CONDITIONS†	TL494M			TL493C, TL494I, TL494C, TL495C			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Frequency	C_T = 0.01 μF, R_T = 12 kΩ		10			10		kHz
Standard deviation of frequency¶	All values of V_{CC}, C_T, R_T, T_A constant		10			10		%
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		0.1			0.1		%
Frequency change with temperature*	C_T = 0.01 μF, R_T = 12 kΩ, ΔT_A = MIN to MAX			12			12	%

amplifier sections (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Input offset voltage	Error	V_O (pin 3) = 2.5 V		2	10	mV
	current-limit (TL493 only)			80		
Input offset current		V_O (pin 3) = 2.5 V		25	250	nA
Input bias current		V_O (pin 3) = 2.5 V		0.2	1	μA
Common-mode input voltage range	Error	V_{CC} = 7 V to 40 V	−0.3 to V_{CC} − 2			V
	Current-limit (TL493 only)		−0.3 to 3			
Open-loop voltage amplification	Error	ΔV_O = 3 V, V_O = 0.5 V to 3.5 V	70	95		dB
	Current-limit (TL493 only)			90		
Unity-gain bandwidth				800		kHz
Common-mode rejection ratio	Error	V_{CC} = 40 V, T_A = 25°C	65	80		dB
	Current-limit (TL493 only)			70		
Output sink current (pin 3)		V_{ID} = −15 mV to −5 V, $V_{(pin\ 3)}$ = 0.5 V	0.3	0.7		mA
Output source current (pin 3)		V_{ID} = 15 mV to 5 V, $V_{(pin\ 3)}$ = 3.5 V	−2			mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values except for parameter changes with temperature are at T_A = 25°C.
§Duration of the short-circuit should not exceed one second.
¶Standard deviation is a measure of the statistical distribution about the mean as derived from the formula $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \bar{x})^2}{N-1}}$
*For M-suffix devices these parameters are guaranteed but not tested.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

output section

PARAMETER		TEST CONDITIONS	TL494M			TL493C, TL494I, TL494C, TL495C			UNIT
			MIN	TYP‡	MAX	MIN	TYP†	MAX	
Collector off-state current		V_{CE} = 40 V, V_{CC} = 40 V		2	100		2	100	μA
Emitter off-state current		V_{CC} = V_C = 40 V, V_E = 0			−150			−100	μA
Collector-emitter saturation voltage	Common-emitter	V_E = 0, I_C = 200 mA		1.1	1.5		1.1	1.3	V
	Emitter-follower	V_C = 15 V, I_E = −200 mA		1.5	2.5		1.5	2.5	
Output control input current		V_I = V_{ref}			3.5			3.5	mA

dead-time control section (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input bias current (pin 4)	V_I = 0 to 5.25 V		−2	−10	μA
Maximum duty cycle, each output*	V_I (pin 4) = 0	45			%
Input threshold voltage (pin 4)*	Zero duty cycle		3	3.3	V
	Maximum duty cycle	0			

pwm comparator section (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage (pin 3)*	Zero duty cycle		4	4.5	V
Input sink current (pin 3)	$V_{(pin\ 3)}$ = 0.7 V	0.3	0.7		mA

steering control (TL495 only)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Input current	V_I = 0.4 V		−200	μA
	V_I = 2.4 V		200	

zener-diode circuit (TL495 only)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Breakdown voltage	V_{CC} = 41 V, I_Z = 2 mA		39		V
Sink current	$V_{I(pin\ 15)}$ = 1 V		0.3		mA

total device (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Standby supply current	Pin 6 at V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		6	10	mA
		V_{CC} = 40 V		9	15	
Average supply current	$V_{(pin\ 4)}$ = 2 V			7.5		mA

switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output voltage rise time*	Common-emitter configuration, See Figure 3		100	200	ns
Output voltage fall time*			25	100	ns
Output voltage rise time*	Emitter-follower configuration, See Figure 4		100	200	ns
Output voltage fall time*			40	100	ns

†All typical values except for temperature coefficient are at T_A 25°C
*For M-suffix devices these parameters are guaranteed but not tested.

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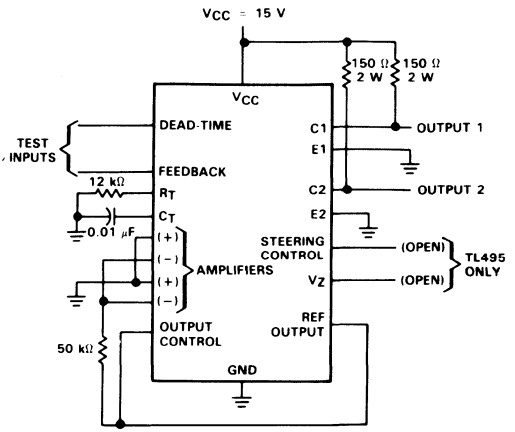
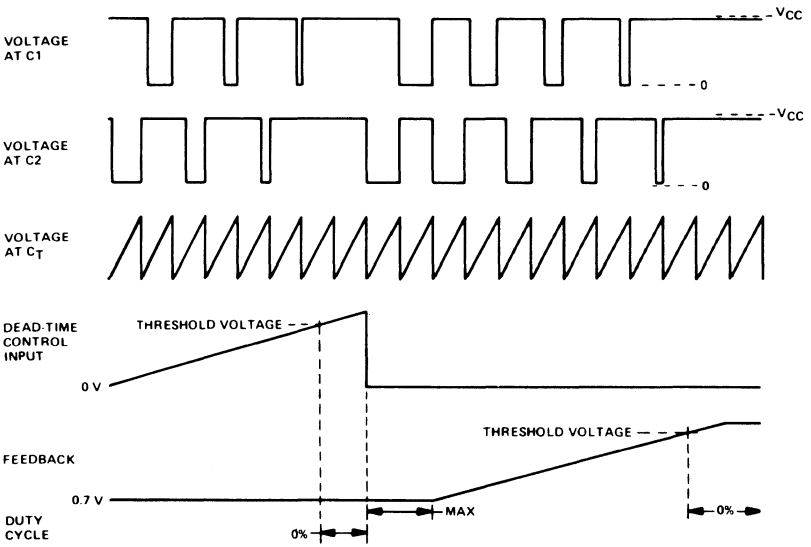
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1–OPERATIONAL TEST CIRCUIT AND WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

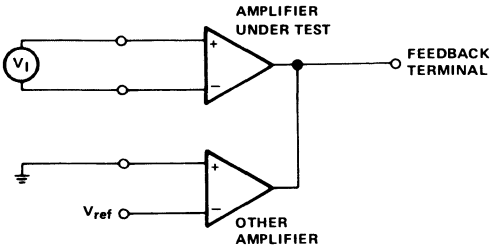
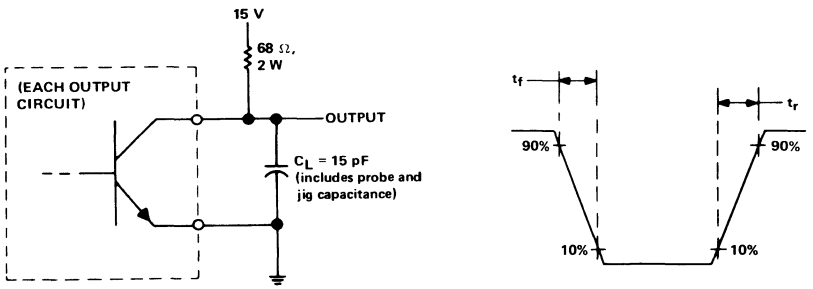


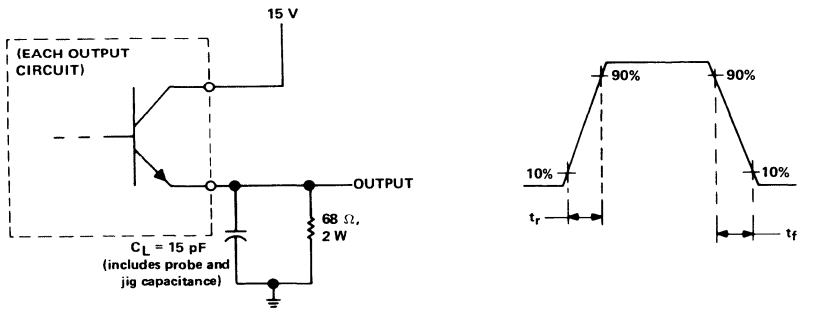
FIGURE 2 – AMPLIFIER CHARACTERISTICS



TEST CIRCUIT

OUTPUT VOLTAGE WAVEFORM

FIGURE 3 – COMMON-EMITTER CONFIGURATION



TEST CIRCUIT

OUTPUT VOLTAGE WAVEFORM

FIGURE 4 – EMITTER-FOLLOWER CONFIGURATION

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY and
FREQUENCY VARIATION† vs
TIMING RESISTANCE

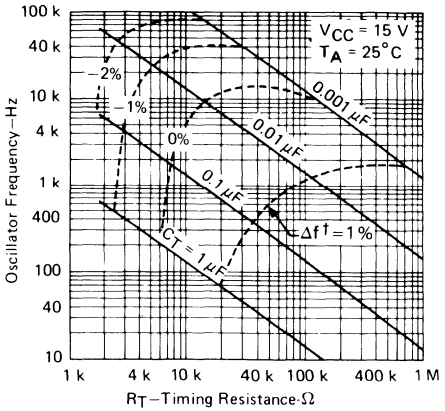


FIGURE 5

AMPLIFIER VOLTAGE AMPLIFICATION
vs
FREQUENCY

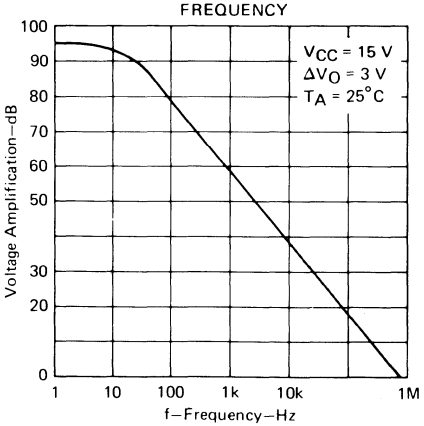


FIGURE 6

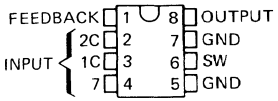
†Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

TYPE TL496C
9-VOLT POWER-SUPPLY CONTROLLER

D2486, AUGUST 1978—REVISED AUGUST 1983

- Internal Step-Up Switching Regulator
- Fixed 9-Volt Output
- Charges Battery Source During Transformer-Coupled-Input Operation
- Minimum External Components Required (1 Inductor, 1 Capacitor, 1 Diode)
- 1- or 2-Cell-Input Operation

P DUAL-IN-LINE PACKAGE
(TOP VIEW)



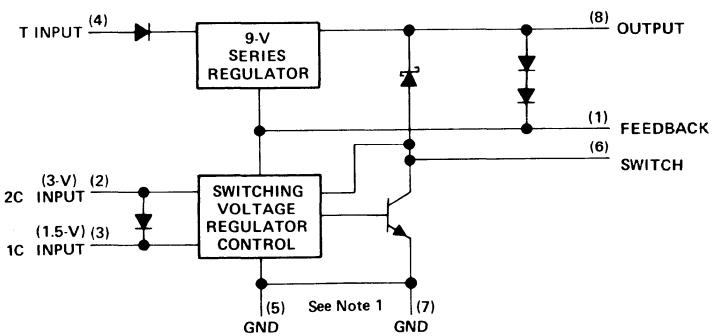
Pins 5 and 7 are connected together internally.

description

The TL496 power supply control circuit is designed to provide a 9-volt regulated supply from a variety of input sources. Operable from a 1- or 2-cell-battery input, the TL496 performs as a switching regulator with the addition of a single inductor and filter capacitor. When ac coupled with a step-down transformer, the TL496 operates as a series regulator to maintain the regulated output voltage and, with the addition of a single catch diode, time shares to recharge the input batteries.

The design of the TL496 allows minimal supply current drain during stand-by operation (125 μA typical). With most battery sources this allows a constant bias to be maintained on the power supply. This makes power instantly available to the system thus eliminating power-up sequencing problems.

functional block diagram



NOTE 1: Pins 5 and 7, though connected together internally, must both be terminated to ground to ensure proper circuit operation.

absolute maximum ratings

Input voltage:
- Pin 2 . . . . . 3.5 V
- Pin 3 . . . . . 2.5 V
- Pin 4 . . . . . 20 V

Output voltage (Pin 6) . . . . . 12 V
Diode reverse voltage (Pin 8) . . . . . 12 V
Switch current (Pin 6) . . . . . 1.2 A
Diode current (Pin 8) . . . . . 1.2 A
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

electrical characteristics at 25°C free-air temperature

series regulator section (input is pin 4)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dropout voltage	V_I = 5 V, I_O = −50 mA			1.5	2	V
Regulated output voltage	V_I = 20 V	I_O = −50 μA	9.5	10.1	11.2	V
		I_O = −80 mA	9.0	10.0	11.0	
	V_I = 20 V, Pin 1 shorted to pin 8	I_O = −50 μA	8.5	9.0	9.7	
		I_O = −80 mA	6.7	8.6	9.5	
Standby current (pin 4)	V_I = 20 V, Pin 8 at 12 V				400	μA
Reverse current thru pin 4	V_I = −1.5 V, 1 mA into Pin 8				−25	μA

output switch

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CE(sat)}$ Collector-emitter saturation voltage	800 mA into Pin 6, Pin 2 at 2.25 V		0.35	0.6	V

diode (pin 6 to pin 8)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_F Forward voltage	I_F = 1.5 A		1.6	2.5	V
I_R Reverse current thru pin 6	Pin 6 at 0 V, 1 mA into Pin 8			−20	μA

control section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
On-state current (pin 2)	Pins 1 and 8 at 0 V, Pin 2 at 3 V		60	100	mA
Standby current (pin 1)	Pin 1 at 8.65 V, Pins 2 and 6 at 3 V			40	μA
Standby current (pin 2 and 6)	Pin 1 at 8.65 V, Pins 2 and 6 at 3 V			400	μA
Start-up current (current into pin 6 to initiate cycle)	Pins 1, 2, 6 and 8 at 2.25 V	16			mA

TYPICAL APPLICATION DATA

CIRCUIT COMPONENT INFORMATION

D1: 1N4001
C_F: 330 to 470 μF, 10 V, electrolytic
L: 40 to 50 μH, Q ≈ 3, R < 0.15 Ω
T1: V_{sec} = 6.8 V RMS typ., R_{sec} = 11 Ω typ.

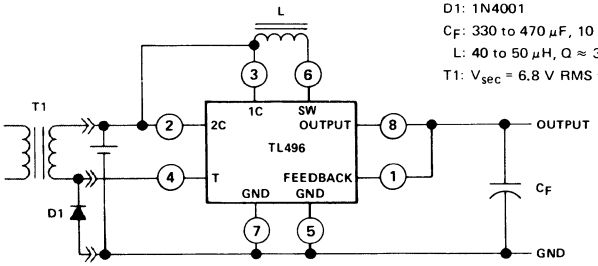


FIGURE 1–ONE-CELL OPERATION

CIRCUIT COMPONENT INFORMATION

D1: 1N4001
C_F: 330 to 470 μF, 10 V electrolytic
L: 40 to 50 μH, Q ≈ 3, R < 0.15 Ω
T1: V_{sec} = 6.8 V RMS typ., R_{sec} = 11 Ω typ.

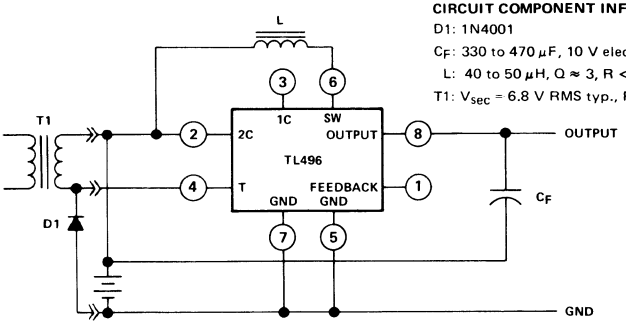


FIGURE 2–TWO-CELL OPERATION

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, one-cell operation (pins 2 and 3 to ground)	1.1	1.5	V
Input voltage, two-cell operation (pin 2 to ground)	2.3	3	V
Input voltage, one-cell or two-cell operation (pin 4 to ground)	V_O+2	20	V

typical electrical characteristics for circuits above

PARAMETER		ONE-CELL OPERATION (FIGURE 1)	TWO-CELL OPERATION (FIGURE 2)
Input current	No load	125 uA	125 uA
	R_L = 120 Ω	525 mA	405 mA
Output voltage	Without T1	7.2 V	8.6 V
	With T1	8.6 V	10 V
Output current capability		40 mA	80 mA
Efficiency		66%	66%
Battery life (AA NiCad) no load		60 days	166 days

functional description

The TL496 is designed to operate from either a single-cell or two-cell source. To operate the device from a single cell (1.1 V to 1.5 V) the source must be connected to both inputs 1C and 2C as shown in Figure 1. For two-cell operation (2.3 V to 3.0 V), the input is applied to the 2C input only and the 1C input is left open (see Figure 2).

battery operation

The TL496 operates as a switching regulator from a battery input. The cycle is initiated when a low voltage condition is sensed by the internal feedback (the thresholds at pin 1 and pin 8 are approximately 7.2 and 8.6 volts respectively). An internal latch is set and the output transistor is turned "on." This causes the current in the external inductor (L) to increase linearly until it reaches a peak value of approximately 1 ampere. When the peak current is sensed the internal latch is reset and the output transistor is turned "off." The energy developed in the inductor is then delivered to the output storage capacitor through the blocking diode. The latch remains in the off state until the feedback signal indicates the output voltage is again deficient.

transformer-coupled operation

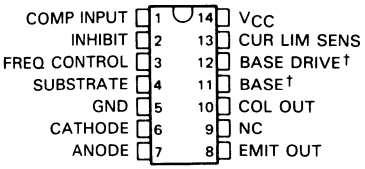
The TL496 operates on alternate half cycles of the ac input during transformer-coupled operation to, first, sustain the output voltage and, second, recharge the batteries. The TL496 performs like a series regulator to supply charge to the output filter/storage capacitor during the first half cycle. The output voltage of the series regulator is slightly higher voltage than that created by the switching circuit; this maintains the feedback voltage above the switching regulator control circuit threshold. This effectively inhibits the switching control circuitry. During the second half cycle an external diode (1N4001) is used to clamp the negative going end of the transformer secondary to ground thus allowing the positive-going end (end connected to V+ side of battery) to pump charge into the stand-by batteries.

TYPES TL497AM, TL497AI, TL497AC
SWITCHING VOLTAGE REGULATORS

D2225, JUNE 1976—REVISED SEPTEMBER 1983

- All Monolithic
- High Efficiency . . . 60% or Greater
- Output Current . . . 500 mA
- Input Current Limit Protection
- TTL Compatible Inhibit
- Adjustable Output Voltage
- Input Regulation . . . 0.2% Typ
- Output Regulation . . . 0.4% Typ
- Soft Start-up Capability

TL497AM . . . J
TL497AI, TL497AC . . . J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

† The Base pin (#11) and Base Drive pin (#12) are used for device testing only. They are not normally used in circuit applications of the device.

description

The TLC497A incorporates on a single monolithic chip all the active functions required in the construction of a switching voltage regulator. It can also be used as the control element to drive external components for high-power-output applications. The TL497A was designed for ease of use in step-up, step-down, or voltage inversion applications requiring high efficiency.

The TL497A is a fixed-on-time variable-frequency switching voltage regulator control circuit. The on-time is programmed by a single external capacitor connected between the frequency control pin and ground. This capacitor, C_T, is charged by an internal constant-current generator to a predetermined threshold. The charging current and the threshold vary proportionally with V_{CC}, thus the one time remains constant over the specified range of input voltage (5 to 12 volts). Typical on-times for various values of C_T are as follows:

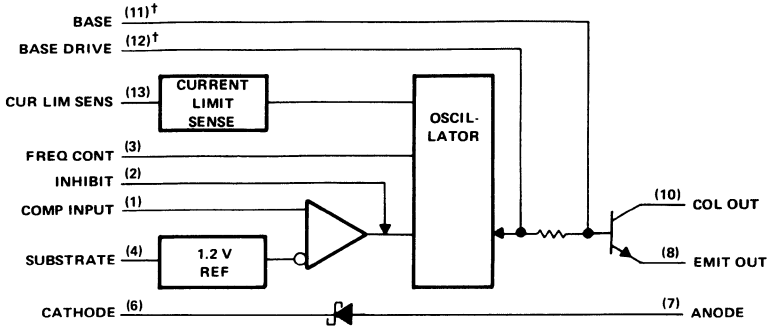
TIMING CAPACITOR, C_T (pF)	200	250	350	400	500	750	1000	1500	2000
ON-TIME (μs)	19	22	26	32	44	56	80	120	180

The output voltage is controlled by an external resistor ladder network (R1 and R2 in Figures 1, 2, and 3) that provides a feedback voltage to the comparator input. This feedback voltage is compared to the reference voltage of 1.2 volts (relative to the substrate pin) by the high-gain comparator. When the output voltage decays below the value required to maintain 1.2 V at the comparator input, the comparator enables the oscillator circuit, which charges and discharges C_T as described above. The internal pass transistor is driven on during the charging of C_T. The internal transistor may be used directly for switching currents up to 500 milliamperes. Its collector and emitter are uncommitted and it is current driven to allow operation from the positive supply voltage or ground. An internal Schottky diode matched to the current characteristics of the internal transistor is also available for blocking or commutating purposes. The TL497A also has on-chip current-limit circuitry that senses the peak currents in the switching regulator and protects the inductor against saturation and the pass transistor against overstress. The current limit is adjustable and is programmed by a single sense resistor, R_{CL}, connected between pin 14 and pin 13. The current-limit circuitry is activated when 0.7 volt is developed across R_{CL}. External gating is provided by the inhibit input. When the inhibit input is high, the output is turned off.

Simplicity of design is a primary feature of the TL497A. With only six external components (three resistors, two capacitors, and one inductor), the TL497A will operate in numerous voltage conversion applications (step-up, step-down, invert) with as much as 85% of the source power delivered to the load. The TL497A replaces the TL497 in all applications.

The TL497AM is characterized for operation over the full military temperature range of −55°C to 125°C, the TL497AI is characterized for operation from −25°C to 85°C, and the TL497AC from 0°C to 70°C.

functional block diagram



†The Base pin (#11) and Base Drive pin (#12) are used for device testing only. They are not normally used in circuit applications of the device.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input voltage, V_{CC} (see Note 1)	15 V
Output voltage	35 V
Comparator input voltage	5 V
Inhibit input voltage	5 V
Diode reverse voltage	35 V
Power switch current	750 mA
Diode forward current	750 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1000 mW
Operating free-air temperature range: TL497AM	−55°C to 125°C
TL497AI	−25°C to 85°C
TL497AC	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values except diode voltages are with respect to network ground terminal.
2. Above 28°C free-air temperature, derate the N package at the rate of 9.2 mW/°C. Above 41°C free-air temperature, derate the J glass-mounted package at the rate of 8.2 mW/°C. Above 59°C free-air temperature, derate the J alloy-mounted package at the rate of 11.0 mW/°C. In the J package, TL4974AM chips are alloy mounted, TL4974AC chips are glass mounted.

recommended operating conditions

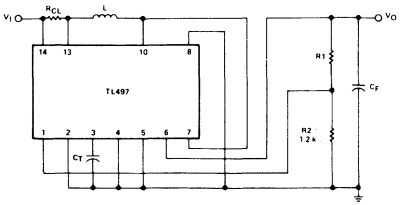
	MIN	MAX	UNIT
Input voltage, V_I	4.5	12	V
Output voltage: step-up configuration (see Figure 1)	$V_I + 2$	30	V
step-down configuration (see Figure 2)	V_{ref}	$V_I - 1$	V
inverting regulator (see Figure 3)	$-V_{ref}$	−25	V
Power switch current		500	mA
Diode forward current		500	mA

electrical characteristics at specified free-air temperature, V_I = 6 V (unless otherwise noted)

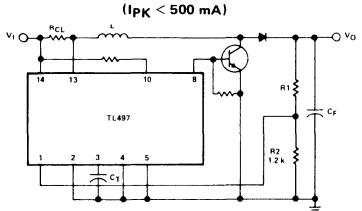
PARAMETER	TEST CONDITIONS†			TL497AM, TL497AI			TL497AC			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
High-level inhibit input voltage			25°C	2.5			2.5			V
Low-level inhibit input voltage			25°C			0.8			0.8	V
High-level inhibit input current	$V_{I(I)}$ = 5 V		Full range		0.8	1.5		0.8	1.5	mA
Low-level inhibit input current	$V_{I(I)}$ = 0 V		Full range		5	20		5	10	μA
Comparator reference voltage	V_I = 4.5 V to 6 V		Full range	1.14	1.20	1.26	1.08	1.20	1.32	V
Comparator input bias current	V_I = 6 V		Full range		40	100		40	100	μA
Switch on-state voltage	V_I = 4.5 V	I_O = 100 mA	25°C		0.13	0.2		0.13	0.2	V
		I_O = 500 mA	Full range			1			0.85	
Switch off-state current	V_I = 4.5 V,	V_O = 30 V	25°C		10	50		10	50	μA
			Full range			500			200	
Current-limit sense voltage	V_I = 6 V		25°C	0.45		1	0.45		1	V
Diode forward voltage	I_O = 10 mA		Full range		0.75	0.95		0.75	0.85	V
	I_O = 100 mA		Full range		0.9	1.1		0.9	1	
	I_O = 500 mA		Full range		1.33	1.75		1.33	1.55	
Diode reverse voltage	I_O = 500 μA		Full range	30						V
	I_O = 200 μA		Full range				30			
On-state supply current			25°C		11	14		11	14	mA
			Full range			16			15	
Off-state supply current			25°C		6	9		6	9	mA
			Full range			11			10	

† Full range for TL497AM is −55°C to 125°C, for TL497AI is −25°C to 85°C, and for TL497AC is 0°C to 70°C.
‡ All typical values are at T_A = 25°C.

TYPICAL APPLICATION DATA



BASIC CONFIGURATION
(I_{PK} < 500 mA)



EXTENDED POWER CONFIGURATION
(USING EXTERNAL TRANSISTOR)

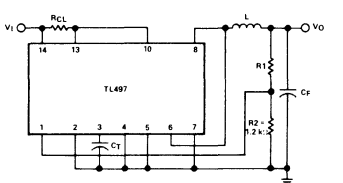
DESIGN EQUATIONS

- $I_{PK} = 2\ I_O\ max \left[\frac{V_O}{V_I}\right]$
- $L\ (\mu H) = \frac{V_I}{I_{PK}}\ t_{on}(\mu s)$

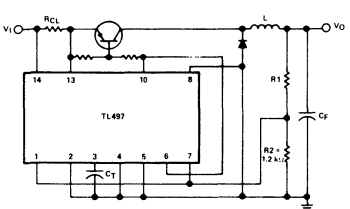
Choose L (50 to 500 μH), calculate t_{on} (25 to 150 μs)

- $C_T(pF) \approx 12\ t_{on}(\mu s)$
- $R1 = (V_O - 1.2)\ k\Omega$
- $R_{CL} = \frac{0.5\ V}{I_{PK}}$
- $C_F\ (\mu F) \approx t_{on}(\mu s)\ \frac{\left[\frac{V_I}{V_O}\ I_{PK} + I_O\right]}{V_{ripple\ (PK)}}$

FIGURE 1–POSITIVE REGULATOR, STEP-UP CONFIGURATIONS



BASIC CONFIGURATION
I_{PK} < 500 mA)



EXTENDED POWER CONFIGURATION
(USING EXTERNAL TRANSISTOR)

DESIGN EQUATIONS

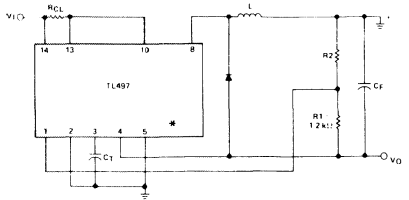
- $I_{PK} = 2\ I_O\ max$
- $L\ (\mu H) = \frac{V_I - V_O}{I_{PK}}\ t_{on}(\mu s)$

Choose L (50 to 500 μH), calculate t_{on} (10 to 150 μs)

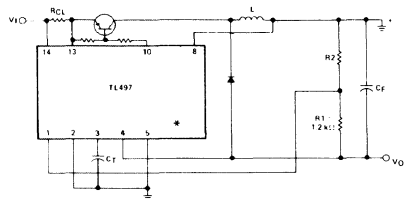
- $C_T(pF) \approx 12\ t_{on}(\mu s)$
- $R1 = (V_O - 1.2)\ k\Omega$
- $R_{CL} = \frac{0.5\ V}{I_{PK}}$
- $C_F(\mu F) \approx t_{on}(\mu s)\ \frac{\left[\frac{V_I}{V_O}\ I_{PK} + I_O\right]}{V_{ripple\ (PK)}}$

FIGURE 2–POSITIVE REGULATOR, STEP-DOWN CONFIGURATIONS

TYPICAL APPLICATION DATA



BASIC CONFIGURATION
(I_{PK} < 500 mA)



EXTENDED POWER CONFIGURATION
(USING EXTERNAL TRANSISTOR)

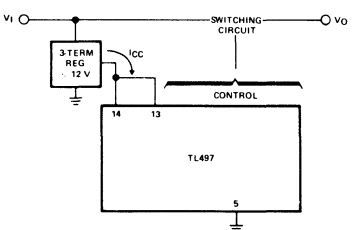
- $I_{PK} = 2\, I_O \text{ max} \left[1 + \frac{|V_O|}{V_I}\right]$
- $L\ (\mu H) = \frac{V_I}{I_{PK}}\, t_{on}(\mu s)$

Choose L (50 to 500 μH), calculate t_{on} (25 to 150 μs)

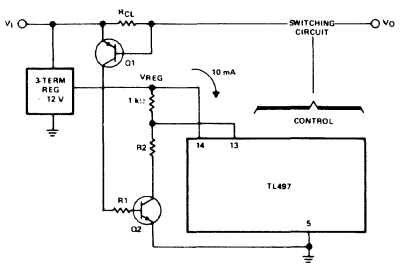
- $C_T(pF) \approx 12\, t_{on}(\mu s)$
- $R2 = (V_O - 1.2)\ k\Omega$
- $R_{CL} = \frac{0.5\ V}{I_{PK}}$
- $C_F\ (\mu F) \approx t_{on}(\mu s)\, \frac{\left[\frac{V_I}{V_O}\, I_{PK} + I_O\right]}{V_{ripple\ (PK)}}$

*Use external catch-diode, e.g., 1N4001, when building an inverting supply with the TL497A.

FIGURE 3–INVERTING APPLICATIONS



EXTENDED INPUT CONFIGURATION WITHOUT CURRENT LIMIT



DESIGN EQUATIONS

$$R_{CL} = \frac{V_{BE(Q1)}}{I_{limit\ (PK)}}$$

$$R1 = \frac{V_I}{I_{B(Q2)}}$$

$$R2 = (V_{reg} - 1)\ 10\ k\Omega$$

CURRENT LIMIT FOR EXTENDED INPUT CONFIGURATION

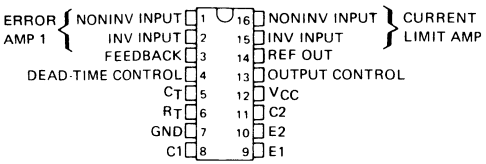
FIGURE 4–EXTENDED INPUT VOLTAGE RANGE (V_I > 15 V)

TYPES TL593, TL594, TL595
PULSE-WIDTH-MODULATION CONTROL CIRCUITS

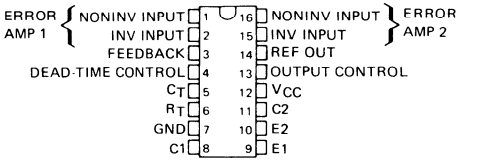
D2712, APRIL 1983 – REVISED DECEMBER 1983

- **Complete PWM Power Control Circuitry**
- **Uncommitted Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Single-Ended or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead-Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply Trimmed to 1%**
- **Circuit Architecture Allows Easy Synchronization**
- **Under-Voltage Lockout for Low V_{CC} Conditions**
- **TL593 has Output Current-Limit Sensing**
- **TL595 has On-Chip 39-V Zener and External Control of Output Steering**
- **Improved Direct Replacements for TL493, TL494, and TL495**

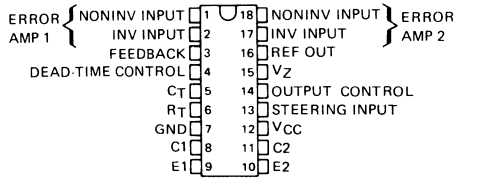
TL593M . . . J
TL593C . . . N
DUAL-IN-LINE PACKAGE (TOP VIEW)



TL594M . . . J
TL594I, TL594C . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



TL595C . . . N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The TL593, TL594, and TL595 devices, each incorporate on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, these devices offer the systems engineer the flexibility to tailor the power supply control circuitry to his application. The TL593, TL594, and TL595 are improved direct replacements for the TL493, TL494, and TL495.

The TL593 contains an error amplifier, current-limiting amplifier, an on-chip adjustable oscillator, a dead-time control comparator, pulse-steering control flip-flop, 5-volt regulator with a precision of 1%, an under-voltage lockout control circuit, and output control circuitry.

The error amplifier exhibits a common-mode voltage range from −0.3 volts to V_{CC} −2 volts. The current-limit amplifier exhibits a common-mode voltage range from −0.3 volts to V_{CC} −6 volts with an offset voltage of approximately 80 millivolts in series with the inverting input to ease circuit design requirements. The dead-time control comparator has a fixed offset that provides approximately 5% dead time when externally altered. The on-chip oscillator may be bypassed by terminating R_T (pin 6) to the reference output and providing a sawtooth input to C_T (pin 5), or it may be used to drive the common circuitry in synchronous multiple-rail power supplies.

DEVICE TYPES, SUFFIX VERSIONS, AND PACKAGES

	TL593	TL594	TL595
TL59–M	J	J	*
TL59–I	*	J,N	*
TL59–C	N	J,N	N

*These combinations are not defined by this data sheet.

FUNCTION TABLE

INPUTS		OUTPUT FUNCTION
OUTPUT CONTROL	STEERING INPUT (TL595 only)	
V_I < 0.4 V	Open	Single ended or parallel output
V_I > 2.4 V	Open	Normal push-pull operation
V_I > 2.4 V	V_I < 0.4 V	PWM Output at Q1
V_I > 2.4 V	V_I > 2.4 V	PWM Output at Q2

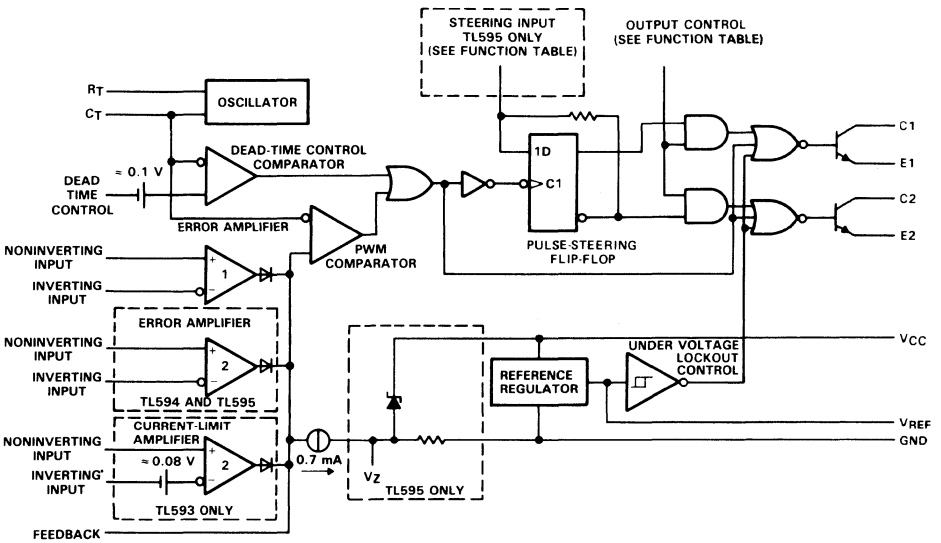
description (continued)

The uncommitted output transistors provide either common-emitter or emitter-follower cutput capability. Each device provides for push-pull or single-ended output operation with selection by means of the output-control function. The architecture of these devices prohibits the possibility of either output being pulsed twice during push-pull operation. The under-voltage lockout control circuit locks the outputs off ur til the internal circuitry is operational.

The TL593 and TL594 are similar except that an additional error amplifier is included in the TL594 instead of a current-limiting amplifier. The TL595 provides the identical functions found in the TL594. In addition, the TL595 also contains an on-chip 39-volt zener diode for high-voltage applications where V_{CC} is greater than 40 volts, and an output steering control that overrides the internal control of the pulse-steering flip-flop.

The TL593M and TL594M are characterized for operation over the full military temperature range from −55°C to 125°C. The TL594I is characterized for operation from −25°C to 85°C. The TL593C, TL594C, and TL595C are characterized for operation from 0°C to 70°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TL593M TL594M	TL594I	TL593C TL594C TL595C	UNIT
Supply voltage, V_{CC} (see Note 1)	41	41	41	V
Amplifier input voltages	$V_{CC}+0.3$	$V_{CC}+0.3$	$V_{CC}+0.3$	V
Collector output voltage	41	41	41	V
Collector output current	250	250	250	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1000	1000	1000	mW
Operating free-air temperature range	−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Table. In the J package, the TL593M and TL594M chips are alloy mounted; TL594I and TL594C chips are glass mounted.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J (Alloy-Mounted Chip)	1000 mW	11.0 mW/°C	59°C
J (Glass-Mounted Chip)	1000 mW	8.2 mW/°C	28°C
N	1000 mW	9.2 mW	41°C

recommended operating conditions

	TL593M TL594M		TL594I		TL593C TL594C TL595C		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	7	40	7	40	7	40	V
Amplifier input voltages, V_I	−0.3	$V_{CC}-2$	−0.3	$V_{CC}-2$	−0.3	$V_{CC}-2$	V
Collector output voltage, V_O		40		40		40	V
Collector output current (each transistor)		200		200		200	mA
Current into feedback terminal		0.3		0.3		0.3	mA
Timing capacitor, C_T	0.47	10 000	0.47	10 000	0.47	10 000	nF
Timing resistor, R_T	1.8	500	1.8	500	1.8	500	kΩ
Oscillator frequency	1	300	1	300	1	300	kHz
Operating free-air temperature, T_A	−55	125	−25	85	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†	TL593M TL594M			TL593C TL594I, TL594C TL595C			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Output voltage (V_{ref})	I_O = 1 mA, T_A = 25°C	4.95	5	5.05	4.95	5	5.05	V
Input regulation	V_{CC} = 7 V to 40 V, T_A = 25°C		2	25		2	25	mV
Output regulation	I_O = 1 to 10 mA, T_A = 25°C		14	35		14	35	mV
Output voltage change with temperature*	ΔT_A = MIN to MAX		0.2	1		0.2	1	%
Short-circuit output current§	V_{ref} = 0	10	35	60	10	35	50	mA

oscillator section (see Figure 2)

PARAMETER	TEST CONDITIONS†	TL593M TL594M			TL593C TL594I, TL594C TL595C			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Frequency			10			10		kHz
Standard deviation of frequency¶	All values of V_{CC}, C_T, R_T, T_A constant		10			10		%
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		0.1			0.1		%
Frequency change with temperature	ΔT_A = MIN to MAX			12			12	%

amplifier sections (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Input offset voltage	Error	Feedback pin at 2.5 V		2	10	mV
	current-limit (TL593 only)			80		
Input offset current		Feedback control at 2.5 V		25	250	nA
Input bias current		Feedback control at 2.5 V		0.2	1	μA
Common-mode input voltage range	Error	V_{CC} = 7 V to 40 V	−0.3 to V_{CC} − 2			V
	Current-limit (TL593 only)		−0.3 to V_{CC} − 6			
Open-loop voltage amplification	Error	ΔV_O = 3 V, V_O = 0.5 V to 3.5 V	70	95		dB
	Current-limit (TL593 only)			90		
Unity-gain bandwidth				800		kHz
Common-mode rejection ratio	Error	V_{CC} = 40 V, T_A = 25°C	65	80		dB
	Current-limit (TL593 only)			70		
Output sink current (pin 3)		V_{ID} = −15 mV to −5 V, Feedback control at 0.5 V	0.3	0.7		mA
Output source current (pin 3)		V_{ID} = 15 mV to 5 V, Feedback at 3.5 V	−2			mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values except for parameter changes with temperature are at T_A = 25°C.
§Duration of the short-circuit should not exceed one second.
¶Standard deviation is a measure of the statistical distribution about the mean as derived from the formula $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \bar{X})^2}{N-1}}$
*For M-suffix devices these parameters are guaranteed but not tested.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

dead-time control section (see Figure 2)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Input bias current (pin 4)	V_I = 0 to 5.25 V		−2	−10	μA
Maximum duty cycle, each output *	Dead-time control at 0 V	45			%
Input threshold voltage (pin 4)*	Zero duty cycle		3	3.3	V
	Maximum duty cycle	0			

output section

PARAMETER		TEST CONDITIONS	TL593M TL594M MIN	TL593M TL594M TYP‡	TL593M TL594M MAX	TL593C TL594I, TL594C TL595C MIN	TL593C TL594I, TL594C TL595C TYP‡	TL593C TL594I, TL594C TL595C MAX	UNIT
Collector off-state current		V_{CE} = 40 V, V_{CC} = 40 V		2	100		2	100	μA
		V_C = 15 V, V_E = 0 V, V_{CC} = 1 to 3 V, Dead-time and output control pins at 0 V		4	200		4	200	
Emitter off-state current		V_{CC} = V_C = 40 V, V_E = 0		−150			−100		μA
Collector-emitter saturation voltage	Common-emitter	V_E = 0, I_C = 200 mA		1.1	1.5		1.1	1.3	V
	Emitter-follower	V_C = 15 V, I_E = −200 mA		1.5	2.5		1.5	2.5	
Output control input current		V_I = V_{ref}			3.5			3.5	mA

pwm comparator section (see Figure 2)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Input threshold voltage (pin 3)*	Zero duty cycle		4	4.5	V
Input sink current (pin 3)	$V_{(pin\ 3)}$ = 0.5 V	0.3	0.7		mA

under-voltage lockout section (see Figure 2)

PARAMETER	TEST CONDITIONS†	TL593M TL594M MIN	TL593M TL594M TYP	TL593M TL594M MAX	TL593C TL594I, TL594C TL595C MIN	TL593C TL594I, TL594C TL595C TYP	TL593C TL594I, TL594C TL595C MAX	UNIT
Threshold voltage	T_A = 25°C			6			6	V
	ΔT_A = MIN to MAX	3		6.9	3.5		6.9	
Hysteresis‖		30			100			mV

total device (see Figure 2)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
Standby supply current	Pin 6 at V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		9	15	mA
		V_{CC} = 40 V		11	18	
Average supply current	Dead-time Control at 2 V, See Figure 2			12.4		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values except for parameter changes with temperature are at T_A = 25°C.
‖Hysteresis is the difference between the positive-going input threshold voltage and the negative-going input threshold voltage.
*For M-suffix devices these parameters are guaranteed but not tested.

switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Output voltage rise time *	Common-emitter configuration,		100	200	ns
Output voltage fall time *	See Figure 3		30	100	
Output voltage rise time *	Emitter-follower configuration,		200	400	ns
Output voltage fall time *	See Figure 4		45	100	

‡All typical values are at T_A = 25°C.
*For M-suffix devices these parameters are guaranteed but not tested.

PARAMETER MEASUREMENT INFORMATION

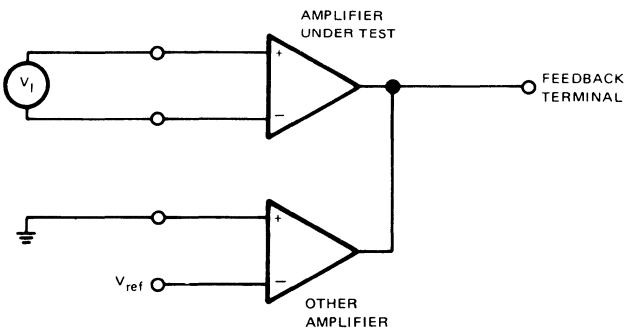
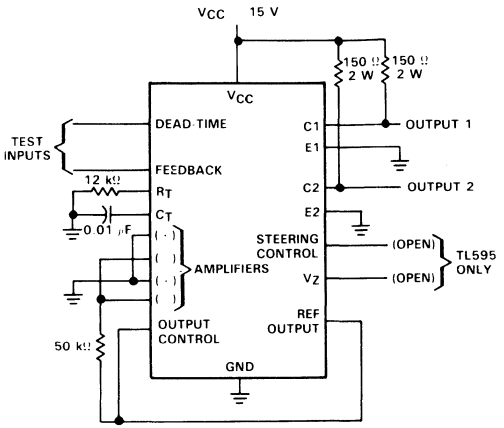
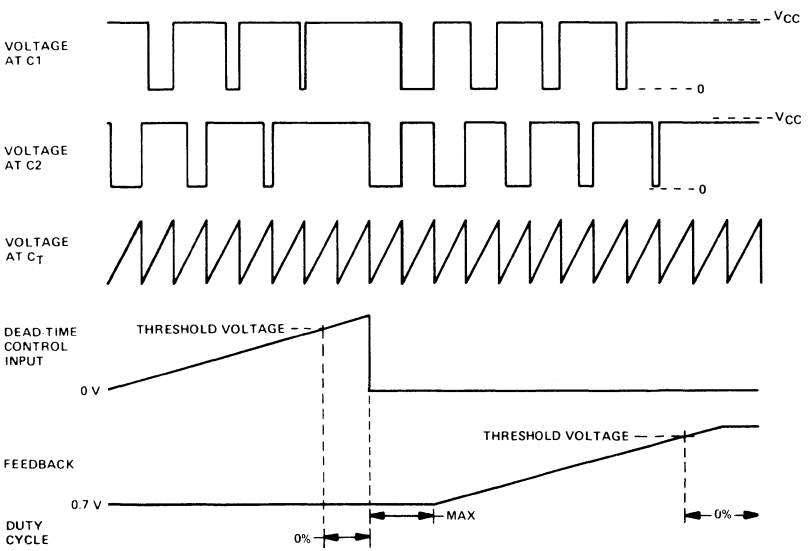


FIGURE 1 — AMPLIFIER CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



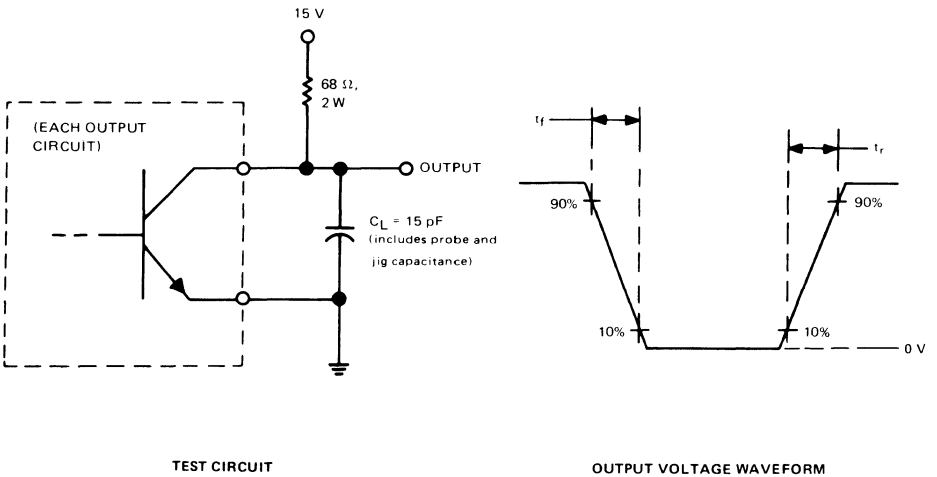
TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2–OPERATIONAL TEST CIRCUIT AND WAVEFORMS

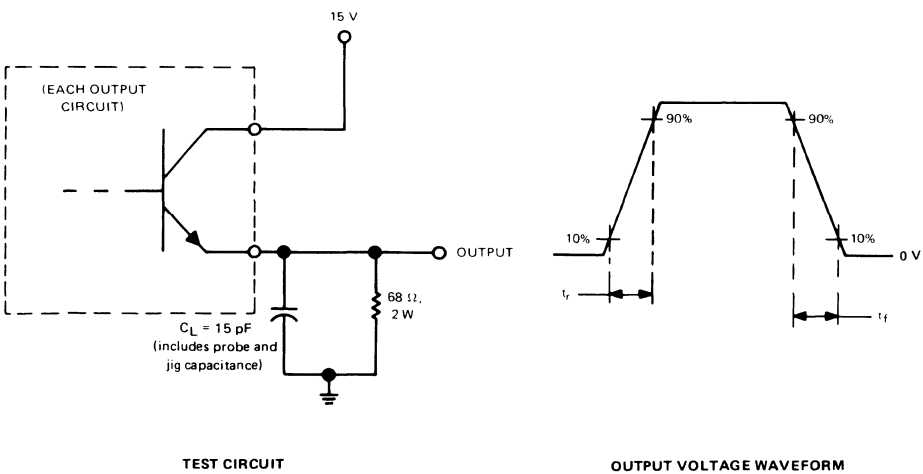
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

OUTPUT VOLTAGE WAVEFORM

FIGURE 3–COMMON-EMITTER CONFIGURATION



TEST CIRCUIT

OUTPUT VOLTAGE WAVEFORM

FIGURE 4–EMITTER-FOLLOWER CONFIGURATION

TYPICAL CHARACTERISTICS

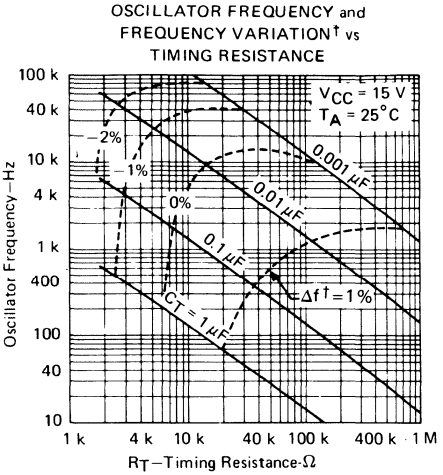


FIGURE 5

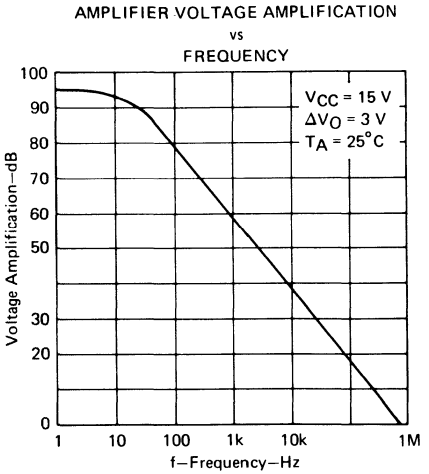


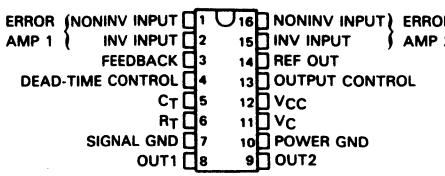
FIGURE 6

†Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

D3026, FEBRUARY 1988—REVISED OCTOBER 1988

- **Complete PWM Power Control Function**
- **Totem-Pole Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Parallel or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead-Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply, Trimmed to 1% Tolerance**
- **On-Board Output Current-Limiting Protection**
- **Under-Voltage Lockout for Low V_{CC} Conditions**
- **Independent Power and Signal Grounds**
- **TL598Q Has Extended Temperature Range . . . −40°C to 125°C**

D, J, OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUT	
OUTPUT CONTROL	OUTPUT FUNCTION
V_I = GND	Single-ended or parallel output
V_I = V_{ref}	Normal push-pull operation

description

The TL598 incorporates all the functions required in the construction of pulse-width-modulated controlled systems on a single monolithic chip. Designed primarily for power supply control, the TL598 provides the systems engineer with the flexibility to tailor the power supply control circuits to a specific application.

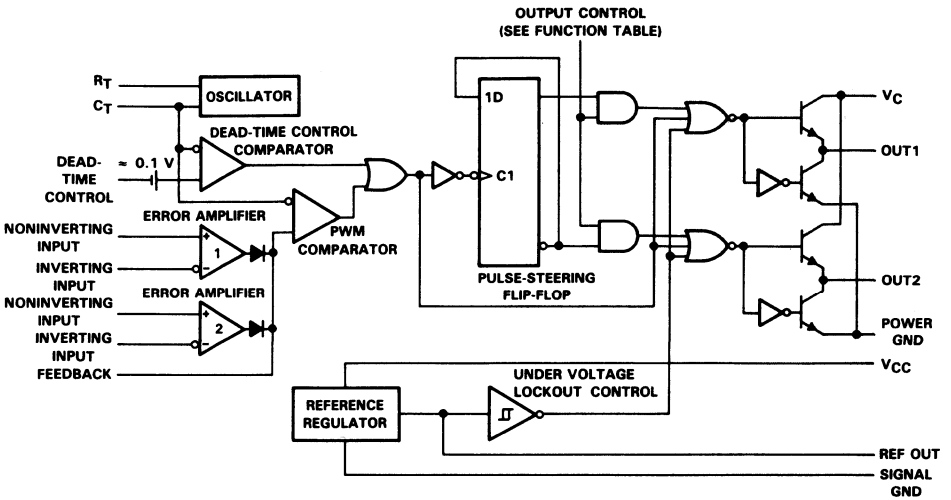
The TL598 contains two error amplifiers, an internal oscillator (externally adjustable), a dead-time control comparator, a pulse-steering flip-flop, a 5-V precision reference, an under-voltage lockout control, and output control circuits. Two totem-pole outputs provide exceptional rise and fall time performance for power FET control. The outputs are designed with the collectors sharing a common source supply and common power grounds and are independent of V_{CC} and signal ground.

The error amplifier has a common-mode voltage range from −0.3 V to V_{CC} −2 V. The dead-time control comparator has a fixed offset that prevents overlap of the outputs during push-pull operation. Synchronous multiple supply operation may be achieved by connecting pin 6 to the reference output and providing a sawtooth input to pin 5.

The TL598 device provides an output control function to select either push-pull or parallel operation. Circuit architecture prevents either output from being pulsed twice during push-pull operation.

The TL598Q is characterized for operation from −40°C to 125°C. The TL598C is characterized for operation from 0°C to 70°C.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 41 V
Amplifier input voltage, V_I . . . . . $V_{CC}+0.3$ V
Collector voltage . . . . . 41 V
Output current (each output), sink or source, I_O . . . . . 250 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J: TL598Q . . . . . −40°C to 150°C
TL598C . . . . . 0°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A	T_A = 70°C POWER RATING	T_A = 125°C POWER RATING
D	950 mW	7.6 mW/°C	25°C	608 mW	190 mW
N	1200 mW	13 mW/°C	58°C	1040 mW	325 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		7	40	V
Amplifier input voltage, V_I		−0.3	$V_{CC}-2$	V
Collector voltage			40	V
Output current (each output), sink or source, I_O			200	mA
Current into feedback terminal, I_{IL}			0.3	mA
Timing capacitor, C_T		0.00047	10	μF
Timing resistor, R_T		1.8	500	kΩ
Oscillator frequency, f_{osc}		1	300	kHz
Free-air temperature, T_A	TL598Q	−40	125	°C
	TL598C	0	70	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted), see Note 2

reference section

PARAMETER	TEST CONDITIONS†		TL598Q MIN	TL598Q TYP‡	TL598Q MAX	TL598C MIN	TL598C TYP‡	TL598C MAX	UNIT
Output voltage (V_{ref})	I_O = 1 mA,	T_A = 25°C	4.95	5	5.05	4.95	5	5.05	V
		T_A = MIN to MAX	4.9		5.1	4.9		5.1	
Input regulation	V_{CC} = 7 V to 40 V,	T_A = 25°C		2	22		2	25	mV
Output regulation	I_O = 1 to 10 mA,	T_A = 25°C		1	15		1	15	mV
		T_A = MIN to MAX			80				
Output voltage change with temperature	ΔT_A = MIN to MAX			0.2	1		0.2	1	%
Short-circuit output current§	V_{ref} = 0		−10	−35		−10	−35		mA

oscillator section (see Figure 1) C_T = 0.001 μF, R_T = 12 kΩ

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
Frequency			100		kHz
Standard deviation of frequency¶	All values of V_{CC}, C_T, R_T, T_A constant		10		%
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		0.1	1	%
Frequency change with temperature#	ΔT_A = MIN to MAX		2	5	%

error amplifier section

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
Input offset voltage	Feedback pin at 2.5 V			2	10	mV
Input offset current	Feedback pin at 2.5 V			25	250	nA
Input bias current	Feedback pin at 2.5 V			0.2	1	μA
Common-mode input voltage range	V_{CC} = 7 V to 40 V		−0.3 to V_{CC}−2			V
Open-loop voltage amplification	ΔV_O (pin 3) = 3 V,	V_O (pin 3) = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth				800		kHz
Common-mode rejection ratio	V_{CC} = 40 V,	ΔV_{IC} = 36.5 V, T_A = 25°C	65	80		dB
Output sink current (pin 3)	Feedback pin at 0.5 V		0.3	0.7		mA
Output source current (pin 3)	Feedback pin at 3.5 V		−2			mA
Phase margin at unity gain	Feedback pin = 0.5 V to 3.5 V, R_L = 2 kΩ			65°		
Supply voltage rejection ratio	Feedback pin at 2.5 V,	ΔV_{CC} = 33 V, R_L = 2 kΩ		100		dB

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
§ Duration of the short-circuit should not exceed one second.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - X)^2}{N-1}}$
# Effects of temperature on external R_T and C_T are not taken into account.

NOTE 2: Pulse testing techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted), see Note 2

under-voltage lockout section

PARAMETER	TEST CONDITIONS†	TL598Q		TL598C		UNIT
		MIN	MAX	MIN	MAX	
Threshold voltage	T_A = 25°C	4	6	4	6	V
	ΔT_A = MIN to MAX	3.8	6.9	3	6.9	
Hysteresis‡	T_A = 25°C	100		100		mV
	T_A = MIN to MAX	30		50		

output section

PARAMETER	TEST CONDITIONS		MIN	TYP§	MAX	UNIT
Collector off-state current	V_{CE} = 40 V, V_{CC} = 40 V, Dead-time pin is connected to REF			2	100	μA
High-level output voltage	V_{CC} = 15 V,	I_O = −200 mA	12			V
	V_C = 15 V,	I_O = −20 mA	13			
Low-level output voltage	V_{CC} = 15 V,	I_O = 200 mA			2	V
	V_C = 15 V,	I_O = 20 mA			0.4	
Output control input current	V_I = V_{ref}				3.5	mA
	V_I = 0.4 V				100	μA

dead-time control section (see Figure 1)

PARAMETER	TEST CONDITIONS	TL598Q			TL598C			UNIT
		MIN	TYP§	MAX	MIN	TYP§	MAX	
Input bias current (pin 4)	V_I = 0 to 5.25 V		−2	−25		−2	−10	μA
Maximum duty cycle, each output	Dead-time control at 0 V	45			45			%
Input threshold voltage (pin 4)	Zero duty cycle		3	3.2		3	3.3	V
	Maximum duty cycle	0			0			

pwm comparator section

PARAMETER	TEST CONDITIONS	MIN	UNIT
Input threshold voltage (pin 3)	Zero duty cycle		V
Input sink current (pin 3)	$V_{(pin\ 3)}$ = 0.5 V	0.3	mA

total device (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	TYP§	MAX	UNIT
Standby supply current	Pin 6 at V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		15	21	mA
		V_{CC} = 40 V		17	23	
Average supply current	Dead-time control at 2 V			15		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡Hysteresis is the difference between the positive-going input threshold voltage and the negative-going input threshold voltage.
§All typical values except for parameter changes with temperature are at T_A = 25°C
NOTE 2: Pulse testing techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage rise time	C_L = 1500 pF,			100	150	ns
Output voltage fall time	V_C = 15 V,	V_{CC} = 15 V, See Figure 2		50	75	ns

PARAMETER MEASUREMENT INFORMATION

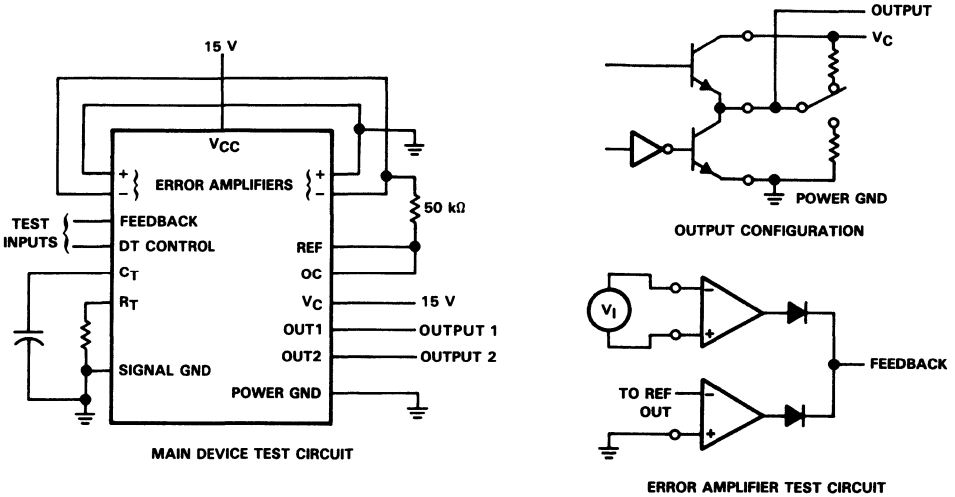


FIGURE 1. TEST CIRCUITS

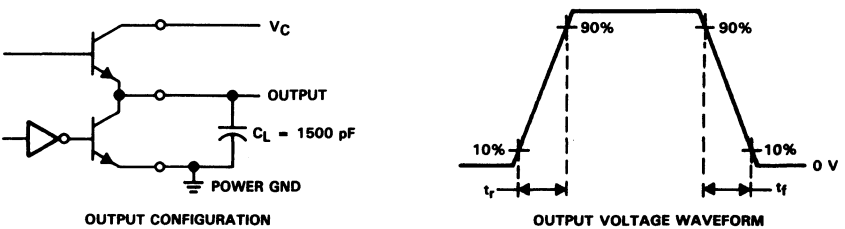


FIGURE 2. SWITCHING OUTPUT CONFIGURATION AND VOLTAGE WAVEFORM

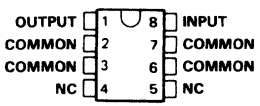
D3017, SEPTEMBER 1987—REVISED FEBRUARY 1988

- Very Low Dropout Voltage, Less than 0.6 V at 150 mA
- Very Low Quiescent Current
- TTL- and CMOS-Compatible Enable On TL751L Series
- 60-V Load-Dump Protection
- Reverse Transient Protection to −50 V
- Internal Thermal Overload Protection
- Over-Voltage Protection
- Internal Over-Current Limiting Circuitry

terminal assignments

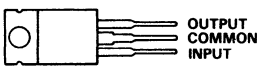
TL750L . . . D
SMALL OUTLINE PACKAGE

(TOP VIEW)



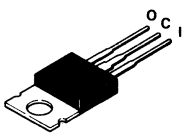
TL750L . . . KC
HEAT-SINK-MOUNTED PACKAGE

(TOP VIEW)



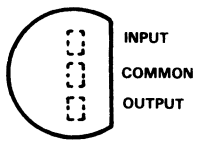
THE COMMON TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

TO-220AB



TL750L . . . LP
SILECT™ PACKAGE

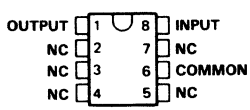
(TOP VIEW)



TO-226AA

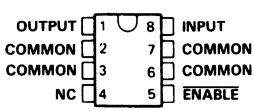
TL750L . . . P
DUAL-IN-LINE PACKAGE

(TOP VIEW)



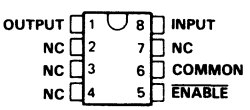
TL751L . . . D
SMALL OUTLINE PACKAGE

(TOP VIEW)



TL751L . . . P
DUAL-IN-LINE PACKAGE

(TOP VIEW)



NC—No internal connection
SILECT is a trademark of Texas Instruments Incorporated.

description

The TL750L and TL751L series are low-dropout positive voltage regulators specifically designed for battery-powered systems. The TL750L and the TL751L incorporate over-voltage and current-limiting protection circuitry along with internal reverse-battery protection circuitry to protect both itself and the regulated system. Both series are fully protected against 60-volt load-dump and reverse-battery conditions. Extremely low quiescent current during full-load conditions makes the TL750L and TL751L series ideal for standby power systems.

The TL750L series of fixed-output voltage regulators offer 5-volt, 8-volt, 10-volt, and 12-volt options. They are available in TO-226AA (formerly TO-92) (LP) packages, TO-220AB (KC) packages, 8-pin "small outline" plastic packages (D), and 8-pin plastic dual-in-line packages (P).

The TL751L series of fixed-output voltage regulators also offer 5-volt, 8-volt, 10-volt, and 12-volt options with the addition of an enable input. The enable input, when taken high, places the regulator output in a high-impedance state. This gives the designer complete control over power up, power down, or emergency shut down. This series is offered in the 8-pin "small outline" plastic package and the 8-pin plastic dual-in-line package.

absolute maximum ratings over operating junction temperature range (unless otherwise noted)

		TL750L	TL751L	UNIT
Continuous input voltage		26	26	V
Transient input voltage, T_A = 25°C (see Note 1)		60	60	V
Continuous reverse input voltage		−15	−15	V
Transient reverse input voltage: t ≤ 100 ms		−50	−50	V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1):	D package	825	825	mW
	KC package	2000		
	LP package	775		
	P package	1000	1000	
Operating virtual junction temperature range		−40 to 150	−40 to 150	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) for 10 seconds		260	260	°C

NOTES: 1. The transient input voltage rating applies for the waveform described in Figure 1.
2. For operation above 25°C free-air temperature, linearly derate the D package at the rate of 6.6 mW/°C, the KC package at 15.2 mW/°C, the LP package at 6.2 mW/°C, and the P package at 8 mW/°C.

recommended operating conditions over recommended operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNITS
Input voltage, V_I	TL75_L05	6	26	V
	TL75_L08	9	26	
	TL75_L10	11	26	
	TL75_L12	13	26	
High-level $\overline{\text{ENABLE}}$ input voltage, V_{IH}	TL751L	2	15	V
Low-level $\overline{\text{ENABLE}}$ voltage, V_{IL}†	TL751L	−0.3	0.8	V
Output current, I_O	TL75_L	0	150	mA
Operating virtual junction temperature, T_J	TL75_L_C	0	125	°C
	TL75_L_Q	−40	125	

†The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for $\overline{\text{ENABLE}}$ voltage levels and temperature only.

TL750L05 and TL751L05 electrical characteristics at 25°C virtual junction temperature, V_I = 14 V, I_O = 10 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 6 V to 26 V,	T_J = 25°C	4.80	5	5.2	V
	I_O = 0 to 150 mA	T_J = T_J min to 125°C	4.75		5.25	
Input regulation	V_I = 9 V to 16 V			5	10	mV
	V_I = 6 V to 26 V			6	30	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz		60	65		dB
Output regulation	I_O = 5 mA to 150 mA			20	50	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Bias current	I_O = 150 mA			10	12	mA
	V_I = 6 V to 26 V,	I_O = 10 mA, T_J = T_J min to 125°C		1	2	

TL750L08 and TL751L08 electrical characteristics at 25°C virtual junction temperature, V_I = 14 V, I_O = 10 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 9 V to 26 V,	T_J = 25°C	7.8	8	8.2	V
	I_O = 0 to 150 mA	T_J = T_J min to 125°C	7.6		8.4	
Input regulation	V_I = 10 V to 17 V			10	20	mV
	V_I = 9 V to 26 V			25	50	
Ripple rejection	V_I = 11 V to 21 V, f = 120 Hz		60	65		dB
Output regulation	I_O = 5 mA to 150 mA			40	80	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Bias current	I_O = 150 mA			10	12	mA
	V_I = 9 V to 26 V,	I_O = 10 mA, T_J = T_J min to 125°C		1	2	

TL750L10 and TL751L10 electrical characteristics at 25°C virtual junction temperature, V_I = 14 V, I_O = 10 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 11 V to 26 V,	T_J = 25°C	9.75	10	10.25	V
	I_O = 0 to 150 mA	T_J = T_J min to 125°C	9.50		10.50	
Input regulation	V_I = 12 V to 19 V			10	25	mV
	V_I = 11 V to 26 V			30	60	
Ripple rejection	V_I = 12 V to 22 V, f = 120 Hz		60	65		dB
Output regulation	I_O = 5 mA to 150 mA			50	100	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			700		μV
Bias current	I_O = 150 mA			10	12	mA
	V_I = 11 V to 26 V,	I_O = 10 mA, T_J = T_J min 125°C		1	2	

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 1 ohm, across the output.

TL750L12 and TL751L12 electrical characteristics at 25°C virtual junction temperature, V_I = 14 V, I_O = 10 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 13 V to 26 V,	T_J = 25°C	11.7	12	12.3	V
	I_O = 0 to 150 mA	T_J = T_J min to 125°C	11.4		12.6	
Input regulation	V_I = 14 V to 19 V			15	30	mV
	V_I = 13 V to 26 V			20	40	
Ripple rejection	V_I = 13 V to 23 V,	f = 120 Hz	50	55		dB
Output regulation	I_O = 5 mA to 150 mA			50	120	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			700		μV
Bias current	I_O = 150 mA			10	12	mA
	V_I = 13 V to 26 V,	I_O = 10 mA, T_J = T_J min to 125°C		1	2	

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 1 ohm, across the output.

ABSOLUTE MAXIMUM RATINGS

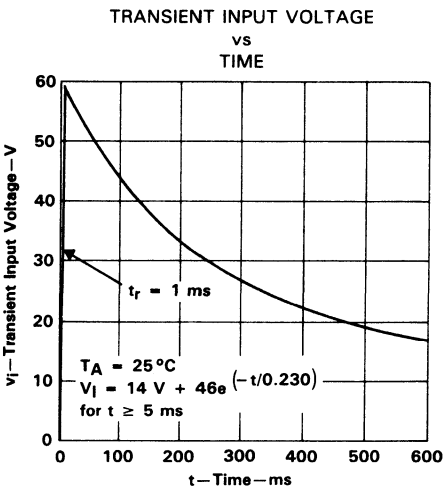


FIGURE 1

D3017, JANUARY 1988

- **Very Low Dropout Voltage, Less than 0.6 V at 750 mA**
- **Low Quiescent Current**
- **TTL- and CMOS-Compatible Enable on TL751M Series**
- **60-V Load-Dump Protection**
- **Over-Voltage Protection**
- **Internal Thermal Overload Protection**
- **Internal Over-Current Limiting Circuitry**

description

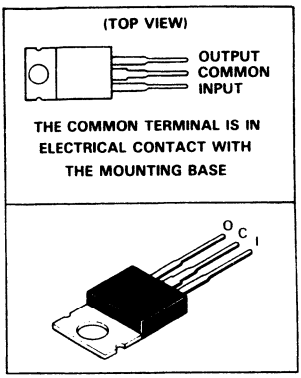
The TL750M and TL751M series are low-dropout positive voltage regulators specifically designed for battery-powered systems. The TL750M and TL751M incorporate on-board over-voltage and current-limit protection circuitry to protect both themselves and the regulated system. Both series are fully protected against 60-V load-dump and reverse battery conditions. Extremely low quiescent current, even during full-load conditions, makes the TL750M and TL751M series ideal for standby power systems.

The TL750M series of fixed-output voltage regulators offer 5-V, 8-V, 10-V, and 12-V options available in 3-lead KC (TO-220AB) plastic packages.

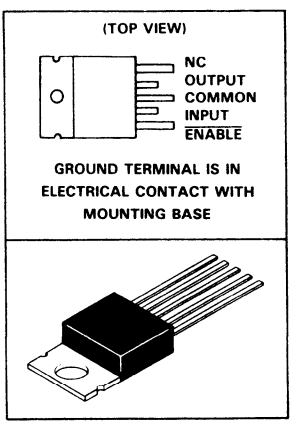
The TL751M series of fixed-output voltage regulators also offer 5-V, 8-V, 10-V, and 12-V options with the addition of an enable input. The enable input gives the designer complete control over power-up, allowing for sequential power-up or emergency shutdown. When taken high, the enable input places the regulator output in a high-impedance state. It is completely TTL- and CMOS-compatible. The TL751M series is offered in 5-lead KC plastic packages.

The TL750M and TL751M series are characterized for operation from −40°C to 125°C free-air temperature.

3-LEAD KC (TO-220AB) PACKAGE



5-LEAD KC PACKAGE



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Continuous input voltage . . . . . 26 V
Transient input voltage (see Figure 1) . . . . . 60 V
Continuous reverse input voltage . . . . . −15 V
Transient reverse input voltage: t = 100 ms . . . . . −50 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1) . . . . . 2 W
Continuous total dissipation at (or below) 25°C case temperature (see Note 1) . . . . . 20 W
Operating free-air, case, or virtual junction temperature . . . . . −40°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

Note 1: For operation above 25°C free-air temperature, refer to Figures 2 and 3. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions over recommended operating free-air temperature range (unless otherwise noted)

	DEVICE	MIN	MAX	UNITS
Input voltage range, V_I	TL75_M05	6	26	V
	TL75_M08	9	26	
	TL75_M10	11	26	
	TL75_M12	13	26	
High-level ENABLE input voltage, V_{IH}	TL751M_	2	15	V
Low-level ENABLE input voltage, V_{IL} (see Note 2)	TL751M_	−0.3	0.8	
Output current range, I_O	TL75_M		750	mA
Operating virtual junction temperature range, T_J	TL75_M_C	0	125	°C
	TL75_M_Q	−40	125	

Note 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for $\overline{\text{ENABLE}}$ voltage levels and temperature only.

TL750M05 and TL751M05 electrical characteristics at 25°C free-air temperature, V_I = 14V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M05 (unless otherwise noted)

PARAMETER	TEST CONDITIONS (see Note 3)		MIN	TYP	MAX	UNIT
Output voltage	V_I = 6 V to 26 V, I_O = 0 to 750 mA	T_A = 25°C	4.95	5	5.05	V
		T_A = T_J min to 125°C	4.9		5.1	
Input regulation	V_I = 9 V to 16 V, I_O = 250 mA			10	25	mV
	V_I = 6 V to 26 V, I_O = 250 mA			12	50	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz			55		dB
Output regulation	I_O = 5 mA to 750 mA			20	50	mV
Dropout voltage	I_O = 500 mA				0.5	V
	I_O = 750 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Bias current	I_O = 750 mA			60		mA
	I_O = 10 mA				5	

NOTE 3: Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 1 Ω, across the output.

TL750M08 and TL751M08 electrical characteristics at 25°C free-air temperature, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M08 (unless otherwise noted)

PARAMETER	TEST CONDITIONS (see Note 3)		MIN	TYP	MAX	UNIT
Output voltage	V_I = 9 V to 26 V, I_O = 0 to 750 mA	T_A = 25°C	7.92	8	8.08	V
		T_A = T_J min to 125°C	7.84		8.16	
Input regulation	V_I = 10 V to 17 V, I_O = 250 mA			12		mV
	V_I = 9 V to 26 V, I_O = 250 mA			15		
Ripple rejection	V_I = 11 V to 21 V, f = 120 Hz			55		dB
Output regulation	I_O = 5 mA to 750 mA			24		mV
Dropout voltage	I_O = 500 mA				0.5	V
	I_O = 750 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Bias current	I_O = 750 mA			60		mA
	I_O = 10 mA				5	

TL750M10 and TL751M10 electrical characteristics at 25°C free-air temperature, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M10 (unless otherwise noted)

PARAMETER	TEST CONDITIONS (see Note 3)		MIN	TYP	MAX	UNIT
Output voltage	V_I = 11 V to 26 V, I_O = 0 to 750 mA	T_A = 25°C	9.9	10	10.1	V
		T_A = T_J min to 125°C	9.8		10.2	
Input regulation	V_I = 12 V to 18 V, I_O = 250 mA			15		mV
	V_I = 11 V to 26 V, I_O = 250 mA			20		
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		55	60		dB
Output regulation	I_O = 5 mA to 750 mA			30		mV
Dropout voltage	I_O = 500 mA				0.5	V
	I_O = 750 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			1000		μV
Bias current	I_O = 750 mA			60		mA
	I_O = 10 mA				5	

TL750M12 and TL751M12 electrical characteristics at 25°C free-air temperature, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M12 (unless otherwise noted)

PARAMETER	TEST CONDITIONS (see Note 3)		MIN	TYP	MAX	UNIT
Output voltage	V_I = 13 V to 26 V, I_O = 0 to 750 mA	T_A = 25°C	11.88	12	12.12	V
		T_A = T_J min to 125°C	11.76		12.24	
Input regulation	V_I = 14 V to 19 V, I_O = 250 mA			15		mV
	V_I = 13 V to 26 V, I_O = 250 mA			20		
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		55	60		dB
Output regulation	I_O = 5 mA to 750 mA			30		mV
Dropout voltage	I_O = 500 mA				0.5	V
	I_O = 750 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			1000		μV
Bias current	I_O = 750 mA			60		mA
	I_O = 10 mA				5	

NOTE 3: Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 1 Ω, across the output.

TL751Mxx electrical characteristics at 25°C free-air temperature, V_I = 14 V, I_O = 300 mA

PARAMETER	MIN	TYP	MAX	UNIT
Response time, $\overline{\text{ENABLE}}$ to output		50		μs

MAXIMUM RATINGS

TRANSIENT INPUT VOLTAGE
vs
TIME

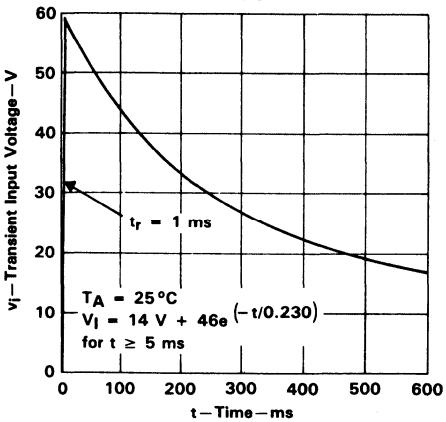


FIGURE 1

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

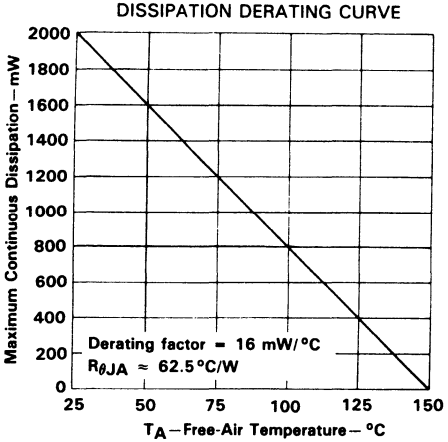


FIGURE 2

CASE TEMPERATURE
DISSIPATION DERATING CURVE

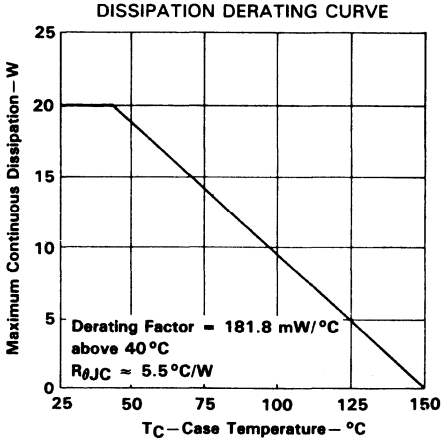
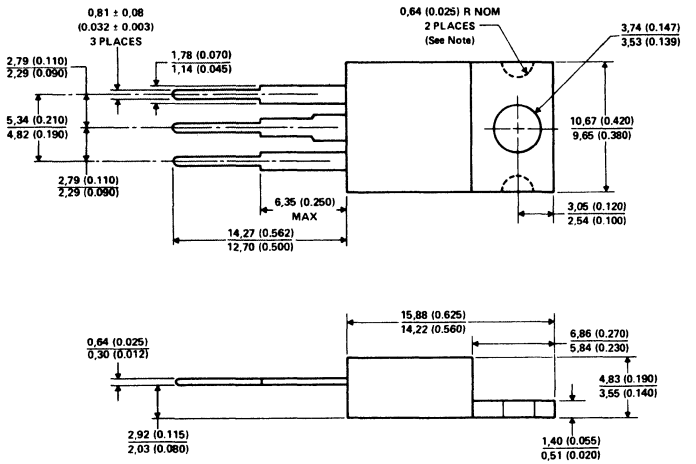


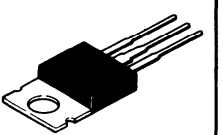
FIGURE 3

MECHANICAL DATA

3-LEAD KC (TO-220AB) PACKAGE

THE CENTER-TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING TAB
FALLS WITHIN JEDEC TO-220AB DIMENSIONS



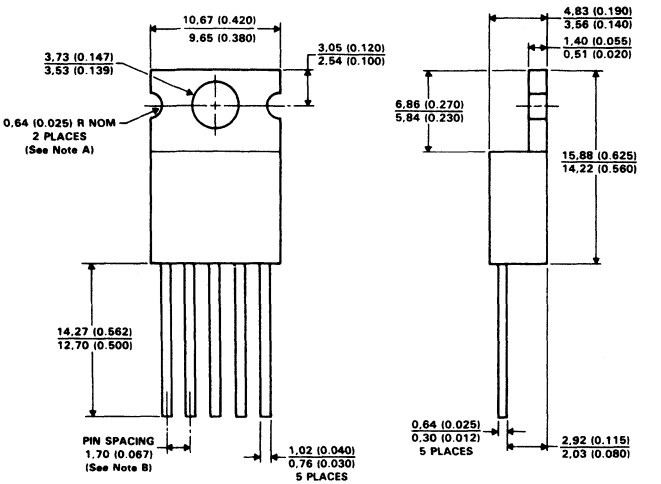


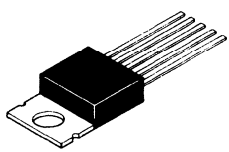
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE: Notches may or may not be present.

MECHANICAL DATA

5-LEAD KC PACKAGE





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

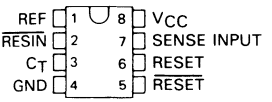
NOTES: A. Notches may or may not be present.
B. Leads are within 0,13 (0.005) radius of true position (T.P.) maximum material conditions.

TYPES TL7702A, TL7705A, TL7709A, TL7712A, TL7715A SUPPLY VOLTAGE SUPERVISORS

D2722, APRIL 1983 – REVISED FEBRUARY 1984

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- Wide Supply Voltage Range . . . 3 V to 18 V
- Precision Voltage Sensor
- Temperature-Compensated Voltage Reference
- True and Complement Reset Outputs
- Externally Adjustable Pulse Width

D OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TL7702A series are monolithic integrated circuit supply voltage supervisors specifically designed for use as reset controllers in microcomputer and microprocessor systems. During power-up the device tests the supply voltage and keeps the RESET and $\overline{\text{RESET}}$ outputs active (high and low, respectively) as long as the supply voltage has not reached its nominal voltage value. Taking $\overline{\text{RESIN}}$ low has the same effect. To ensure that the microcomputer system has reset, the TL7702A then initiates an internal time delay that delays the return of the reset outputs to their inactive states. Since the time delay for most microcomputers and microprocessors is in the order of several machine cycles, the device internal time delay is determined by an external capacitor connected to the C_T input (pin 3).

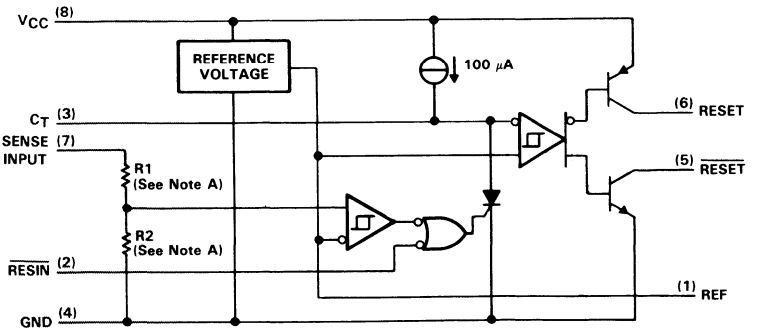
$$t_d = 1.3 \times 10^4 \times C_T$$

Where: C_T is in farads (F) and t_d is in seconds(s)

In addition, when the supply voltage drops below the nominal value, the outputs will be active until the supply voltage returns to the nominal value. An external capacitor (typically 0.1 μF) must be connected to the REF output (pin 1) to reduce the influence of fast transients in the supply voltage.

The TL7702AI series is characterized for operation from –40°C to 85°C; the TL7702AC series is characterized from 0°C to 70°C.

functional block diagram



NOTE A: TL7702A: R1 = 0 Ω, R2 = open
TL7705A: R1 = 7.8 kΩ, R2 = 10 kΩ
TL7709A: R1 = 19.7 kΩ, R2 = 10 kΩ
TL7712A: R1 = 32.7 kΩ, R2 = 10 kΩ
TL7715A: R1 = 43.4 kΩ, R2 = 10 kΩ

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 20 V
Input voltage range at $\overline{RESIN}$ . . . . . −0.3 V to 20 V
Input voltage at SENSE:
TL7702A (see Note 2) . . . . . −0.3 V to 6 V
TL7705A . . . . . −0.3 V to 10 V
TL7709A . . . . . −0.3 V to 15 V
TL7712A . . . . . −0.3 V to 20 V
TL7715A . . . . . −0.3 V to 20 V
High-level output current at $\overline{RESET}$ . . . . . −30 mA
Low-level output current at $\overline{RESET}$ . . . . . 30 mA
Operating free-air temperature range:
TL77 − AI . . . . . −40° to 85°C
TL77 − AC . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For the TL7702A, the voltage applied to the SENSE terminal must never exceed V_{CC}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3.6		18	V
High-level input voltage at $\overline{RESIN}$, V_{IH}		2			V
Low-level input voltage at $\overline{RESIN}$, V_{IL}				0.6	V
Voltage at sense input, V_I:	TL7702A	0		See Note 3	V
	TL7705A	0		10	
	TL7709A	0		15	
	TL7712A	0		20	
	TL7715A	0		20	
High-level output current at RESET, I_{OH}				−16	mA
Low-level output current at $\overline{RESET}$, I_{OL}				16	mA
Operating free-air temperature range, T_A:	TL77−AI	−40		85	°C
	TL77−AC	0		70	

NOTE 3: For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_{CC} − 1 V or 6 V, whichever is less.

electrical characteristics over recommended ranges of supply voltage, input voltage, output current, and free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage at $\overline{RESET}$		I_{OH} = −16 mA	V_{CC} − 1.5			V
V_{OL}	Low-level output voltage at $\overline{RESET}$		I_{OL} = 16 mA			0.4	V
V_{ref}	Reference voltage		T_A = 25°C	2.48	2.53	2.58	V
V_T	Threshold voltage at SENSE input	TL7702A	V_{CC} = 3.6 V to 18 V, T_A = 25°C	2.48	2.53	2.58	V
		TL7705A		4.5	4.55	4.6	
		TL7709A		7.5	7.6	7.7	
		TL7712A		10.6	10.8	11	
		TL7715A		13.2	13.5	13.8	
V_T	Threshold voltage at SENSE input	TL7702A	V_{CC} = 3.6 V to 18 V	2.45	2.53	2.58	V
		TL7705A		4.45	4.55	4.6	V
		TL7709A		7.4	7.6	7.7	V
		TL7712A		10.4	10.8	11.0	V
		TL7715A		13.0	13.5	13.8	V
$V_{T+} - V_{T-}$	Hysteresis‡ at SENSE input	TL7702A	V_{CC} = 3.6 V to 18 V, T_A = 25°C		10		mV
		TL7705A			15		
		TL7709A			20		
		TL7712A			35		
		TL7715A			45		
I_I	Input current at $\overline{RESIN}$ input		V_I = 2.4 V to V_{CC}			20	μA
			V_I = 0.4 V			−100	
I_I	Input current at SENSE input	TL7702A	$V_{ref} < V_I < V_{CC}$ − 1.5 V		0.5	2	μA
I_{OH}	High-level output current at $\overline{RESET}$		V_O = 18.V			50	μA
I_{OL}	Low-level output current at $\overline{RESET}$		V_O = 0			−50	μA
I_{CC}	Supply current		All inputs and outputs open		1.8	3	mA

†All characteristics are measured with C = 0.1 μF from Pin 1 to GND, and with C = 0.1 μF from Pin 3 to GND.
‡Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

Parameter		Test conditions	min	typ	max	Unit
t_{pi}	Pulse width at SENSE input	$V_{ih} = V_{styp} + 0.04 \times V_s$ $V_{il} = V_{styp} - 0.04 \times V_s$	.9			μs
t_{pi}	Pulse width at $\overline{RESIN}$ input		.4			μs
t_{po}	Pulse width at output	Ct = .1 μF	.65	1.3	2.6	ms
t_{pdHL}	Propagation delay time from $\overline{RESIN}$ to $\overline{RESET}$	C_L = 100pF; V_{CC} = 5V R_L = 4.7 kOhm			1	μs
$t_{r/f}$	Risetime for $\overline{RESET}$ Falltime for $\overline{RESET}$	C_L = 100pF; V_{CC} = 5V R_L = 4.7 kOhm			1	μs

TYPICAL APPLICATION DATA

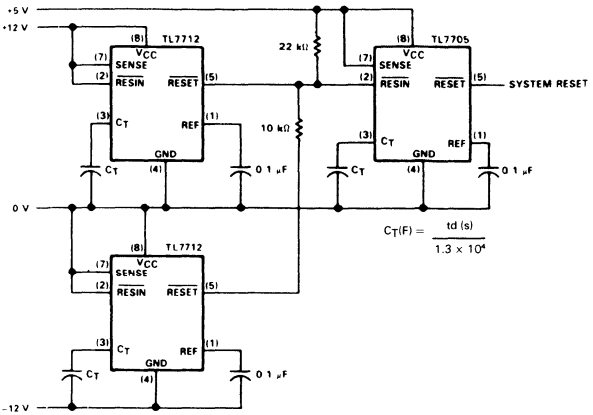


FIGURE 3 – MULTIPLE POWER SUPPLY SYSTEM RESET GENERATION

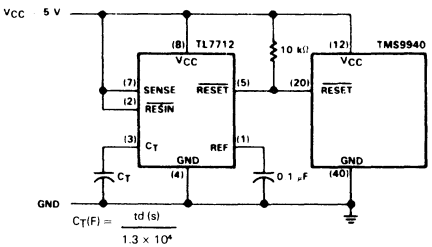


FIGURE 4 – RESET CONTROLLER FOR TMS9940 SYSTEM

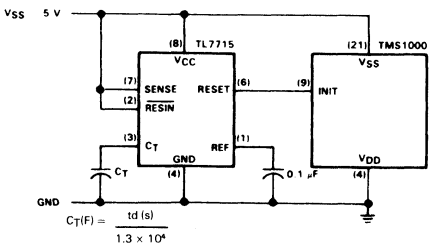
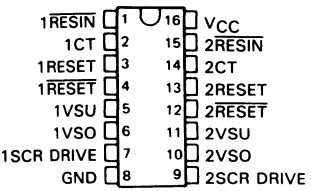


FIGURE 5 – RESET CONTROLLER FOR TMS1000

D3035, OCTOBER 1987—REVISED MAY 1988

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **$\overline{\text{RESET}}$ Defined When V_{CC} Exceeds 1 V**
- **\Wide Supply Voltage Range . . . 3.5 V to 18 V**
- **Precision Overvoltage and Undervoltage Sensing**
- **250-mA Peak Output Current for Driving SCR Gates**
- **2-mA Active-Low SCR Gate Drive for False Trigger Protection**
- **Temperature-Compensated Voltage Reference**
- **True and Complementary Reset Outputs**
- **Externally Adjustable Output Pulse Duration**

DW OR N PACKAGE
(TOP VIEW)



description

The TL7770 is a monolithic integrated circuit system supervisor designed for use as a reset controller in microcomputer and microprocessor power supply systems. This device contains two independent supply-voltage supervisors that monitor the supplies for overvoltage and undervoltage conditions at the VSO and VSU pins, respectively. When V_{CC} attains the minimum voltage of 1 V during power-up, the $\overline{\text{RESET}}$ output becomes active (low). As V_{CC} approaches 3.5 V, the delay timer function activates latching RESET and $\overline{\text{RESET}}$ active (high and low respectively) for a time delay, t_d, after system voltages have achieved normal levels. Above V_{CC} = 3.5 V, taking $\overline{\text{RESIN}}$ low will activate the time delay function, RESET and $\overline{\text{RESET}}$, during normal system voltage levels. To ensure that the microcomputer system has reset, the outputs remain active until the voltage at VSU exceeds the threshold value V_{T+} for a time delay, t_d, which is determined by an external timing capacitor such that:

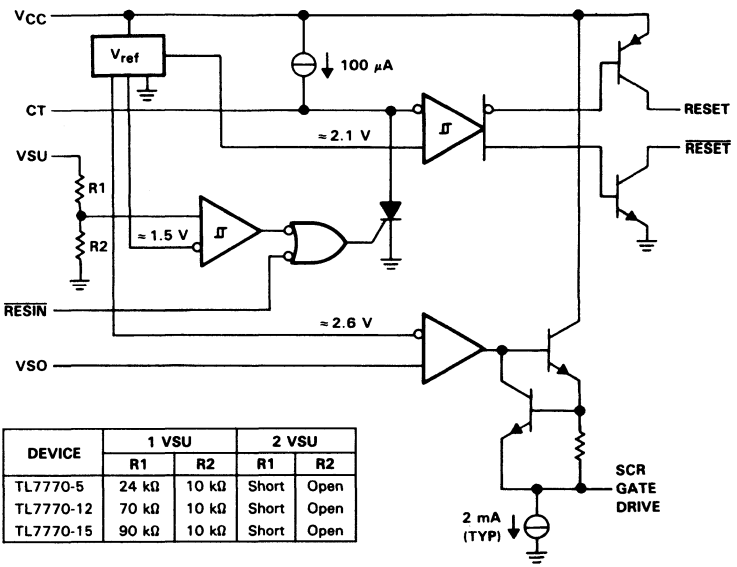
$$t_d \approx 20 \times 10^3 \times \text{capacitance}$$

where t_d is in seconds and capacitance is in farads.

The overvoltage-detection circuit is programmable for a wide range of user designs. During an overvoltage condition, an internal SCR is triggered, providing 250 mA peak instantaneous current and 25 mA continuous current to the SCR gate drive pin, which can be used to drive an external high-current SCR gate or an overvoltage warning circuit.

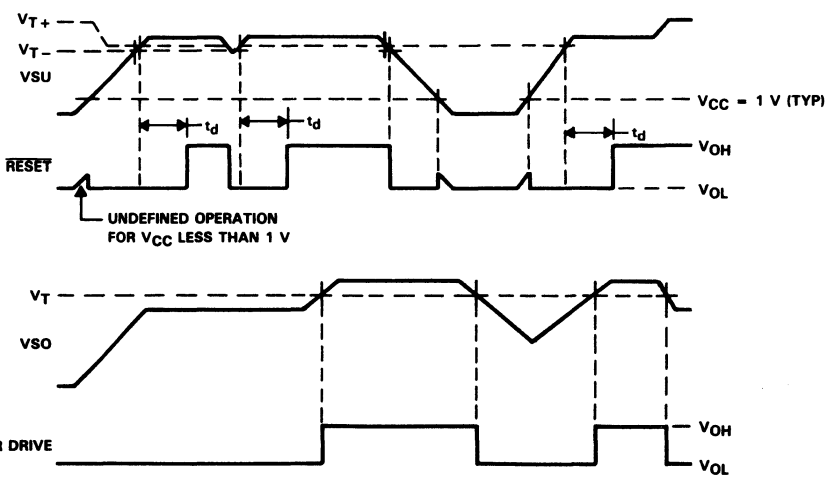
The TL7770Q series is characterized for operation from −40°C to 125°C. The TL7770C series is characterized for operation from 0°C to 70°C.

logic diagram (each channel)



DEVICE	1 VSU		2 VSU	
	R1	R2	R1	R2
TL7770-5	24 kΩ	10 kΩ	Short	Open
TL7770-12	70 kΩ	10 kΩ	Short	Open
TL7770-15	90 kΩ	10 kΩ	Short	Open

typical timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 20 V
Input voltage range, V_I: 1VSU, 2VSU, 1VSO, and 2VSO . . . . . −0.3 V to 18 V
Low-level output current (1$\overline{\text{RESET}}$ and 2$\overline{\text{RESET}}$), I_{OL} . . . . . 20 mA
High-level output current (1RESET and 2RESET), I_{OH} . . . . . −20 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range (see Note 2) . . . . . −40°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1000 mW	8.2 mW/°C	25°C	656 mW	205 mW
N	1000 mW	12.4 mW/°C	69°C	992 mW	310 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.5	18	V
Input voltage range, V_I (see Note 2)	1$\overline{\text{RESIN}}$, 2$\overline{\text{RESIN}}$, 1VSU, 2VSU, 2VSO, 1VSO	0	18	V
Output voltage (1CT and 2CT), V_O			5	V
Output sink current (1CT and 2CT), I_O			50	μA
High-level output current (1RESET and 2RESET), I_{OH}			−16	mA
Low-level output current (1$\overline{\text{RESET}}$ and 2$\overline{\text{RESET}}$), I_{OL}			16	mA
Continuous output current (1SCR GATE DRIVE and 2SCR GATE DRIVE), I_O			25	mA
Operating free-air temperature, T_A	TL7770Q Series	−40	125	°C
	TL7770C Series	0	70	

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

electrical characteristics over recommended ranges of supply voltage, input voltage, output current, and free-air temperature (unless otherwise noted)

supply supervisor section

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{OH} High-level output voltage	RESET	I_{OH} = −15 mA	V_{CC}−1.5			V
	SCR GATE DRIVE	I_{OH} = −20 mA	V_{CC}−1.5			
V_{OL} Low-level output voltage	$\overline{\text{RESET}}$	I_{OL} = 15 mA			0.4	V
V_{T-} Undervoltage threshold (negative-going)	TL7770-5 (5-V sense, 1VSU)	T_A = 25°C	4.5	4.55	4.6	V
	TL7770-12 (12-V sense, 1VSU)		10.8	10.9	11.02	
	TL7770-15 (15-V sense, 1VSU)		13.5	13.64	13.77	
	TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)		1.485	1.5	1.515	
	TL7770-5 (5-V sense, 1VSU)		4.46		4.64	
	TL7770-12 (12-V sense, 1VSU)		10.68		11.12	
	TL7770-15 (15-V sense, 1VSU)		13.36		13.91	
	TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)		1.47		1.53	
V_T Overvoltage threshold	TL7770-5, TL7770-12, TL7770-15 (VSO)	T_A = 25°C	2.53	2.58	2.63	V
		T_A = MIN to MAX	2.48		2.68	
V_{hys} Hysteresis ($V_{T+} - V_{T-}$) at VSU	TL7770-5 (5-V sense, 1VSU)	T_A = 25°C		15		mV
	TL7770-12 (12-V sense, 1VSU)			36		
	TL7770-15 (15-V sense, 1VSU)			45		
	TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)			5		
I_I Input current	$\overline{\text{RESIN}}$	V_I = 5.5 V or 0.4 V			−10	μA
	VSO	V_I = 2.4 V		0.5	2	
I_{OH} High-level output current	$\overline{\text{RESET}}$	V_O = 18 V			50	μA
I_{OL} Low-level output current	RESET	V_O = 0			−50	μA
I_{OH} Peak output current	SCR GATE DRIVE	Duration = 1 ms	250			mA

total device

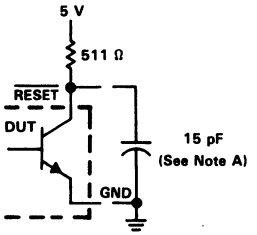
PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
I_{CC} Supply current	1VSU and 2VSU at > V_{T+}, 1$\overline{\text{RESIN}}$ and 2$\overline{\text{RESIN}}$ at V_{CC},	T_A = 25°C			5	mA
	1VSO and 2VSO at 0 V	T_A = MIN to MAX			6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified in the recommended operating conditions.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

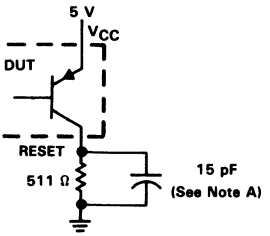
switching characteristics, V_{CC} = 5 V, CT open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{RESIN}$	RESET	See Figure 1		270	500	ns
t_{PHL}	Propagation delay time, high-to-low-level output	$\overline{RESIN}$	RESET			270	500	ns
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{RESIN}$	$\overline{RESET}$			270	500	ns
t_{PHL}	Propagation delay time, high-to-low-level output	$\overline{RESIN}$	$\overline{RESET}$			270	500	ns
t_r	Rise time		RESET				75	ns
t_f	Fall time					150		
t_r	Rise time		$\overline{RESET}$			75		ns
t_f	Fall time						50	
$t_{w(min)}$	Minimum effective pulse duration	$\overline{RESIN}$		See Figure 2(a)		150		ns
		VSU		See Figure 2(b)		100		

PARAMETER MEASUREMENT INFORMATION



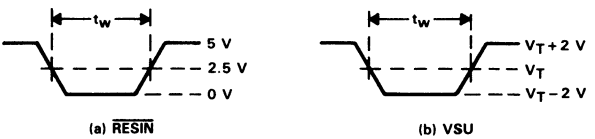
$\overline{\text{RESET}}$ OUTPUT CONFIGURATION



RESET OUTPUT CONFIGURATION

NOTE A: Includes jig and probe capacitance.

FIGURE 1. RESET AND $\overline{\text{RESET}}$ OUTPUT CONFIGURATIONS



WAVEFORMS

FIGURE 2. INPUT PULSE DEFINITION

SERIES TL780
POSITIVE VOLTAGE REGULATORS

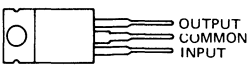
D2643, APRIL 1981

- ±1% Output tolerance at 25°C
- ±2% Output Tolerance Over Full Operating Range
- Thermal Shutdown
- Internal Short-Circuit Current Limiting
- Pinout Identical to uA7800 Series
- Improved Version of uA7800 Series

NOMINAL OUTPUT VOLTAGE	REGULATOR
5 V	TL780-05C
12 V	TL780-12C
15 V	TL780-15C

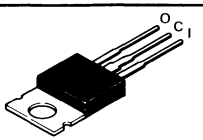
KC PACKAGE

(TOP VIEW)



THE COMMON TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

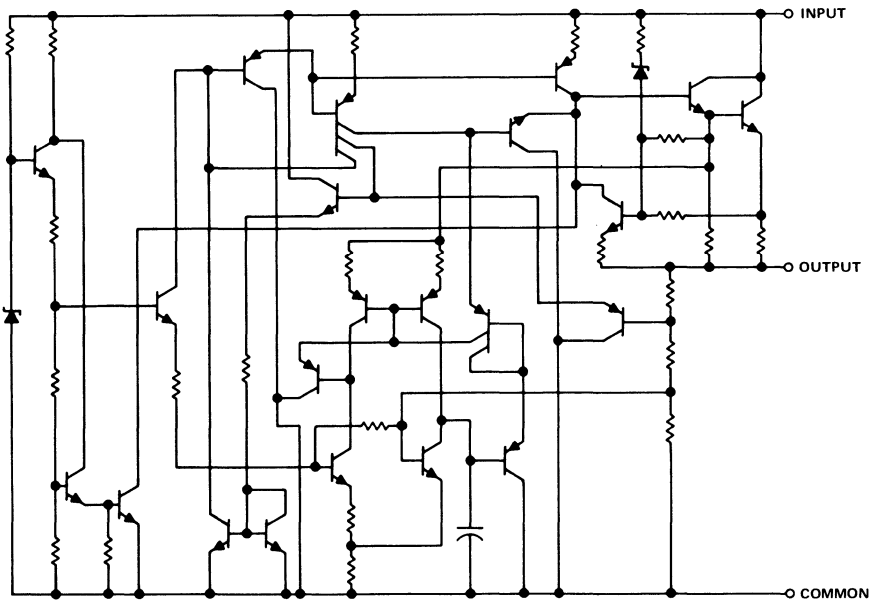
TO-220AB



description

Each fixed-voltage precision regulator in this series is capable of supplying 1.5 amperes of load current. A unique temperature-compensation technique coupled with an internally trimmed bandgap reference has resulted in improved accuracy when compared to other three-terminal regulators. Advanced layout techniques provide excellent line, load, and thermal regulation. The internal current limiting and thermal shutdown features make the devices essentially immune to overload.

schematic



absolute maximum ratings over operating temperature range (unless otherwise noted)

Input voltage	35 V
Continuous total dissipation at 25°C free-air temperature (see Note 1)	2 W
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)	15 W
Operating free-air, case, or virtual junction temperature range	0 to 150°C
Storage temperature range	−65 to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

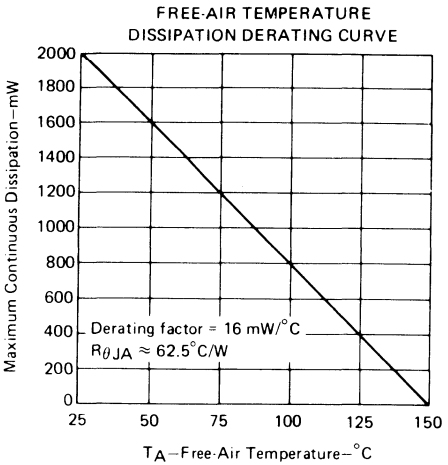


FIGURE 1

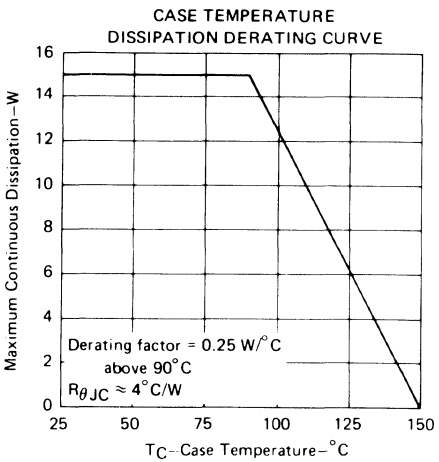


FIGURE 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	TL780-05C	7	25	V
	TL780-12C	14.5	30	
	TL780-15C	17.5	30	
Output current, I_O			1.5	A
Operating virtual junction temperature, T_J		0	125	°C

TL780-05C electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	I_O = 5 mA to 1 A, P ≤ 15 W V_I = 7 V to 20 V	25°C	4.95	5	5.05	V
		0°C to 125°C	4.9		5.1	
Input regulation	V_I = 7 V to 25 V	25°C		0.5	5	mV
	V_I = 8 V to 12 V			0.5	5	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	0°C to 125°C	70	85		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		4	25	mV
	I_O = 250 mA to 750 mA			1.5	15	
Output resistance	f = 1 kHz	0°C to 125°C		0.0035		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		0.25		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		75		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		5	8	mA
Bias current change	V_I = 7 V to 25 V	0°C to 125°C		0.7	1.3	mA
	I_O = 5 mA to 1 A			0.03	0.5	
Short-circuit output current	V_I = 35 V	25°C		750		mA
Peak output current		25°C		2.2		A

TL780-12C electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	I_O = 5 mA to 1 A, P ≤ 15 W V_I = 14.5 V to 27 V	25°C	11.88	12	12.12	V
		0°C to 125°C	11.76		12.24	
Input regulation	V_I = 14.5 V to 30 V	25°C		1.2	12	mV
	V_I = 16 V to 22 V			1.2	12	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	0°C to 125°C	65	80		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		6.5	60	mV
	I_O = 250 mA to 750 mA			2.5	36	
Output resistance	f = 1 kHz	0°C to 125°C		0.0035		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		0.6		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		180		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		5.5	8	mA
Bias current change	V_I = 14.5 V to 30 V	0°C to 125°C		0.4	1.3	mA
	I_O = 5 mA to 1 A			0.03	0.5	
Short-circuit output current	V_I = 35 V	25°C		350		mA
Peak output current		25°C		2.2		A

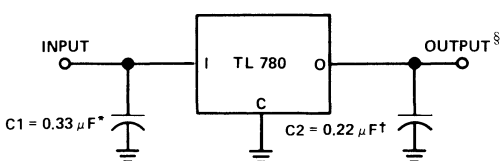
† All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.22 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycles ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

TL780-15C electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	I_O = 5 mA to 1 A, P ≤ 15 W	25°C	14.85	15	15.15	V
	V_I = 17.5 V to 30 V	0°C to 125°C	14.7		15.3	
Input regulation	V_I = 17.5 V to 30 V	25°C		1.5	15	mV
	V_I = 20 V to 26 V			1.5	15	
Ripple rejection	V_I = 18.5 V to 28.5 V f = 120 Hz	0°C to 125°C	60	75		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		7	75	mV
	I_O = 250 mA to 750 mA			2.5	45	
Output resistance	f = 1 kHz	0°C to 125°C		0.0035		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		0.62		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		225		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		5.5	8	mA
Bias current change	V_I = 17.5 V to 30 V	0°C to 125°C		0.4	1.3	mA
	I_O = 5 mA to 1 A			0.02	0.5	
Short-circuit output current	V_I = 35 V	25°C		230		mA
Peak output current		25°C		2.2		A

† All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.22 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

TYPICAL APPLICATION DATA



*C1 required if regulator is far from power supply filter.
†C2 not required for stability, however transient response is improved
§ Permanent damage can occur if output is pulled below ground.

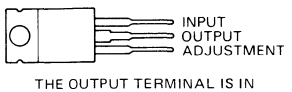
TYPE TL783C
HIGH-VOLTAGE ADJUSTABLE REGULATOR

D2659, SEPTEMBER 1981 – REVISED JANUARY 1983

- Output Adjustable From 1.25 V To 125-Volt
- 700 mA Output Current
- Full Short-Circuit, Safe-Operating-Area, and Thermal Shutdown Protection
- 0.001 %/V Typical Input Regulation
- 0.15% Typical Output Regulation
- 76 dB Typical Ripple Rejection
- Standard TO-220AB Package

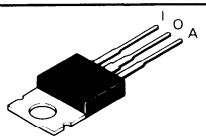
KC PACKAGE

(TOP VIEW)



THE OUTPUT TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

TO-220AB



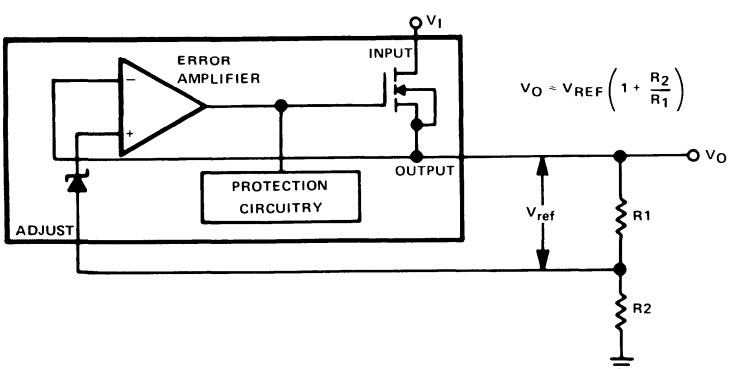
description

The TL783 is an adjustable 3-terminal positive-voltage regulator with an output range of 1.25 volts to 125 volts and a DMOS output transistor capable of sourcing more than 700 milliamperes. It is designed for use in high-voltage applications where standard bipolar regulators cannot be used. Excellent performance specifications . . . superior to those of most bipolar regulators . . . are achieved through circuit design and advanced layout techniques.

As a state-of-the-art regulator, the TL783 combines standard bipolar circuitry with high-voltage double-diffused MOS transistors on one chip to yield a device capable of withstanding voltages far higher than standard bipolar integrated circuits. Because of its lack of secondary breakdown and thermal runaway characteristics usually associated with bipolar outputs, the TL783 maintains full overload protection while operating at up to 125 volts from input to output. Other features of the device include current limiting, safe-operating-area (SOA) protection, and thermal shutdown. Even if the adjustment pin is inadvertently disconnected, the protection circuitry remains functional.

Only two external resistors are required to program the output voltage. An input bypass capacitor is necessary only when the regulator is situated far from the input filter. An output capacitor, although not required, will improve transient response and protection from instantaneous output short-circuits. Excellent ripple rejection can be achieved without a bypass capacitor at the adjustment terminal.

functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)

Input-to-output differential voltage, $V_I - V_O$	125 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1)	2 W
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)	20 W
Operating free-air, case, or virtual junction temperature range	0°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds	260°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual dvice electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

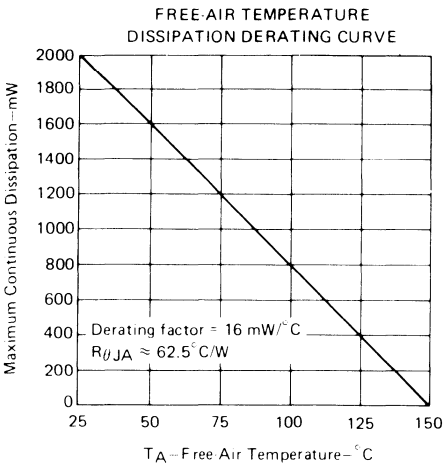


FIGURE 1

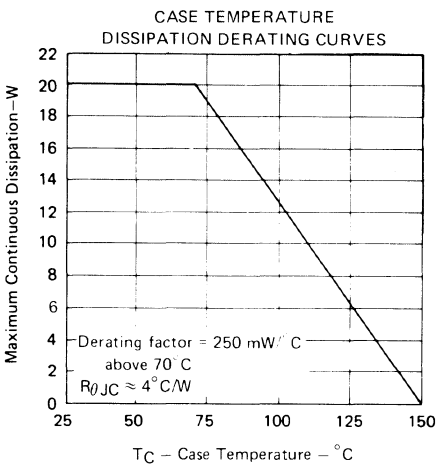


FIGURE 2

recommended operating conditions

	MIN	MAX	UNIT
Input-to-output voltage differential, $V_I - V_O$		125	V
Output current, I_O	15	700	mA
Operating virtual junction temperature, T_J	0	125	°C

electrical characteristics at $V_I - V_O = 25$ V, $I_O = 0.5$ A, $T_J = 0°C$ to $125°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
Input regulation‡	$V_I - V_O = 20$ V to 125 V		$T_J = 25°C$		0.001	0.01	%/V
			$T_J = 0°C$ to $125°C$		0.004	0.02	
Ripple rejection	$\Delta V_{I(p-p)} = 10$ V,	$V_O = 10$ V,	f = 120 Hz	66	76		dB
Output regulation	$I_O = 15$ mA to 700 mA,	$T_J = 25°C$	$V_O \leq 5$ V		7.5	25	mV
			$V_O \geq 5$ V		0.15	0.5	%
	$I_O = 15$ mA to 700 mA		$V_O \leq 5$ V		20	70	mV
			$V_O \geq 5$ V		0.3	1.5	%
Output voltage change with temperature					0.4		%
Output voltage long-term drift	1000 h at $T_J = 125°C$, See Note 2	$V_I - V_O = 125$ V,			0.2		%
Output noise voltage	f = 10 Hz to 10 kHz,	$T_J = 25°C$			0.003		%
Minimum output current to maintain regulation	$V_I - V_O = 125$ V					15	mA
Peak output current	$V_I - V_O = 25$ V,	t = 1 ms			1100		mA
	$V_I - V_O = 15$ V,	t = 30 ms			715		
	$V_I - V_O = 25$ V,	t = 30 ms		700	900		
	$V_I - V_O = 125$ V,	t = 30 ms		100	250		
Adjustment-terminal current					83	110	μA
Change in adjustment-terminal current	$V_I - V_O = 15$ V to 125 V,	$I_O = 15$ mA to 700 mA,	P ≤ rated dissipation		0.5	5	μA
Reference voltage (output to ADJ)	$V_I - V_O = 10$ V to 125 V,	$I_O = 15$ mA to 700 mA,	P ≤ rated dissipation	1.2	1.27	1.3	V

† All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%) to limit changes in average internal dissipation. Output voltage changes due to large changes in internal dissipation must be taken into account separately.

‡ Input regulation is expressed here as the percentage change in output voltage per 1-volt change at the input.

NOTE 2: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

TYPICAL CHARACTERISTICS

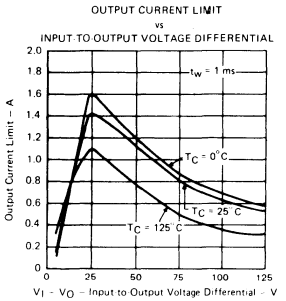


FIGURE 3

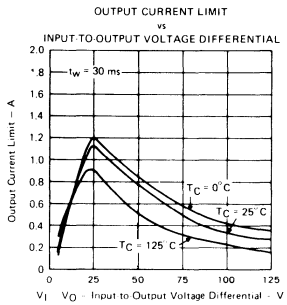


FIGURE 4

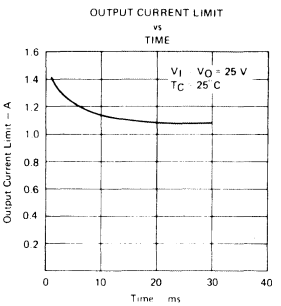


FIGURE 5

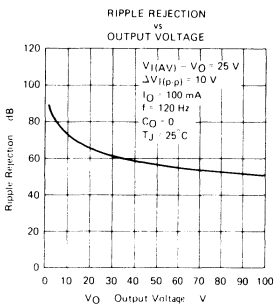


FIGURE 6

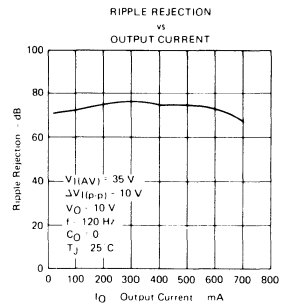


FIGURE 7

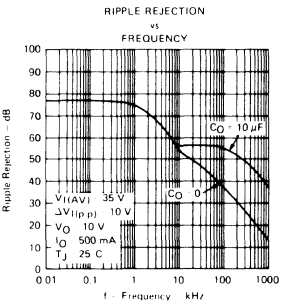


FIGURE 8

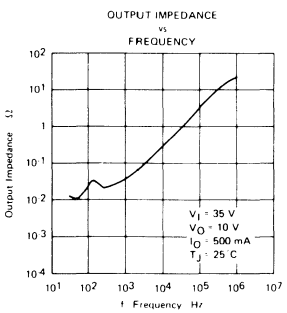


FIGURE 9

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

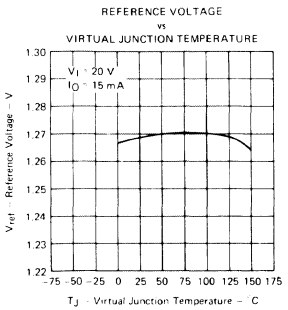


FIGURE 10

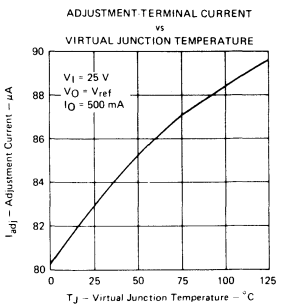


FIGURE 11

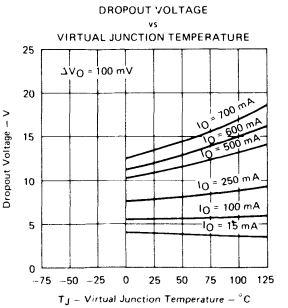


FIGURE 12

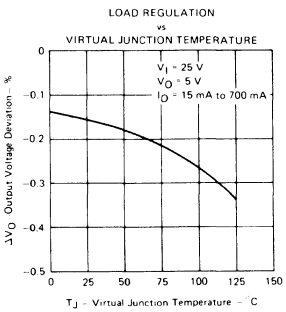


FIGURE 13

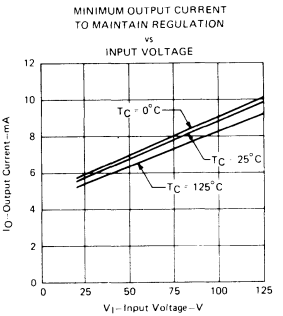


FIGURE 14

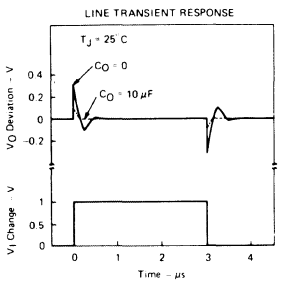


FIGURE 15

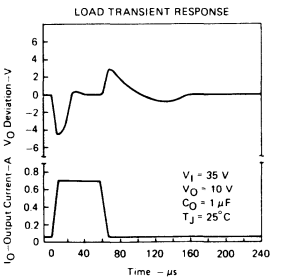


FIGURE 16

DESIGN CONSIDERATIONS

The internal reference (see functional block diagram) is used to generate 1.25 volts nominal (V_{ref}) between the output and adjustment terminals. This voltage is developed across R1 and causes a constant current to flow through R1 and the programming resistor R2, giving an output voltage of:

$$V_O = V_{ref} (1 + R2/R1) + I_{adj} (R2)$$

or

$$V_O \approx V_{ref} (1 + R2/R1).$$

The TL783 was designed to minimize I_{adj} and maintain consistency over line and load variations, thereby minimizing the I_{adj} (R2) error term.

To maintain I_{adj} at a low level, all quiescent operating current is returned to the output terminal. This quiescent current must be sunk by the external load and is the minimum load current necessary to prevent the output from rising. The recommended R1 value of 82 ohms will provide a minimum load current of 15 milliamperes. Larger values may be used if the input-to-output differential voltage is less than 125 volts (see minimum operating current curve) or if the load will sink some portion of the minimum current.

Bypass capacitors

The TL783 regulator is stable without bypass capacitors; however, any regulator will become unstable with certain values of output capacitance if an input capacitor is not used. Therefore, the use of input bypassing is recommended whenever the regulator is located more than four inches from the power-supply filter capacitor. A 1-microfarad tantalum or electrolytic capacitor is usually sufficient.

Adjustment-terminal capacitors are not recommended for use on the TL783 because they can seriously degrade load transient response as well as create a need for extra protection circuitry. Excellent ripple rejection is presently achieved without this added capacitor.

Due to the relatively low gain of the MOS output stage, output voltage drop-out may occur under large load transient conditions. Addition of an output bypass capacitor will greatly enhance load transient response as well as prevent drop-out. For most applications it is recommended that an output bypass capacitor be used with a minimum value of:

$$C_O (\mu f) = 15/V_O$$

Larger values will provide proportionally better transient response characteristics.

Protection circuitry

The TL783 regulator includes built-in protection circuitry capable of guarding the device against most overload conditions encountered in normal operation. These protective features are current limiting, safe-operating-area protection, and thermal shutdown. These circuits are meant to protect the device under occasional fault conditions only. Continuous operation in the current limit or thermal shutdown mode is not recommended.

The internal protection circuits of the TL783 will protect the device up to maximum rated V_I as long as certain precautions are taken. If V_I is instantaneously switched on, transients exceeding maximum input ratings may occur, which can destroy the regulator. These are usually caused by lead inductance and bypass capacitors causing a ringing voltage on the input. In addition, if rise times in excess of 10 V/ns are applied to the input, a parasitic n-p-n transistor in parallel with the DMOS output can be turned on causing the device to fail. If the device is operated over 50 volts and the input is switched on rather than ramped on, a low-Q capacitor, such as a tantalum or electrolytic should be used rather than ceramic, paper, or plastic bypass capacitors. A dissipation factor of 0.015 or greater will usually provide adequate damping to suppress ringing. Normally, no problems will occur if the input voltage is allowed to ramp upward through the action of an ac line rectifier and filter network.

Similarly, if an instantaneous short circuit is applied to the outputs, both ringing and excessive fall times can result. A tantalum or electrolytic bypass capacitor is recommended to eliminate this problem. However, if a large output capacitor is used and the input is shorted, addition of a protection diode may be necessary to prevent capacitor discharge through the regulator. The amount of discharge current delivered is dependent on output voltage, size of capacitor, and fall time of V_I. A protective diode (see Figure 17) is required only for capacitance values greater than

$$C_O\ (\mu f) = 3 \times 10^4/(V_O)^2.$$

Care should always be taken to prevent insertion of regulators into a socket with power on. Power should be turned off before removing or inserting regulators.

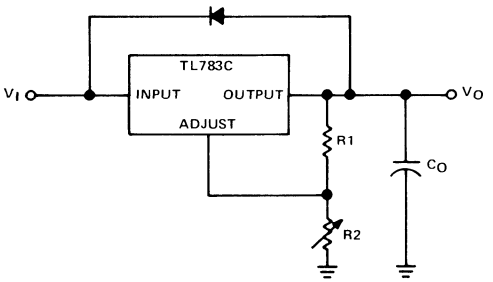


FIGURE 17– REGULATOR WITH PROTECTIVE DIODE

Load regulation

The current set resistor (R1) should be located close to the regulator output terminal rather than near the load. This eliminates long line drops from being amplified through the action of R1 and R2 to degrade load regulation. To provide remote ground sensing, R2 should be near the load ground.

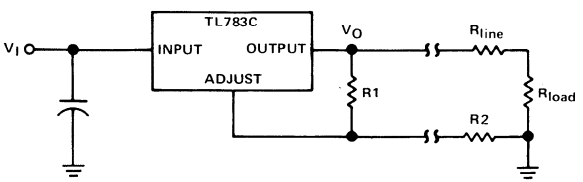
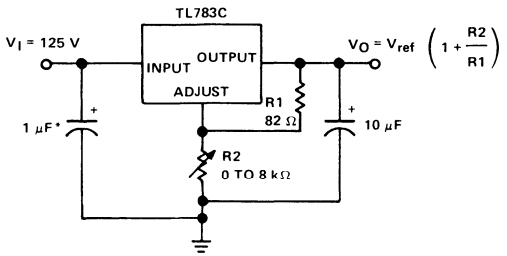


FIGURE 18–REGULATOR WITH CURRENT-SET RESISTOR

TYPICAL APPLICATION DATA



NEEDED IF DEVICE IS MORE THAN 4 INCHES FROM FILTER CAPACITOR

FIGURE 19–1.25-V TO 115-V ADJUSTABLE REGULATOR

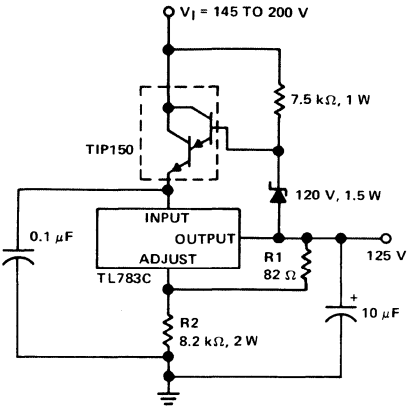


FIGURE 20–125 V SHORT-CIRCUIT-PROTECTED OFF-LINE REGULATOR

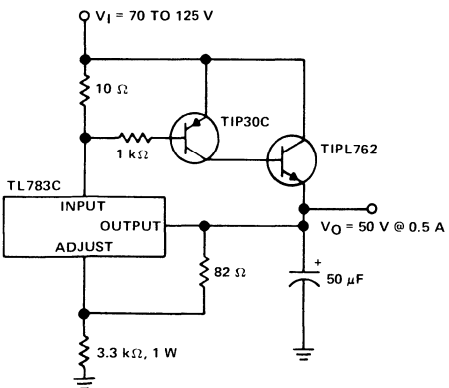


FIGURE 21–50-V REGULATOR WITH CURRENT BOOST

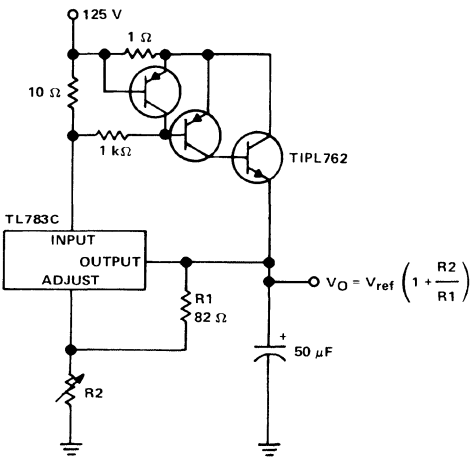


FIGURE 22–ADJUSTABLE REGULATOR WITH CURRENT BOOST AND CURRENT LIMIT

TYPICAL APPLICATION DATA

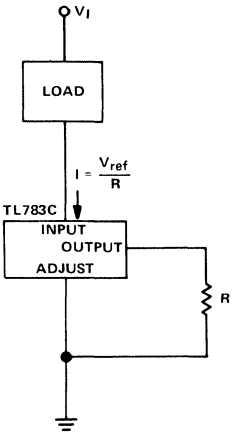


FIGURE 23–CURRENT-SINKING REGULATOR

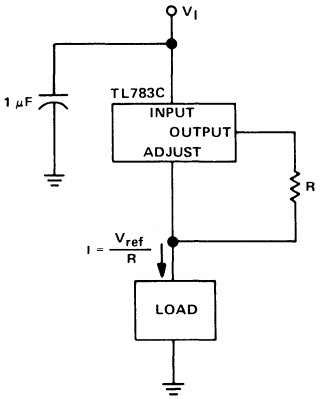


FIGURE 24–CURRENT-SOURCING REGULATOR

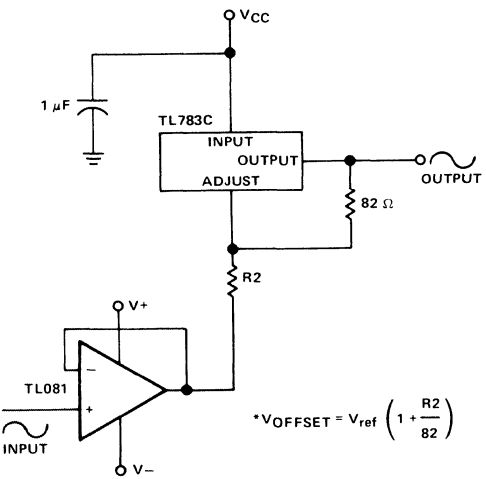


FIGURE 25–HIGH-VOLTAGE UNITY-GAIN OFFSET AMPLIFIER

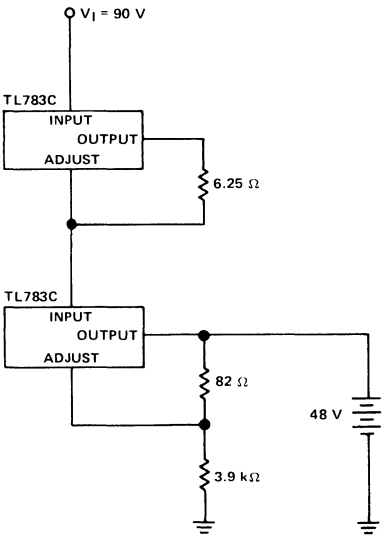


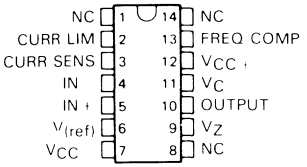
FIGURE 26–48-V, 200-mA FLOAT CHARGER

TYPES uA723M, uA723C
PRECISION VOLTAGE REGULATORS

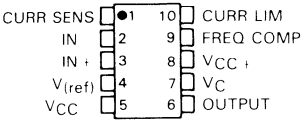
D1063, AUGUST 1972 REVISED DECEMBER 1982

- 150-mA Load Current Without External Power Transistor
- Typically 0.02% Input Regulation and 0.03% Load Regulation (uA723M)
- Adjustable Current Limiting Capability
- Input Voltages to 40 Volts
- Output Adjustable from 2 to 37 Volts
- Direct Replacement for Fairchild μA723M and μA723C

uA723M . . . J PACKAGE
uA723C . . . D, J, OR N PACKAGE
(TOP VIEW)



uA723M . . . U PACKAGE
(TOP VIEW)



NC No internal connection

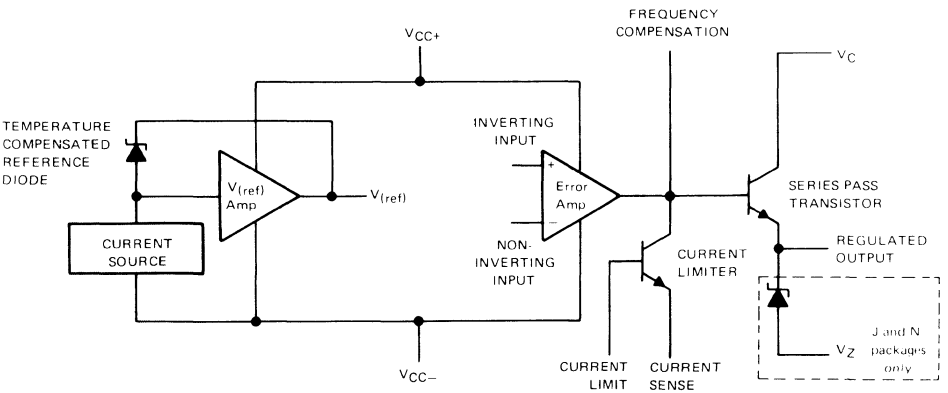
description

The uA723M and uA723C are monolithic integrated circuit voltage regulators featuring high ripple rejection, excellent input and load regulation, excellent temperature stability, and low standby current. The circuit consists of a temperature-compensated reference voltage amplifier, an error amplifier, a 150-milliampere output transistor, and an adjustable output current limiter.

The uA723M and uA723C are designed for use in positive or negative power supplies as a series, shunt, switching, or floating regulator. For output currents exceeding 150 mA, additional pass elements may be connected as shown in Figure 4 and 5.

The uA723M is characterized for operation over the full military temperature range of −55°C to 125°C. The uA723C is characterized for operation from 0°C to 70°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Peak voltage from V_{CC+} to V_{CC-} ($t_w \leq 50$ ms)	50 V
Continuous voltage from V_{CC+} to V_{CC-}	40 V
Input-to-output voltage differential	40 V
Differential input voltage to error amplifier	±5 V
Voltage between noninverting input and V_{CC-}	8 V
Current from V_Z	25 mA
Current from $V_{(ref)}$	15 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1):	
J or N package	1000 mW
U package	675 mW
Operating free-air temperature range: uA723M Circuits	−55°C to 125°C
uA723C Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, J or U package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, N package	260°C

NOTE 1: Power dissipation = $|I_{I(standby)} + I_{(ref)}|\,V_{CC} + |V_C - V_O|\,I_O$. For operation at elevated temperature, refer to Dissipation Derating Table. In the J package, uA723M chips are alloy-mounted; uA723C chips are glass-mounted.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	9.5	40	V
Output voltage, V_O	2	37	V
Input-to-output voltage differential, $V_C - V_O$	3	38	V
Output current, I_O		150	mA

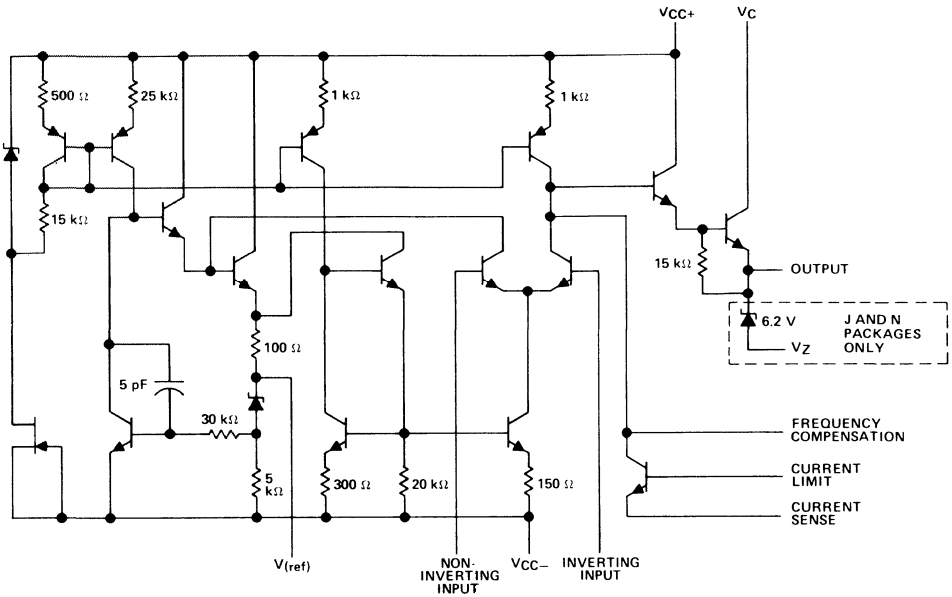
electrical characteristics at specified free-air temperature (see Note 2)

PARAMETER	TEST CONDITIONS†			uA723M			uA723C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Input regulation	V_I = 12 V to V_I = 15 V		25°C		0.01%	0.1%		0.01%	0.1%	
	V_I = 12 V to V_I = 40 V		25°C		0.02%	0.2%		0.1%	0.5%	
	V_I = 12 V to V_I = 15 V		Full range			0.3%			0.3%	
Ripple rejection	f = 50 Hz to 10 kHz,	$C_{(ref)}$ = 0	25°C		74			74		dB
	f = 50 Hz to 10 kHz,	$C_{(ref)}$ = 5 μF	25°C		86			86		
Output regulation	I_O = 1 mA to I_O = 50 mA		25°C		−0.03%	−0.15%		−0.03%	−0.2%	
			Full range			−0.6%			−0.6%	
Reference voltage, $V_{(ref)}$			25°C	6.95	7.15	7.35	6.8	7.15	7.5	V
Standby current	V_I = 30 V,	I_O = 0	25°C		2.3	3.5		2.3	4	mA
Temperature coefficient of output voltage			Full range		0.002	0.015		0.003	0.015	%/°C
Short-circuit output current	R_{SC} = 10 Ω,	V_O = 0	25°C		65			65		mA
Output noise voltage	BW = 100 Hz to 10 kHz,	$C_{(ref)}$ = 0	25°C		20			20		μV
	BW = 100 Hz to 10 kHz,	$C_{(ref)}$ = 5 μF	25°C		2.5			2.5		

†Full range for uA723M is −55°C to 125°C and for uA723C is 0°C to 70°C.

NOTE 2: For all values in this table the device is connected as shown in Figure 1 with the divider resistance as seen by the error amplifier ≤ 10 kΩ. Unless otherwise specified, $V_I = V_{CC+} = V_C$ = 12 V, V_{CC-} = 0, V_O = 5 V, I_O = 1 mA, R_{SC} = 0, and $C_{(ref)}$ = 0.

schematic



RESISTOR AND CAPACITOR VALUES SHOWN ARE NOMINAL.

DISSIPATION DERATING TABLE

POWER	POWER RATING	DERATING FACTOR	ABOVE T_A
J (Alloy-Mounted Chip)	1000 mW	11.0 mW/°C	59°C
J (Glass-Mounted Chip)	1000 mW	8.2 mW/°C	28°C
N	1000 mW	9.2 mW/°C	41°C
U	675 mW	5.4 mW/°C	25°C

TYPICAL APPLICATION DATA

TABLE I

RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGES

OUTPUT VOLTAGE (V)	APPLICABLE FIGURES (SEE NOTE 3)	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (SEE NOTE 4)			OUTPUT VOLTAGE (V)	APPLICABLE FIGURES (SEE NOTE 3)	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (SEE NOTE 4)		
		R1 (kΩ)	R2 (kΩ)	R1 (kΩ)	P1 (kΩ)	R2 (kΩ)			R1 (kΩ)	R2 (kΩ)	R1 (kΩ)	P1 (kΩ)	R2 (kΩ)
+3.0	1, 5, 6, 9, 11, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	105	2.2	10	91
+3.6	1, 5, 6, 9, 11, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 11, 12 (4)	2.15	4.99	0.75	0.5	2.2	−6 (Note 5)	3, (10)	3.57	2.43	1.2	0.5	0.75
+6.0	1, 5, 6, 9, 11, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 9, 12)	1.87	7.15	0.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.57	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	95.3	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II

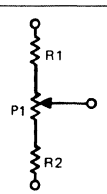
FORMULAS FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts [Figures 1, 5, 6, 9, 11, 12, (4)] $V_O = V_{(ref)} \times \frac{R2}{R1 + R2}$	Outputs from +4 to +250 volts [Figure 7] $V_O = \frac{V_{(ref)}}{2} \times \frac{R2 - R1}{R1}$; R3 = R4	Current Limiting $I_{(limit)} \approx \frac{0.65\ V}{R_{sc}}$
Outputs from +7 to +37 volts [Figures 2, 4, (5, 6, 9, 11, 12)] $V_O = V_{(ref)} \times \frac{R1 + R2}{R2}$	Outputs from −6 to −250 volts [Figures 3, 8, 10] $V_O = -\frac{V_{(ref)}}{2} \times \frac{R1 + R2}{R1}$; R3 = R4	Foldback Current Limiting [Figure 6] $I_{(knee)} \approx \frac{V_O R3 + (R3 + R4)\ 0.65\ V}{R_{sc} R4}$ $I_{OS} \approx \frac{0.65\ V}{R_{sc}} \times \frac{R3 + R4}{R4}$

NOTES: 3. The R1/R2 divider may be across either V_O or $V_{(ref)}$. If the divider is across $V_{(ref)}$ and uses figures without parentheses, use figures with parentheses when the divider is across V_O.

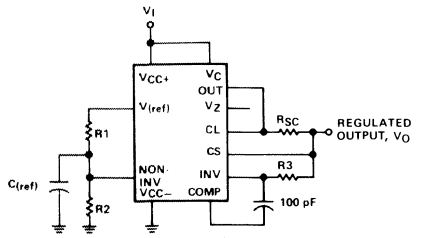
4. To make the voltage adjustable, the R1/R2 divider shown in the figures must be replaced by the divider shown at the right.

5. The device requires a minimum of 9 V between V_{CC+} and V_{CC-} when V_O is equal to or more positive than −9 V.



ADJUSTABLE OUTPUT CIRCUITS

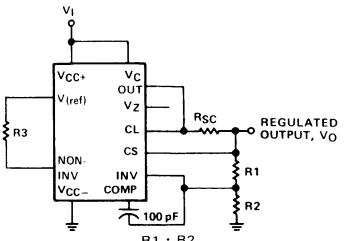
TYPICAL APPLICATION DATA



NOTES: A. $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum α_{VO}.

B. R3 may be eliminated for minimum component count. Use direct connection (i.e., $R_3 = 0$).

FIGURE 1–BASIC LOW-VOLTAGE REGULATOR
(V_O = 2 TO 7 VOLTS)



NOTES: A. $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum α_{VO}.

B. R3 may be eliminated for minimum component count. Use direct connection (i.e., $R_3 = 0$).

FIGURE 2–BASIC HIGH-VOLTAGE REGULATOR
(V_O = 7 TO 37 VOLTS)

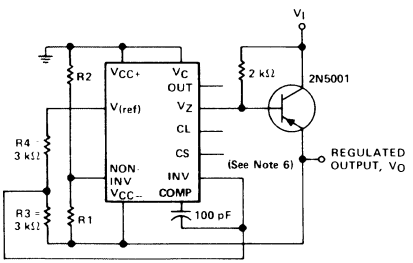


FIGURE 3–NEGATIVE-VOLTAGE REGULATOR

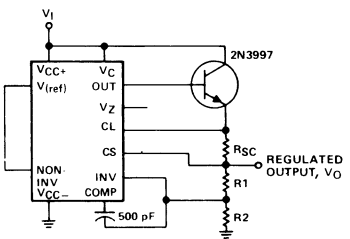


FIGURE 4–POSITIVE-VOLTAGE REGULATOR
(EXTERNAL N-P-N- PASS TRANSISTOR)

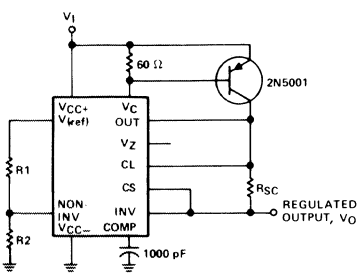


FIGURE 5–POSITIVE-VOLTAGE REGULATOR
(EXTERNAL P-N-P PASS TRANSISTOR)

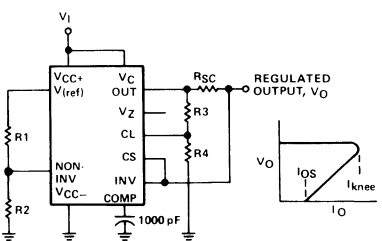


FIGURE 6–FOLDBACK CURRENT LIMITING

TYPICAL APPLICATION DATA

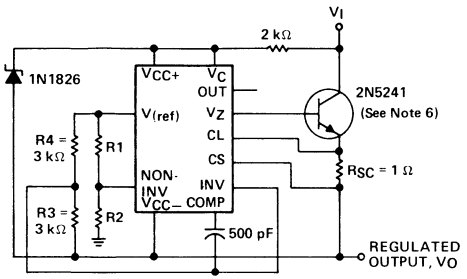


FIGURE 7–POSITIVE FLOATING REGULATOR

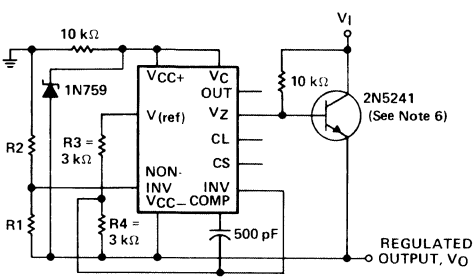


FIGURE 8–NEGATIVE FLOATING REGULATOR

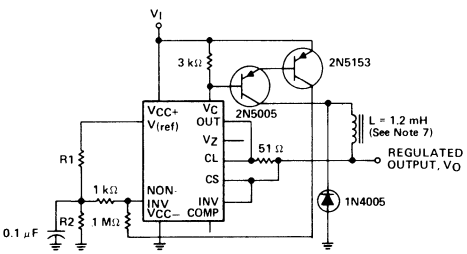


FIGURE 9–POSITIVE SWITCHING REGULATOR

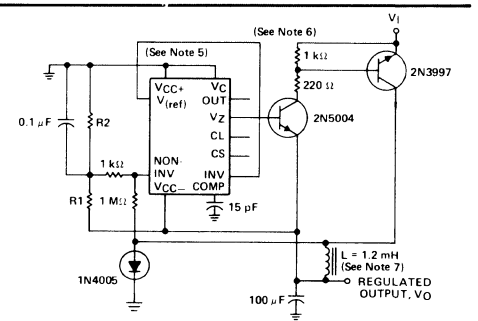
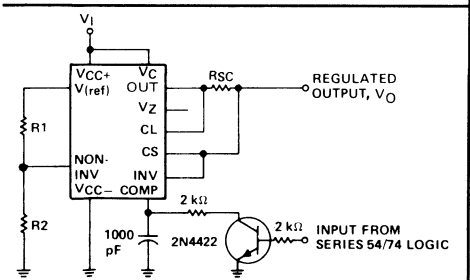


FIGURE 10–NEGATIVE SWITCHING REGULATOR



NOTE A: Current limit transistor may be used for shutdown if current limiting is not required.

FIGURE 11–REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING

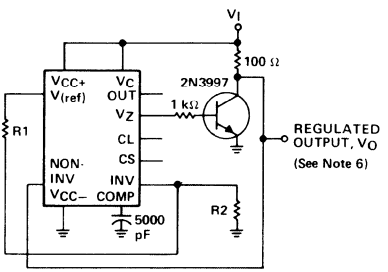


FIGURE 12–SHUNT REGULATOR

NOTES: 5. The device requires a minimum of 9 V between V_{CC+} and V_{CC-} when V_O is equal to or more positive than −9 V.
6. When 10-lead uA723 devices are used in applications requiring V_Z, an external 6.2-V regulator diode must be connected in series with the V_O terminal.
7. L is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 potted core, or equivalent, with 0.009-inch air gap.

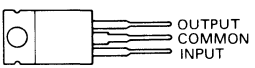
SERIES uA7800
POSITIVE-VOLTAGE REGULATORS

D2154, MAY 1976–REVISED DECEMBER 1982

- 3-Terminal Regulators
- Output Current up to 1.5 A
- No External Components
- Internal Thermal Overload Protection
- High Power Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Direct replacements for Fairchild μA7800 Series

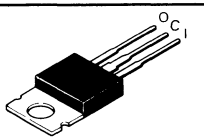
NOMINAL OUTPUT VOLTAGE	REGULATOR
5 V	uA7805C
6 V	uA7806C
8 V	uA7808C
8.5 V	uA7885C
10 V	uA7810C
12 V	uA7812C
15 V	uA7815C
18 V	uA7818C
24 V	uA7824C

KC PACKAGE
(TOP VIEW)



THE COMMON TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

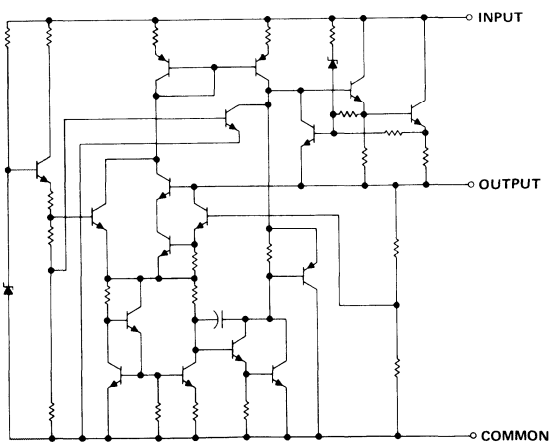
TO-220AB



description

This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 1.5 amperes of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power-pass element in precision regulators.

schematic



Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating temperature range (unless otherwise noted)

		uA78__C	UNIT
Input voltage	uA7824C	40	V
	All others	35	
Continuous total dissipation at 25°C free-air temperature (see Note 1)		2	W
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)		15	W
Operating free-air, case, or virtual junction temperature range		0 to 150	C
Storage temperature range		−65 to 150	C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

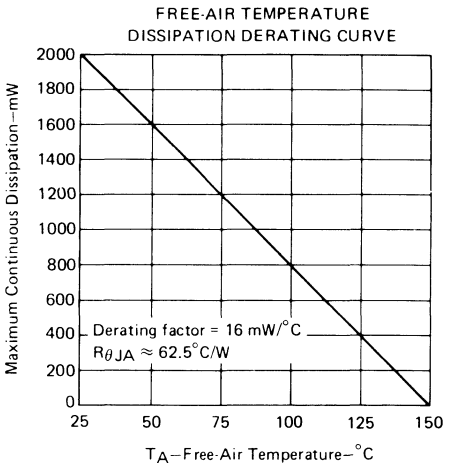


FIGURE 1

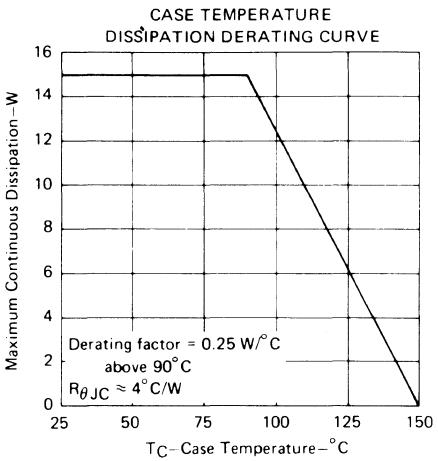


FIGURE 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA7805C	7	25	V
	uA7806C	8	25	
	uA7808C	10.5	25	
	uA7885C	10.5	25	
	uA7810C	12.5	28	
	uA7812C	14.5	30	
	uA7815C	17.5	30	
	uA7818C	21	33	
	uA7824C	27	38	
Output current, I_O			1.5	A
Operating virtual junction temperature, T_J		0	125	°C

uA7805C electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7805C			UNIT
			MIN	TYP	MAX	
Output voltage *		25°C	4.8	5	5.2	V
	I_O = 5 mA to 1 A, V_I = 7 V to 20 V, P ≤ 15 W	0°C to 125°C	4.75		5.25	
Input regulation	V_I = 7 V to 25 V	25°C		3	100	mV
	V_I = 8 V to 12 V			1	50	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	0°C to 125°C	62	78		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	100	mV
	I_O = 250 mA to 750 mA			5	50	
Output resistance	f = 1 kHz	0°C to 125°C		0.017		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1.1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		40		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.2	8	mA
Bias current change	V_I = 7 V to 25 V	0°C to 125°C			1.3	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		750		mA
Peak output current		25°C		2.2		A

uA7806C electrical characteristics at specified virtual junction temperature, V_I = 11 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7806C			UNIT
			MIN	TYP	MAX	
Output voltage *		25°C	5.75	6	6.25	V
	I_O = 5 mA to 1 A, V_I = 8 V to 21 V, P ≤ 15 W	0°C to 125°C	5.7		6.3	
Input regulation	V_I = 8 V to 25 V	25°C		5	120	mV
	V_I = 9 V to 13 V			1.5	60	
Ripple rejection	V_I = 9 V to 19 V, f = 120 Hz	0°C to 125°C	59	75		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		14	120	mV
	I_O = 250 mA to 750 mA			4	60	
Output resistance	f = 1 kHz	0°C to 125°C		0.019		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		45		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 8 V to 25 V	0°C to 125°C			1.3	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		550		mA
Peak output current		25°C		2.2		A

†All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

uA7808C electrical characteristics at specified virtual junction temperature, V_I = 14 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7808C			UNIT
			MIN	TYP	MAX	
Output voltage *		25°C	7.7	8	8.3	V
	I_O = 5 mA to 1 A, V_I = 10.5 V to 23 V, P ≤ 15 W	0°C to 125°C	7.6		8.4	
Input regulation	V_I = 10.5 V to 25 V	25°C		6	160	mV
	V_I = 11 V to 17 V			2	80	
Ripple rejection	V_I = 11.5 V to 21.5 V, f = 120 Hz	0°C to 125°C	56	72		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	160	mV
	I_O = 250 mA to 750 mA			4	80	
Output resistance	f = 1 kHz	0°C to 125°C		0.016		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		52		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 10.5 V to 25 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		450		mA
Peak output current		25°C		2.2		A

uA7885C electrical characteristics at specified virtual junction temperature, V_I = 15 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7885C			UNIT
			MIN	TYP	MAX	
Output voltage *		25°C	8.15	8.5	8.85	V
	I_O = 5 mA to 1 A, V_I = 11 V to 23.5 V, P ≤ 15 W	0°C to 125°C	8.1		8.9	
Input regulation	V_I = 10.5 V to 25 V	25°C		6	170	mV
	V_I = 11 V to 17 V			2	85	
Ripple rejection	V_I = 11.5 V to 21.5 V, f = 120 Hz	0°C to 125°C	54	70		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	170	mV
	I_O = 250 mA to 750 mA			4	85	
Output resistance	f = 1 kHz	0°C to 125°C		0.016		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		55		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 10.5 V to 25 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		450		mA
Peak output current		25°C		2.2		A

†All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

uA7810C electrical characteristics at specified virtual junction temperature, V_I = 17 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7810C			UNIT
			MIN	TYP	MAX	
Output voltage *		25°C	9.6	10	10.4	V
	I_O = 5 mA to 1 A, V_I = 12.5 V to 25 V, P ≤ 15 W	0°C to 125°C	9.5	10	10.5	V
Input regulation	V_I = 12.5 V to 28 V	25°C		7	200	mV
	V_I = 14 V to 20 V			2	100	mV
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	0°C to 125°C	55	71		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	200	mV
	I_O = 250 mA to 750 mA			4	100	mV
Output resistance	f = 1 kHz	0°C to 125°C		0.018		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1.0		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		70		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 12.5 V to 28 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	mA
Short-circuit output current		25°C		400		mA
Peak output current		25°C		2.2		A

uA7812C electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7812C			UNIT
			MIN	TYP	MAX	
Output voltage *		25°C	11.5	12	12.5	V
	I_O = 5 mA to 1 A, V_I = 14.5 V to 27 V, P ≤ 15 W	0°C to 125°C	11.4		12.6	V
Input regulation	V_I = 14.5 V to 30 V	25°C		10	240	mV
	V_I = 16 V to 22 V			3	120	mV
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	0°C to 125°C	55	71		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	240	mV
	I_O = 250 mA to 750 mA			4	120	mV
Output resistance	f = 1 kHz	0°C to 125°C		0.018		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1.0		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		75		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 14.5 V to 30 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	mA
Short-circuit output current		25°C		350		mA
Peak output current		25°C		2.2		A

† All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

uA7815C electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7815C			UNIT
			MIN	TYP	MAX	
Output voltage •		25°C	14.4	15	15.6	V
	I_O = 5 mA to 1 A, V_I = 17.5 V to 30 V, P ≤ 15 W	0°C to 125°C	14.25		15.75	
Input regulation	V_I = 17.5 V to 30 V	25°C		11	300	mV
	V_I = 20 V to 26 V			3	150	
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz	0°C to 125°C	54	70		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	300	mV
	I_O = 250 mA to 750 mA			4	150	
Output resistance	f = 1 kHz	0°C to 125°C		0.019		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1.0		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		90		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.4	8	mA
Bias current change	V_I = 17.5 V to 30 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		230		mA
Peak output current		25°C		2.1		A

uA7818C electrical characteristics at specified virtual junction temperature, V_I = 27 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7818C			UNIT
			MIN	TYP	MAX	
Output voltage •		25°C	17.3	18	18.7	V
	I_O = 5 mA to 1 A, V_I = 21 V to 33 V, P ≤ 15 W	0°C to 125°C	17.1		18.9	
Input regulation	V_I = 21 V to 33 V	25°C		15	360	mV
	V_I = 24 V to 30 V			5	180	
Ripple rejection	V_I = 22 V to 32 V, f = 120 Hz	0°C to 125°C	53	69		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	360	mV
	I_O = 250 mA to 750 mA			4	180	
Output resistance	f = 1 kHz	0°C to 125°C		0.022		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1.0		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		110		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.5	8	mA
Bias current change	V_I = 21 V to 33 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		200		mA
Peak output current		25°C		2.1		A

†All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

uA7824C electrical characteristics at specified virtual junction temperature, V_I = 33 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7824C			UNIT
			MIN	TYP	MAX	
Output voltage •		25°C	23	24	25	V
	I_O = 5 mA to 1 A, V_I = 27 V to 38 V, P ≤ 15 W	0°C to 125°C	22.8		25.2	
Input regulation	V_I = 27 V to 38 V	25°C		18	480	mV
	V_I = 30 V to 36 V			6	240	
Ripple rejection	V_I = 28 V to 38 V, f = 120 Hz	0°C to 125°C	50	66		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	480	mV
	I_O = 250 mA to 750 mA			4	240	
Output resistance	f = 1 kHz	0°C to 125°C		0.028		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1.5		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		170		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.6	8	mA
Bias current change	V_I = 27 V to 38 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		150		mA
Peak output current		25°C		2.1		A

†All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

SERIES uA78L00
POSITIVE-VOLTAGE REGULATORS

D2203, JANUARY 1976 – REVISED AUGUST 1983

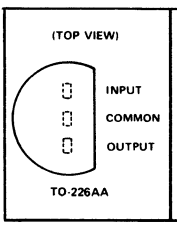
- 3-Terminal Regulators
- Output Current up to 100 mA
- No External Components
- Internal Thermal Overload Protection
- Unusually High Power Dissipation Capability
- Internal Short-Circuit Current Limiting
- Direct Replacement for Fairchild μA78L00 Series

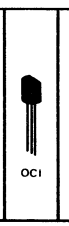
NOMINAL OUTPUT VOLTAGE	5% OUTPUT VOLTAGE TOLERANCE	10% OUTPUT VOLTAGE TOLERANCE
2.6 V	uA78L02AC	uA78L02C
5 V	uA78L05AC	uA78L05C
6.2 V	UA78L06AC	uA78L06C
8 V	uA78L08AC	uA78L08C
9 V	uA78L09AC	uA78L09C
10 V	uA78L10AC	uA78L10C
12 V	uA78L12AC	uA78L12C
15 V	uA78L15AC	uA78L15C

description

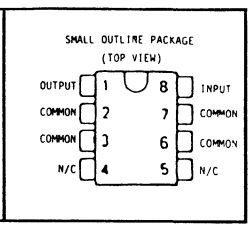
This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power-pass elements to make high-current voltage regulators. One of these regulators can deliver up to 100 mA of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. When used as a replacement for a Zener-diode–resistor combination, an effective improvement in output impedance of typically two orders of magnitude can be obtained together with lower-bias current.

LP
SILECT PACKAGE



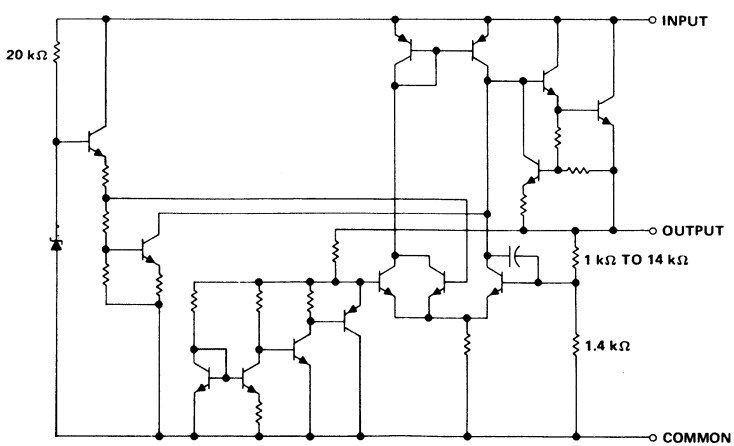


uA78L00...D



NC - NO INTERNAL CONNECTION

schematic



Resistor values shown are nominal

absolute maximum ratings over operating temperature range (unless otherwise noted)

		uA78L02AC, uA78L02C THRU uA78L10AC, uA78L10C	uA78L12AC, uA78L12C uA78L15AC, uA78L15C	UNIT
Input voltage		30	35	V
Continuous total dissipation at 25°C free-air temperature (see Note 1)	D package	833	833	mW
	LP package	775	775	
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)		1600	1600	mW
Operating free-air, case, or virtual junction temperature range		0 to 150	0 to 150	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	260	°C

NOTE 1: For operation above 25°C free-air temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

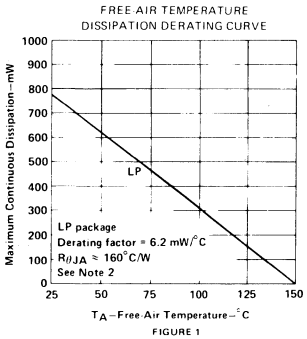


FIGURE 1

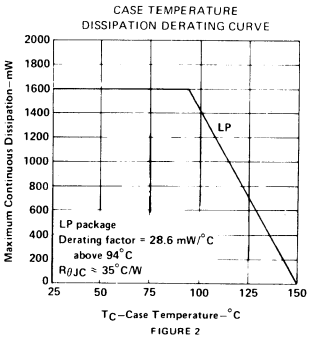


FIGURE 2

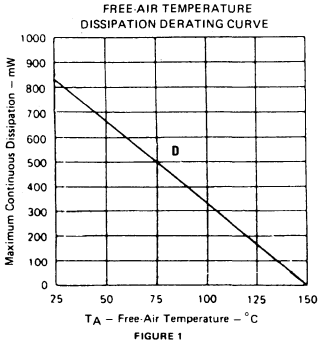


FIGURE 1

NOTE 2: This curve for the LP package is based on thermal resistance, $R_{\theta JA}$, measured in still air with the device mounted in an Augat socket. The bottom of the package was 3 8 inch above the socket.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA78L02C, uA78L02AC	4.75	20	V
	uA78L05C, uA78L05AC	7	20	
	uA78L06C, uA78L06AC	8.5	20	
	uA78L08C, uA78L08AC	10.5	23	
	uA78L09C, uA78L09AC	11.5	24	
	uA78L10C, uA78L10AC	12.5	25	
	uA78L12C, uA78L12AC	14.5	27	
	uA78L15C, uA78L15AC	17.5	30	
Output current, I_O			100	mA
Operating virtual junction temperature, T_J		0	125	°C

uA78L02AC, uA78L02C electrical characteristics at specified virtual junction temperature, V_I = 9 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L02AC			uA78L02C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage *		25°C	2.5	2.6	2.7	2.4	2.6	2.8	V
	V_I = 4.75 V to 20 V, I_O = 1 mA to 40 mA	0°C to 125°C	2.45		2.75	2.35		2.85	
	I_O = 1 mA to 70 mA		2.45		2.75	2.35		2.85	
Input regulation	V_I = 4.75 V to 20 V	25°C		20	100		20	125	mV
	V_I = 5 V to 20 V			16	75		16	100	
Ripple rejection	V_I = 6 V to 16 V, f = 120 Hz	25°C	43	51		42	51		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		12	50		12	50	mV
	I_O = 1 mA to 40 mA			6	25		6	25	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		30			30		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.6	6		3.6	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 5 V to 20 V	0°C to 125°C			2.5			2.5	mA
	I_O = 1 mA to 40 mA				0.1			0.2	

uA78L05AC, uA78L05C electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L05AC			uA78L05C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage *		25°C	4.8	5	5.2	4.6	5	5.4	V
	V_I = 7 V to 20 V, I_O = 1 mA to 40 mA	0°C to 125°C	4.75		5.25	4.5		5.5	
	I_O = 1 mA to 70 mA		4.75		5.25	4.5		5.5	
Input regulation	V_I = 7 V to 20 V	25°C		32	150		32	200	mV
	V_I = 8 V to 20 V			26	100		26	150	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	25°C	41	49		40	49		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		15	60		15	60	mV
	I_O = 1 mA to 40 mA			8	30		8	30	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		42			42		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.8	6		3.8	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 8 V to 20 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.1			0.2	

† All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse tchniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

uA78L06AC, uA78L06C electrical characteristics at specified virtual junction temperature, V_I = 12 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L06AC			uA78L06C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage •		25°C	5.95	6.2	6.45	5.7	6.2	6.7	V
	V_I = 8.5 V to 20 V, I_O = 1 mA to 40 mA	0°C to 125°C	5.9		6.5	5.6		6.8	
	I_O = 1 mA to 70 mA		5.9		6.5	5.6		6.8	
Input regulation	V_I = 8.5 V to 20 V	25°C		35	175		35	200	mV
	V_I = 9 V to 20 V			29	125		29	150	
Ripple rejection	V_I = 10 V to 20 V, f = 120 Hz	25°C	40	48		39	48		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		16	80		16	80	mV
	I_O = 1 mA to 40 mA			9	40		9	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		46			46		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.9	6		3.9	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 9 V to 20 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.1			0.2	

uA78L08AC, uA78L08C electrical characteristics at specified virtual junction temperature, V_I = 14 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L08AC			uA78L08C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage •		25°C	7.7	8	8.3	7.36	8	8.64	V
	V_I = 10.5 V to 23 V, I_O = 1 mA to 40 mA	0°C to 125°C	7.6		8.4	7.2		8.8	
	I_O = 1 mA to 70 mA		7.6		8.4	7.2		8.8	
Input regulation	V_I = 10.5 V to 23 V	25°C		42	175		42	200	mV
	V_I = 11 V to 23 V			36	125		36	150	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	25°C	37	46		36	46		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		18	80		18	80	mV
	I_O = 1 mA to 40 mA			10	40		10	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		54			54		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4	6		4	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 11 V to 23 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.1			0.2	

† All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

•This specification applies only for DC power dissipation permitted by absolute maximum ratings.

uA78L09AC, uA78L09C electrical characteristics at specified virtual junction temperature, V_I = 16 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L09AC			uA78L09C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage *		25°C	8.6	9	9.4	8.3	9	9.7	V
	V_I = 12 V to 24 V, I_O = 1 mA to 40 mA	0°C to 125°C	8.55		9.45	8.1		9.9	
	I_O = 1 mA to 70 mA		8.55		9.45	8.1		9.9	
Input regulation	V_I = 12 V to 24 V	25°C		45	175		45	225	mV
	V_I = 13 V to 24 V			40	125		40	175	
Ripple rejection	V_I = 13 V to 24 V, f = 120 Hz	25°C	37	45		36	45		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		19	90		19	90	mV
	I_O = 1 mA to 40 mA			11	40		11	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		58			58		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.1	6		4.1	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 13 V to 24 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.1			0.2	

uA78L10AC, uA78L10C electrical characteristics at specified virtual junction temperature, V_I = 17 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L10AC			uA78L10C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage *		25°C	9.6	10	10.4	9.2	10	10.8	V
	V_I = 13 V to 25 V, I_O = 1 mA to 40 mA	0°C to 125°C	9.5		10.5	9		10	
	I_O = 1 mA to 70 mA		9.5		10.5	9		10	
Input regulation	V_I = 13 V to 25 V	25°C		51	175		51	225	mV
	V_I = 14 V to 25 V			42	125		42	175	
Ripple rejection	V_I = 14 V to 25 V, f = 120 Hz	25°C	37	44		36	44		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		20	90		20	90	mV
	I_O = 1 mA to 40 mA			11	40		11	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		62			62		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.2	6		4.2	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 14 V to 25 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.1			0.2	

† All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

uA78L12AC, uA78L12C electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L12AC			uA78L12C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage*		25°C	11.5	12	12.5	11.1	12	12.9	V
	V_I = 14.5 V to 27 V, I_O = 1 mA to 40 mA	0°C to 125°C	11.4		12.6	10.8		13.2	
	I_O = 1 mA to 70 mA		11.4		12.6	10.8		13.2	
Input regulation	V_I = 14.5 V to 27 V	25°C		55	250		55	250	mV
	V_I = 16 V to 27 V			49	200		49	200	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	25°C	37	42		36	42		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		22	100		22	100	mV
	I_O = 1 mA to 40 mA			13	50		13	50	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		70			70		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.3	6.5		4.3	6.5	mA
		125°C			6			6	
Bias current change	V_I = 16 V to 27 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.1			0.2	

uA78L15AC, uA78L15C electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L15AC			uA78L15C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage *		25°C	14.4	15	15.6	13.8	15	16.2	V
	V_I = 17.5 V to 30 V, I_O = 1 mA to 40 mA	0°C to 125°C	14.25		15.75	13.5		16.5	
	I_O = 1 mA to 70 mA		14.25		15.75	13.5		16.5	
Input regulation	V_I = 17.5 V to 30 V	25°C		65	300		65	300	mV
	V_I = 20 V to 30 V			58	250		58	250	
Ripple rejection	V_I = 18.5 to 28.5 V, f = 120 Hz	25°C	34	39		33	39		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		25	150		25	150	mV
	I_O = 1 mA to 40 mA			15	75		15	75	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		82			82		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.6	6.5		4.6	6.5	mA
		125°C			6			6	
Bias current change	V_I = 10 V to 30 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.1			0.2	

† All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

SERIES uA78M00
POSITIVE-VOLTAGE REGULATORS

D2214, JUNE 1976 – REVISED SEPTEMBER 1983

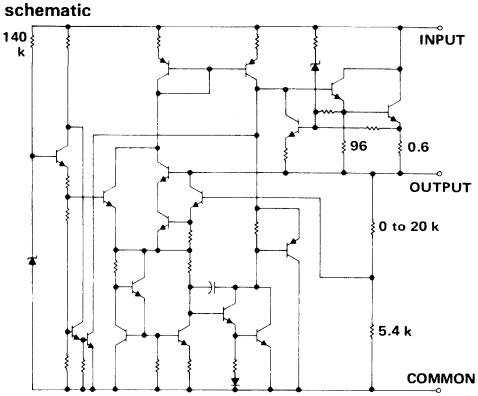
- 3-Terminal Regulators
- Output Current up to 500 mA
- No External Components
- Internal Thermal Overload Protection
- High Power Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Direct Replacements for Fairchild μA78M00 Series and National LM78MXX and LM341 Series

NOMINAL OUTPUT VOLTAGE	–55°C to 150°C OPERATING TEMPERATURE RANGE	0°C to 125°C OPERATING TEMPERATURE RANGE
5 V	uA78M05M	uA78M05C
6 V	uA78M06M	uA78M06C
8V	uA78M08M	uA78M08C
10 V	uA78M10M	uA78M10C
12 V	uA78M12M	uA78M12C
15 V	uA78M15M	uA78M15C
20 V		uA78M20C
24 V		uA78M24C
PACKAGES	JG	KC

description

This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 500 milliamperes of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

schematic

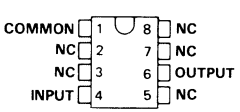


Resistor values shown are nominal and in ohms.

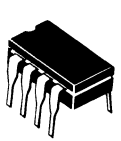
terminal assignments

uA78M_M . . . JG PACKAGE

(TOP VIEW)

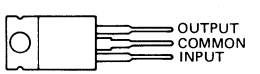


NC – No internal connection.



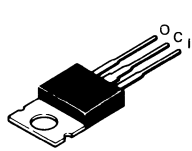
uA78M_C . . . KC PACKAGE

(TOP VIEW)



THE COMMON TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

TO-220AB



absolute maximum ratings over operating temperature range (unless otherwise noted)

		uA78M05M THRU uA78M24M	uA78M05C THRU uA78M24C	UNIT
Input voltage	uA78M20 thru uA78M24		40	V
	All others	35	35	
Continuous total dissipation at 25°C free-air temperature (see Note 1)	JG package	1.05		W
	KC (TO-220AB) package		2	
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)	KC package		7.5	W
Operating free-air, case, or virtual junction temperature range		−55 to 150	0 to 150	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300		°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	KC package		260	°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 through 3. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA78M05M, uA78M05C	7	25	V
	uA78M06M, uA78M06C	8	25	
	uA78M08M, uA78M08C	10.5	25	
	uA78M10M, uA78M10C	12.5	28	
	uA78M12M, uA78M12C	14.5	30	
	uA78M15M, uA78M15C	17.5	30	
	uA78M20C	23	35	
	uA78M24C	27	38	
Output current, I_O	All devices		500	mA
Operating virtual junction temperature, T_J	uA78M05M thru uA78M15M	−55	150	°C
	uA78M05C thru uA78M24C	0	125	

uA78M05M, uA78M05C electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA78M05M			uA78M05C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage *	I_O = 5 mA to 350 mA		25°C	4.8	5	5.2	4.8	5	5.2	V
		V_I = 8 V to 20 V	−55°C to 150°C	4.7		5.3				
		V_I = 7 V to 20 V	0°C to 125°C				4.75		5.25	
Input regulation	I_O = 200 mA	V_I = 7 V to 25 V	25°C		3	50		3	100	mV
		V_I = 8 V to 20 V			1	25				
		V_I = 8 V to 25 V						1	50	
Ripple rejection**	V_I = 8 V to 18 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	62						dB
			0°C to 125°C				62			
		I_O = 300 mA	25°C	62	80		62	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		20	50		20	100	mV
	I_O = 5 mA to 200 mA				10	25		10	50	
Temperature coefficient of output voltage**	I_O = 5 mA		−55°C to 25°C			−2				mV/°C
			25°C to 150°C			−1.5				
			0°C to 125°C					−1		
Output noise voltage**	f = 10 Hz to 100 kHz		25°C		40	200		40	200	μV
Dropout voltage			25°C		2	2.5		2	2.5	V
Bias current			25°C		4.5	7		4.5	6	mA
Bias current change	I_O = 200 mA, V_I = 8 V to 25 V		−55°C to 150°C			0.8				mA
			0°C to 125°C						0.8	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current	V_I = 35 V		25°C		300	500		300		mA
Peak output current**			25°C	0.5	0.7	1.4		0.7		A

†All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.
**For M-suffix devices these parameters are guaranteed but not tested.

uA78M06M, uA78M06C electrical characteristics at specified virtual junction temperature, V_I = 11 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA78M06M			uA78M06C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage *	I_O = 5 mA to 350 mA	V_I = 9 V to 21 V	25°C	5.75	6	6.25	5.75	6	6.25	V
			−55°C to 150°C	5.7		6.3				
		V_I = 8 V to 21 V	0°C to 125°C				5.7		6.3	
Input regulation	I_O = 200 mA	V_I = 8 V to 25 V	25°C		5	60		5	100	mV
		V_I = 9 V to 20 V			1.5	30				
		V_I = 9 V to 25 V						1.5	50	
Ripple rejection **	V_I = 9 V to 19 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	59						dB
			0°C to 125°C				59			
		I_O = 300 mA	25°C	59	80		59	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		20	60		20	120	mV
	I_O = 5 mA to 200 mA				10	30		10	60	
Temperature coefficient of output voltage **	I_O = 5 mA		−55°C to 25°C			−2.4				mV/°C
			25°C to 150°C			−1.8				
			0°C to 125°C					−1		
Output noise voltage**	f = 10 Hz to 100 kHz		25°C		45	240		45		μV
Dropout voltage			25°C		2	2.5		2		V
Bias current			25°C		4.5	7		4.5	6	mA
Bias current change	I_O = 200 mA, V_I = 9 V to 25 V		−55°C to 150°C			0.8				mA
			0°C to 125°C						0.8	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current	V_I = 35 V		25°C		270	600		270		mA
Peak output current **			25°C	0.5	0.7	1.4		0.7		A

†All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

**For M-suffix devices these parameters are guaranteed but not tested.

uA78M08M, uA78M08C electrical characteristics at specified virtual junction temperature, V_I = 14 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA78M08M			uA78M08C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage *	I_O = 5 mA to 350 mA		25°C	7.7	8	8.3	7.7	8	8.3	V
		V_I = 11.5 V to 23 V	−55°C to 150°C	7.6		8.4				
		V_I = 10.5 V to 23 V	0°C to 125°C				7.6		8.4	
Input regulation	I_O = 200 mA	V_I = 10.5 V to 25 V	25°C		6	60		6	100	mV
		V_I = 11 V to 20 V			2	30				
		V_I = 11 V to 25 V						2	50	
Ripple rejection**	V_I = 11.5 V to 21.5 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	56						dB
			0°C to 125°C				56			
		I_O = 300 mA	25°C	56	80		56	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		25	80		25	160	mV
	I_O = 5 mA to 200 mA				10	40		10	80	
Temperature coefficient of output voltage**	I_O = 5 mA		−55°C to 25°C			−3.2				mV/°C
			25°C to 150°C			−2.4				
			0°C to 125°C					−1		
Output noise voltage**	f = 10 Hz to 100 kHz		25°C		52	320		52		μV
Dropout voltage			25°C		2	2.5		2		V
Bias current			25°C		4.6	7		4.6	6	mA
Bias current change	I_O = 200 mA,	V_I = 11.5 V to 25 V	−55°C to 150°C			0.8				mA
		V_I = 10.5 V to 25 V	0°C to 125°C						0.8	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current	V_I = 35 V		25°C		250	600		250		mA
Peak output current**			25°C	0.5	0.7	1.4		0.7		A

†All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.
**For M-suffix devices these parameters are guaranteed but not tested.

uA78M10M, uA78M10C electrical characteristics at specified virtual junction temperature, V_I = 17 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA78M10M			uA78M10C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage*			25°C	9.6	10	10.4	9.6	10	10.4	V
	I_O = 5 mA to 350 mA	V_I = 13.5 V to 25 V	−55°C to 150°C	9.5		10.5				
		V_I = 12.5 V to 25 V	0°C to 125°C				9.5		10.5	
Input regulation	I_O = 200 mA	V_I = 12.5 V to 28 V	25°C		7	60		7	100	mV
		V_I = 14 V to 20 V			2	30				
		V_I = 14 V to 28 V						2	50	
Ripple rejection**	V_I = 15 V to 25 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	55						dB
			0°C to 125°C				55			
		I_O = 300 mA	25°C	55	80		55	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		25	100		25	200	mV
	I_O = 5 mA to 200 mA				10	50		10	100	
Temperature coefficient of output voltage**	I_O = 5 mA		−55°C to 25°C			−4				mV/°C
			25°C to 150°C			−3				
			0°C to 125°C					−1		
Output noise voltage**	f = 10 Hz to 100 kHz		25°C		64			64		μV
Dropout voltage			25°C		2	2.5		2		V
Bias current			25°C		4.7	6		4.7	6	mA
Bias current change	I_O = 200 mA,	V_I = 13.5 V to 28 V	−55°C to 150°C			0.8				mA
		V_I = 12.5 V to 28 V	0°C to 125°C						0.8	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current	V_I = 35 V		25°C		245	600		245		mA
Peak output current**			25°C	0.5	0.7	1.4		0.7		A

†All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

**For M-suffix devices these parameters are guaranteed but not tested.

uA78M12M, uA78M12C electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA78M12M			uA78M12C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage*			25°C	11.5	12	12.5	11.5	12	12.5	V
	I_O = 5 mA to 350 mA	V_I = 15.5 V to 27 V	−55°C to 150°C	11.4		12.6				
		V_I = 14.5 V to 27 V	0°C to 125°C				11.4		12.6	
Input regulation	I_O = 200 mA	V_I = 14.5 V to 30 V	25°C		8	60		8	100	mV
		V_I = 16 V to 25 V			2	30				
		V_I = 16 V to 30 V						2	50	
Ripple rejection**	V_I = 15 V to 25 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	55						dB
			0°C to 125°C				55			
		I_O = 300 mA	25°C	55	80		55	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		25	120		25	240	mV
	I_O = 5 mA to 200 mA				10	60		10	120	
Temperature coefficient of output voltage**	I_O = 5 mA		−55°C to 25°C			−4.8				mV/°C
			25°C to 150°C			−3.6				
			0°C to 125°C					−1		
Output noise voltage**	f = 10 Hz to 100 kHz		25°C		75	480		75		μV
Dropout voltage			25°C		2	2.5		2		V
Bias current			25°C		4.8	7		4.8	6	mA
Bias current change	I_O = 200 mA,	V_I = 15 V to 30 V	−55°C to 150°C			0.8				mA
		V_I = 14.5 V to 30 V	0°C to 125°C						0.8	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current	V_I = 35 V		25°C		240	600		240		mA
Peak output current**			25°C	0.5	0.7	1.4		0.7		A

†All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

**For M-suffix devices these parameters are guaranteed but not tested.

uA78M15M, uA78M15C electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA78M15M			uA78M15C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage*	I_O = 5 mA to 350 mA	V_I = 18.5 V to 30 V	25°C	14.4	15	15.6	14.4	15	15.6	V
			−55°C to 150°C	14.25		15.75				
		V_I = 17.5 V to 30 V	0°C to 125°C				14.25		15.75	
Input regulation	I_O = 200 mA	V_I = 17.5 V to 30 V	25°C		10	60		10	100	mV
		V_I = 20 V to 30 V			3	30		3	50	
Ripple rejection**	V_I = 18.5 V to 28.5 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	54						dB
			0°C to 125°C				54			
		I_O = 300 mA	25°C	54	70		54	70		
Output regulation	I_O = 5 mA to 500 mA		25°C		25	150		25	300	mV
	I_O = 5 mA to 200 mA				10	75		10	150	
Temperature coefficient of output voltage**	I_O = 5 mA		−55°C to 25°C			−6				mV/°C
			25°C to 150°C			−4.5				
			0°C to 125°C					−1		
Output noise voltage**	f = 10 Hz to 100 kHz		25°C		90	600		90		μV
Dropout voltage			25°C		2	2.5		2		V
Bias current			25°C		4.8	7		4.8	6	mA
Bias current change	I_O = 200 mA,	V_I = 18.5 V to 30 V	−55°C to 150°C			0.8				mA
		V_I = 17.5 V to 30 V	0°C to 125°C						0.8	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current	V_I = 35 V		25°C		240	600		240		mA
Peak output current**			25°C	0.5	0.7	1.4		0.7		A

†All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

**For M-suffix devices these parameters are guaranteed but not tested.

uA78M20C electrical characteristics at specified virtual junction temperature, V_I = 29 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA78M20C			UNIT
				MIN	TYP	MAX	
Output voltage *			25°C	19.2	20	20.8	V
	I_O = 5 mA to 350 mA,	V_I = 23 V to 35 V	0°C to 125°C	19		21	
Input regulation	I_O = 200 mA	V_I = 23 V to 35 V	25°C		10	100	mV
		V_I = 24 V to 35 V			5	50	
Ripple rejection	V_I = 24 V to 34 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	53			dB
		I_O = 300 mA	25°C	53	70		
Output regulation	I_O = 5 mA to 500 mA		25°C		30	400	mV
	I_O = 5 mA to 200 mA				10	200	
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1.1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		110		μV
Dropout voltage			25°C		2		V
Bias current			25°C		4.9	6	mA
Bias current change	I_O = 200 mA,	V_I = 23 V to 35 V	0°C to 125°C			0.8	mA
	I_O = 5 mA to 350 mA		0°C to 125°C			0.5	
Short-circuit output current	V_I = 35 V		25°C		240		mA
Peak output current			25°C		0.7		A

†All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

uA78M24C electrical characteristics at specified virtual junction temperature, V_I = 33 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA78M24C			UNIT
				MIN	TYP	MAX	
Output voltage *			25°C	23	24	25	V
	I_O = 5 mA to 350 mA,	V_I = 27 V to 38 V	0°C to 125°C	22.8		25.2	
Input regulation	I_O = 200 mA	V_I = 27 V to 38 V			10	100	mV
		V_I = 28 V to 38 V			5	50	
Ripple rejection	V_I = 28 V to 38 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C				dB
			0°C to 125°C	50			
		I_O = 300 mA	25°C	50	70		
Output regulation	I_O = 5 mA to 500 mA		25°C		30	480	mV
	I_O = 5 mA to 200 mA				10	240	
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1.2		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		170		μV
Dropout voltage			25°C		2		V
Bias current			25°C		5	6	mA
Bias current change	I_O = 200 mA,	V_I = 27 V to 38 V	0°C to 125°C			0.8	mA
	I_O = 5 mA to 350 mA		0°C to 125°C			0.5	
Short-circuit output current	V_I = 35 V		25°C		240		mA
Peak output current			25°C		0.7		A

†All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

THERMAL INFORMATION

KC PACKAGE
FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

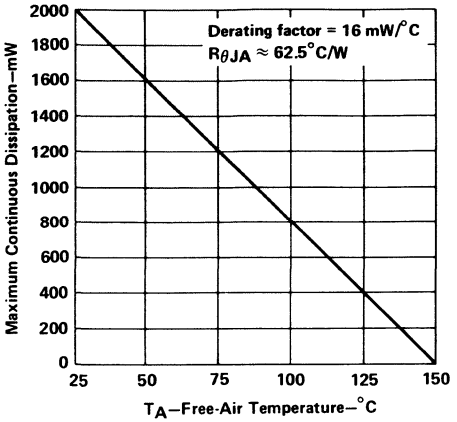


FIGURE 1

KC PACKAGE
CASE TEMPERATURE
DISSIPATION DERATING CURVE

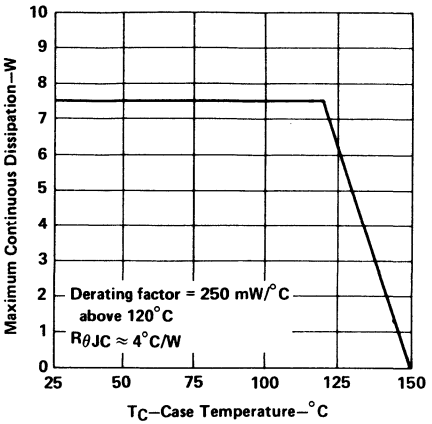


FIGURE 2

JG PACKAGE
CASE TEMPERATURE
DISSIPATION DERATING CURVE

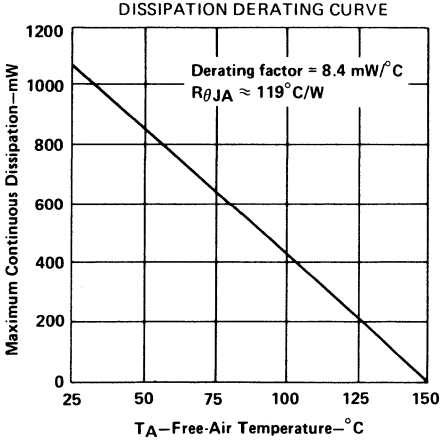


FIGURE 3

SERIES uA7900
NEGATIVE-VOLTAGE REGULATORS

D2215, JUNE 1976—REVISED AUGUST 1983

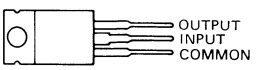
- 3-Terminal Regulators
- Output Current up to 1.5 A
- No External Components
- Internal Thermal Overload Protection
- High Power Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Essentially Equivalent to National LM320 Series
- Direct Replacements for Fairchild μA7900 Series and National LM79XX Series

NOMINAL OUTPUT VOLTAGE	REGULATOR
−5 V	uA7905C
−5.2 V	uA7952C
−6 V	uA7906C
−8 V	uA7908C
−12 V	uA7912C
−15 V	uA7915C
−18 V	uA7918C
−24 V	uA7924C

description

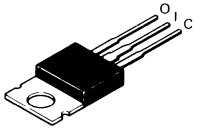
This series of fixed-negative-voltage monolithic integrated-circuit voltage regulators is designed to complement Series uA7800 in a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 1.5 amperes of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

KC PACKAGE
(TOP VIEW)

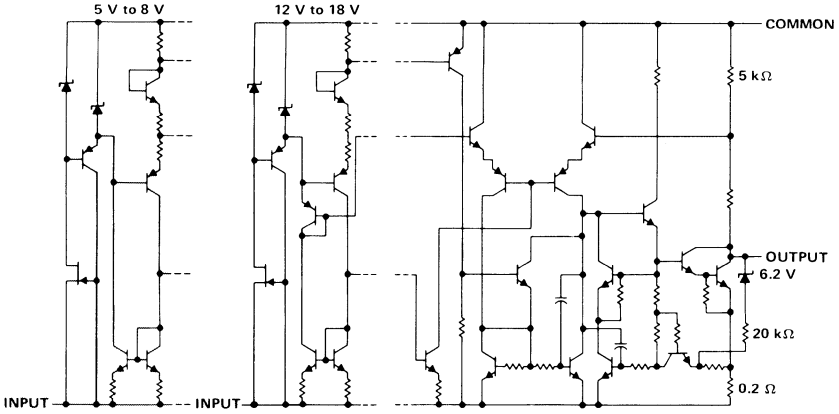


THE INPUT TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

TO-220AB



schematic



All component values are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)

		uA7905C THRU uA7924C	UNIT
Input voltage	uA7924C	−40	V
	All others	−35	
Continuous total dissipation at 25°C free-air temperature (see Note 1)		2	W
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)		15	W
Operating free-air, case, or virtual junction temperature range		0 to 150	C
Storage temperature range		−65 to 150	C
Lead temperature 3,2 mm (1/8 inch) from case for 10 seconds		260	C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

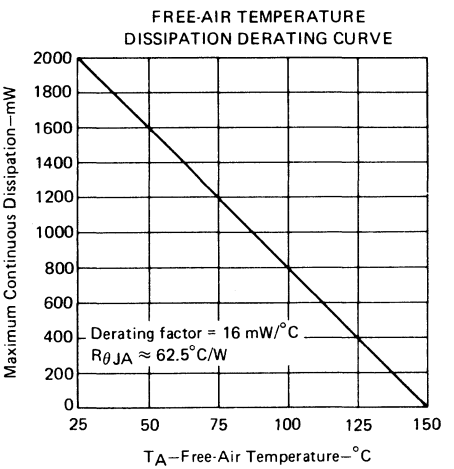


FIGURE 1

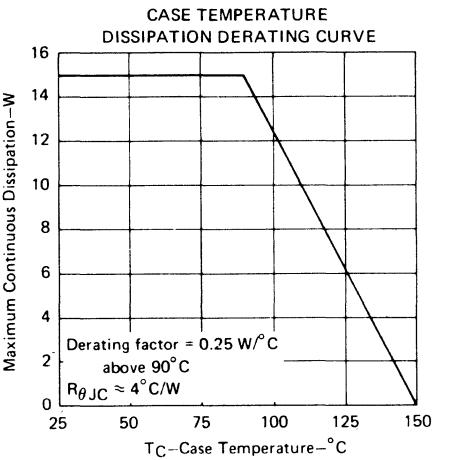


FIGURE 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA7905C	−7	−25	V
	uA7952C	−7.2	−25	
	uA7906C	−8	−25	
	uA7908C	−10.5	−25	
	uA7912C	−14.5	−30	
	uA7915C	−17.5	−30	
	uA7918C	−21	−33	
	uA7924C	−27	−38	
Output current, I_O			1.5	A
Operating virtual junction temperature, T_J		0	125	C

uA7905C electrical characteristics at specified virtual junction temperature, $V_I = -10$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7905C			UNIT
			MIN	TYP	MAX	
Output voltage*		25°C	−4.8	−5	−5.2	V
	I_O = 5 mA to 1 A, V_I = −7 V to −20 V, $P \leq 15$ W	0°C to 125°C	−4.75		−5.25	
Input regulation	V_I = −7 V to −25 V	25°C		12.5	50	mV
	V_I = −8 V to −12 V			4	15	
Ripple rejection	V_I = −8 V to −18 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	100	mV
	I_O = 250 mA to 750 mA			5	50	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.4		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		125		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	V_I = −7 V to −25 V	0°C to 125°C		0.15	0.5	mA
	I_O = 5 mA to 1 A			0.08	0.5	
Peak output current		25°C		2.1		A

uA7952C electrical characteristics at specified virtual junction temperature, $V_I = -10$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7952C			UNIT
			MIN	TYP	MAX	
Output voltage*		25°C	−5	−5.2	−5.4	V
	I_O = 5 mA to 1 A, V_I = −7.2 V to −20 V, $P \leq 15$ W	0°C to 125°C	−4.95		−5.45	
Input regulation	V_I = −7.2 V to −25 V	25°C		12.5	100	mV
	V_I = −8.2 V to −12 V			4	50	
Ripple rejection	V_I = −8.2 V to −18 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	100	mV
	I_O = 250 mA to 750 mA			5	50	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.4		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		125		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	V_I = −7.2 V to −25 V	0°C to 125°C		0.15	1.3	mA
	I_O = 5 mA to 1 A			0.08	0.5	
Peak output current		25°C		2.1		A

†All characteristics are measured with a solid-tantalum capacitor across the input of 2 μF and a solid-tantalum capacitor across the output of 1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

uA7906C electrical characteristics at specified virtual junction temperature, V_I = −11 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7906C			UNIT
			MIN	TYP	MAX	
Output voltage*		25°C	−5.75	−6	−6.25	V
	I_O = 5 mA to 1 A, V_I = −8 V to −21 V, P ≤ 15 W	0°C to 125°C	−5.7		−6.3	
Input regulation	V_I = −8 V to −25 V	25°C		12.5	120	mV
	V_I = −9 V to −13 V			4	60	
Ripple rejection	V_I = −9 V to −19 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	120	mV
	I_O = 250 mA to 750 mA			5	60	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.4		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		150		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	V_I = −8 V to −25 V	0°C to 125°C		0.15	1.3	mA
	I_O = 5 mA to 1 A			0.08	0.5	
Peak output current		25°C		2.1		A

uA7908C electrical characteristics at specified virtual junction temperature, V_I = −14 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7908C			UNIT
			MIN	TYP	MAX	
Output voltage*		25°C	−7.7	−8	−8.3	V
	I_O = 5 mA to 1 A, V_I = −10.5 V to −23 V, P ≤ 15 W	0°C to 125°C	−7.6		−8.4	
Input regulation	V_I = −10.5 V to −25 V	25°C		12.5	160	mV
	V_I = −11 V to −17 V			4	80	
Ripple rejection	V_I = −11.5 V to −21.5 V, f = 120Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	160	mV
	I_O = 250 mA to 750 mA			5	80	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.6		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		200		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	V_I = −10.5 V to −25 V	0°C to 125°C		0.15	1	mA
	I_O = 5 mA to 1 A			0.08	0.5	
Peak output current		25°C		2.1		A

†All characteristics are measured with a solid-tantalum capacitor across the input of 2 μF and a solid-tantalum capacitor across the output of 1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

uA7912C electrical characteristics at specified virtual junction temperature, $V_I = -19$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7912C			UNIT
			MIN	TYP	MAX	
Output voltage *		25°C	−11.5	−12	−12.5	V
	I_O = 5 mA to 1 A, V_I = −14.5 V to −27 V, P ≤ 15 W	0°C to 125°C	−11.4		−12.6	
Input regulation	V_I = −14.5 V to −30 V	25°C		5	80	mV
	V_I = −16 V to −22 V			3	30	
Ripple rejection	V_I = −15 V to −25 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	200	mV
	I_O = 250 mA to 750 mA			5	75	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		300		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		2	3	mA
Bias current change	V_I = −14.5 V to −30 V	0°C to 125°C		0.04	0.5	mA
	I_O = 5 mA to 1 A			0.06	0.5	
Peak output current		25°C		2.1		A

uA7915C electrical characteristics at specified virtual junction temperature, $V_I = -23$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7915C			UNIT
			MIN	TYP	MAX	
Output voltage*		25°C	−14.4	−15	−15.6	V
	I_O = 5 mA to 1 A, V_I = −17.5 V to −30 V, P ≤ 15 W	0°C to 125°C	−14.25		−15.75	
Input regulation	V_I = −17.5 V to −30 V	25°C		5	100	mV
	V_I = −20 V to −26 V			3	50	
Ripple rejection	V_I = −18.5 V to −28.5 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	200	mV
	I_O = 250 mA to 750 mA			5	75	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		375		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		2	3	mA
Bias current change	V_I = −17.5 V to −30 V	0°C to 125°C		0.04	0.5	mA
	I_O = 5 mA to 1 A			0.06	0.5	
Peak output current		25°C		2.1		A

†All characteristics are measured with a solid-tantalum capacitor across the input of 2 μF and a solid-tantalum capacitor across the output of 1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

uA7918C electrical characteristics at specified virtual junction temperature, V_I = −27 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7918C			UNIT
			MIN	TYP	MAX	
Output voltage*	I_O = 5 mA to 1 A, $P \leq 15$ W, V_I = −21 V to −33 V	25°C	−17.3	−18	−18.7	V
		0°C to 125°C	−17.1		−18.9	
Input regulation	V_I = −21 V to −33 V	25°C		5	360	mV
	V_I = −24 V to −30 V			3	180	
Ripple rejection	V_I = −22 V to −32 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		30	360	mV
	I_O = 250 mA to 750 mA			10	180	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		450		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		2	3	mA
Bias current change	V_I = −21 V to −33 V	0°C to 125°C		0.04	1	mA
	I_O = 5 mA to 1 A			0.06	0.5	
Peak output current		25°C		2.1		A

uA7924C electrical characteristics at specified virtual junction temperature, V_I = −33 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7924C			UNIT
			MIN	TYP	MAX	
Output voltage*	I_O = 5 mA to 1 A, $P \leq 15$ W, V_I = −27 V to −38 V	25°C	−23	−24	−25	V
		0°C to 125°C	−22.8		−25.2	
Input regulation	V_I = −27 V to −38 V	25°C		5	480	mV
	V_I = −30 V to −36 V			3	240	
Ripple rejection	V_I = −28 V to −38 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		85	480	mV
	I_O = 250 mA to 750 mA			25	240	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		600		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		2	3	mA
Bias current change	V_I = −27 V to −38 V	0°C to 125°C		0.04	1	mA
	I_O = 5 mA to 1 A			0.06	0.5	
Peak output current		25°C		2.1		A

†All characteristics are measured with a solid-tantalum capacitor across the input of 2 μF and a solid-tantalum capacitor across the output of 1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

SERIES uA79M00
NEGATIVE-VOLTAGE REGULATORS

D2216, JUNE 1976 - REVISED AUGUST 1983

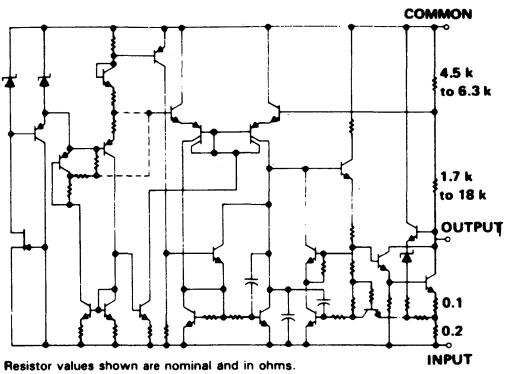
- 3-Terminal Regulators
- Output Current up to 500 mA
- No External Components
- High Power Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Direct Replacements for Fairchild μA79M00 Series

NOMINAL OUTPUT VOLTAGE	−55°C TO 150°C OPERATING TEMPERATURE RANGE	0°C TO 125°C OPERATING TEMPERATURE RANGE
−5 V	uA79M05M	uA79M05C
−6 V	uA79M06M	uA79M06C
−8 V	uA79M08M	uA79M08C
−12 V	uA79M12M	uA79M12C
−15 V	uA79M15M	uA79M15C
−20 V		uA79M20C
−24 V		uA79M24C
PACKAGE	JG	KC

description

This series of fixed-negative-voltage monolithic integrated-circuit voltage regulators is designed to complement Series uA78M00 in a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 500 milliamperes of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

schematic

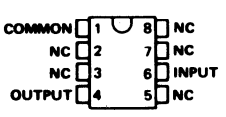


Resistor values shown are nominal and in ohms.

terminal assignments

uA79M_M. . .JG PACKAGE

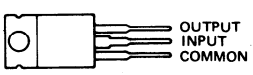
(TOP VIEW)



NC—No internal connection

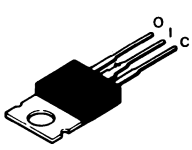
uA79M_C. . .KC PACKAGE

(TOP VIEW)



THE INPUT TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

TO-220AB



absolute maximum ratings over operating temperature range (unless otherwise noted)

		uA79M05M THRU uA79M15M	uA79M05C THRU uA79M24C	UNIT
Input voltage	uA79M20, uA79M24		−40	V
	All others	−35	−35	
Continuous total dissipation at 25°C free-air temperature (see Note 1)	JG package	1.05		W
	KC (TO-220AB) package		2	
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)	KC package		7.5	W
Operating free-air, case or virtual junction temperature range		−55 to 150	0 to 150	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	KC package		260	°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 through 3. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual dvice electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA79M05M, uA79M05C	−7	−25	V
	uA79M06M, uA79M06C	−8	−25	
	uA79M08M, uA79M08C	−10.5	−25	
	uA79M12M, uA79M12C	−14.5	−30	
	uA79M15M, uA79M15C	−17.5	−30	
	uA79M20C	−23	−35	
	uA79M24C	−27	−38	
Output current, I_O			500	mA
Operating virtual junction temperature, T_J	uA79M05M thru uA79M15M	−55	150	°C
	uA79M05C thru uA79M24C	0	125	

uA79M05M, uA79M05C electrical characteristics at specified virtual junction temperature, $V_I = -10$ V, $I_O = 350$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M05M			uA79M05C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage *	I_O = 5 mA to 350 mA, V_I = −7 V to −25 V		25°C	−4.8	−5	−5.2	−4.8	−5	−5.2	V
			−55°C to 150°C	−4.75		−5.25				
			0°C to 125°C				−4.75		−5.25	
Input regulation	V_I = −7 V to −25 V		25°C		7	50		7	50	mV
	V_I = −8 V to −18 V				3	30		3	30	
Ripple rejection **	V_I = −8 V to −18 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	50						dB
			0°C to 125°C				50			
		I_O = 300 mA	25°C	54	60		54	60		
Output regulation	I_O = 5 mA to 500 mA		25°C		75	100		75	100	mV
	I_O = 5 mA to 350 mA				50			50		
Temperature coefficient of output voltage **	I_O = 5 mA		−55°C to 150°C			−1.5				mV/°C
			0°C to 125°C					−0.4		
Output noise voltage**	f = 10 Hz to 100 kHz		25°C		125	400		125		μV
Dropout voltage			25°C		1.1	2.3		1.1		V
Bias current			25°C		1	2		1	2	mA
Bias current change	V_I = −8 V to −25 V		−55°C to 150°C			0.4				mA
			0°C to 125°C						0.4	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.4				
			0°C to 125°C						0.4	
Short-circuit output current	V_I = −30 V		25°C			600		140		mA
Peak output current**			25°C	0.5	0.65	1.4		0.65		A

†All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

**For M-suffix devices these parameters are guaranteed but not tested.

uA79M06M, uA79M06C electrical characteristics at specified virtual junction temperature, V_I = −11 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M06M			uA79M06C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage *			25 C	−5.75	−6	−6.25	−5.75	−6	−6.25	V
	I_O = 5 mA to 350 mA, V_I = −8 V to −25 V		−55 C to 150 C	−5.7		−6.3				
			0 C to 125 C				−5.7		−6.3	
Input regulation	V_I = −8 V to −25 V		25 C		7	60		7	60	mV
	V_I = −9 V to −19 V				3	40		3	40	
Ripple rejection **	V_I = −9 V to −19 V, f = 120 Hz	I_O = 100 mA	−55 C to 150 C	50						dB
			0 C to 125 C				50			
		I_O = 300 mA	25 C	54	60		54	60		
Output regulation	I_O = 5 mA to 500 mA		25 C		80	120		80	120	mV
	I_O = 5 mA to 350 mA				55			55		
Temperature coefficient of output voltage **	I_O = 5 mA		−55 C to 150 C			−1.5				mV/°C
			0 C to 125 C					−0.4		
Output noise voltage **	f = 10 Hz to 100 kHz		25 C		150	480		150		μV
Dropout voltage			25 C		1.1	2.3		1.1		V
Bias current			25 C		1	2		1	2	mA
Bias current change	V_I = −9 V to −25 V		−55 C to 150 C			0.4				mA
			0 C to 125 C						0.4	
	I_O = 5 mA to 350 mA		−55 C to 150 C			0.4				
			0 C to 125 C						0.4	
Short-circuit output current	V_I = −30 V		25 C			600		140		mA
Peak output current **			25 C	0.5	0.65	1.4		0.65		A

† All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

**For M-suffix devices these parameters are guaranteed but not tested.

uA79M08M, uA79M08C electrical characteristics at specified virtual junction temperature, $V_I = -19$ V, $I_O = 350$ mA (unless noted)

PARAMETER	TEST CONDITIONS†			uA79M08M			uA79M08C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage *			25 C	−7.7	−8	−8.3	−7.7	−8	−8.3	V
	I_O = 5 mA to 350 mA, V_I = −10.5 V to −25 V		−55 C to 150 C	−7.6		−8.4				
			0 C to 125 C				−7.6		−8.4	
Input regulation	V_I = −10.5 V to −25 V		25 C		8	80		8	80	mV
	V_I = −11 V to −21 V				4	50		4	50	
Ripple rejection **	V_I = −11.5 V to −21.5 V, f = 120 Hz	I_O = 100 mA	−55 C to 150 C	50						dB
			0 C to 125 C				50			
		I_O = 300 mA	25 C	54	59		54	59		
Output regulation	I_O = 5 mA to 500 mA		25 C		90	160		90	160	mV
	I_O = 5 mA to 350 mA				60			60		
Temperature coefficient of output voltage **	I_O = 5 mA		−55 C to 150 C			−2.4				mV/ C
			0 C to 125 C					−0.6		
Output noise voltage**	f = 10 Hz to 100 kHz		25 C		200	640		200		μV
Dropout voltage			25 C		1.1	2.3		1.1		V
Bias current			25 C		1	2		1	2	mA
Bias current change	V_I = −10.5 V to −25 V		−55 C to 150 C			0.4				mA
			0 C to 125 C						0.4	
	I_O = 5 mA to 350 mA		−55 C to 150 C			0.4				
			0 C to 125 C						0.4	
Short-circuit output current	V_I = −30 V		25 C			600		140		mA
Peak output current**			25 C	0.5	0.65	1.4		0.65		A

†All characteristics are measured with a 2 μF capacitor across the input and a 1 μF capacitor across the output. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

**For M-suffix devices these parameters are guaranteed but not tested.

uA79M12M, uA79M12C electrical characteristics at specified virtual junction temperature, V_I = −19 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M12M			uA79M12C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage *			25°C	−11.5	−12	−12.5	−11.5	−12	−12.5	V
	I_O = 5 mA to 350 mA, V_I = −14.5 V to −30 V		−55°C to 150°C	−11.4		−12.6				
			0°C to 125°C				−11.4		−12.6	
Input regulation	V_I = −14.5 V to −30 V		25°C		9	80		9	80	mV
	V_I = −15 V to −25 V				5	50		5	50	
Ripple rejection **	V_I = −15 V to −25 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	50						dB
			0°C to 125°C				50			
		I_O = 300 mA	25°C	54	60		54	60		
Output regulation	I_O = 5 mA to 500 mA		25°C		65	240		65	240	mV
	I_O = 5 mA to 350 mA				45			45		
Temperature coefficient of output voltage **	I_O = 5 mA		−55°C to 150°C			−3.6				mV/°C
			0°C to 125°C					−0.8		
Output noise voltage **	f = 10 Hz to 100 kHz		25°C		300	960		300		μV
Dropout voltage			25°C		1.1	2.3		1.1		V
Bias current			25°C		1.5	3		1.5	3	mA
Bias current change	V_I = −14.5 V to −30 V		−55°C to 150°C			0.4				mA
			0°C to 125°C						0.4	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.4				
			0°C to 125°C						0.4	
Short-circuit output current	V_I = −30 V		25°C			600		140		mA
Peak output current **			25°C	0.5	0.65	1.4		0.65		A

†All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

**For M-suffix devices these parameters are guaranteed but not tested.

uA79M15M, uA79M15C electrical characteristics at specified virtual junction temperature, $V_I = -23$ V, $I_O = 350$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M15M			uA79M15C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage*	I_O = 5 mA to 350 mA, V_I = −17.5 V to −30 V		25 C	−14.4	−15	−15.6	−14.4	−15	−15.6	V
			−55 C to 150 C	−14.25		−15.75				
			0 C to 125 C				−14.25		−15.75	
Input regulation	V_I = −17.5 V to −30 V		25 C		9	80		9	80	mV
	V_I = −18 V to −28 V				7	50		7	50	
Ripple rejection **	V_I = −18.5 V to −28.5 V, f = 120 Hz	I_O = 100 mA	−55 C to 150 C	50						dB
			0 C to 125 C				50			
		I_O = 300 mA	25 C	54	59		54	59		
Output regulation	I_O = 5 mA to 500 mA		25 C		65	240		65	240	mV
	I_O = 5 mA to 350 mA				45			45		
Temperature coefficient of output voltage **	I_O = 5 mA		−55 C to 150 C			−4.5				mV/ C
			0 C to 125 C					−1		
Output noise voltage**	f = 10 Hz to 100 kHz		25 C		375	1200		375		μV
Dropout voltage			25 C		1.1	2.3		1.1		V
Bias current			25 C		1.5	3		1.5	3	mA
Bias current change	V_I = −17.5 V to −30 V		−55 C to 150 C			0.4				mA
			0 C to 125 C						0.4	
	I_O = 5 mA to 350 mA		−55 C to 150 C			0.4				
			0 C to 125 C						0.4	
Short-circuit output current	V_I = −30 V		25 C			600		140		mA
Peak output current**			25 C		0.5	0.65		0.65		A

† All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

**For M-suffix devices these parameters are guaranteed but not tested.

uA79M20C electrical characteristics at specified virtual junction temperature
V_I = −29 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M20C			UNIT
				MIN	TYP	MAX	
Output voltage *	I_O = 5 mA to 350 mA, V_I = −23 V to −35 V		25°C	−19.2	−20	−20.8	V
			0°C to 125°C	−19		−21	
Input regulation	V_I = −23 V to −35 V		25°C		12	80	mV
	V_I = −24 V to −34 V				10	70	
Ripple rejection	V_I = −24 V to −34 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	50			dB
		I_O = 300 mA	25°C	54	58		
Output regulation	I_O = 5 mA to 500 mA		25°C		75	300	mV
	I_O = 5 mA to 350 mA				50		
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		500		μV
Dropout voltage			25°C		1.1		V
Bias current			25°C		1.5	3.5	mA
Bias current change	V_I = −23 V to −35 V		0°C to 125°C			0.4	mA
	I_O = 5 mA to 350 mA					0.4	
Short-circuit output current	V_I = −30 V		25°C		140		mA
Peak output current			25°C		650		A

† All characteristics are measured with a 2 μF capacitor across the input and a 1 μF capacitor across the output. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

uA79M24C electrical characteristics at specified virtual junction temperature, $V_I = -33$ V, $I_O = 350$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M24C			UNIT
				MIN	TYP	MAX	
Output voltage*	I_O = 5 mA to 350 mA, V_I = −27 V to −38 V		25°C	−23	−24	−25	V
			0°C to 125°C	−22.8		−25.2	
Input regulation	V_I = −27 V to −38 V		25°C		12	80	mV
	V_I = −28 V to −38 V				12	70	
Ripple rejection	V_I = −28 V to −38 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	50			dB
		I_O = 300 mA	25°C	54	58		
Output regulation	I_O = 5 mA to 500 mA		25°C		75	300	mV
	I_O = 5 mA to 350 mA				50		
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		600		μV
Dropout voltage			25°C		1.1		V
Bias current			25°C		1.5	3.5	mA
Bias current change	V_I = −27 V to −38 V		0°C to 125°C			0.4	mA
	I_O = 5 mA to 350 mA					0.4	
Short-circuit output current	V_I = −30 V		25°C		140		mA
Peak output current			25°C		650		A

†All characteristics are measured with a 2 μF capacitor across the input and a 1 μF capacitor across the output. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

*This specification applies only for DC power dissipation permitted by absolute maximum ratings.

THERMAL INFORMATION

KC PACKAGE
FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

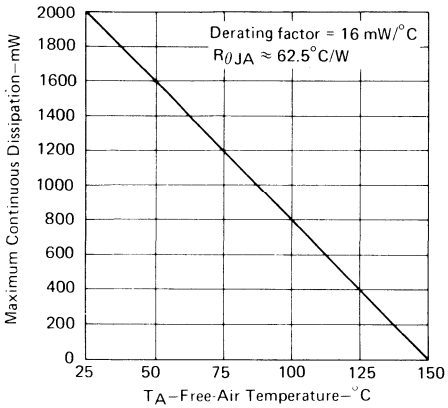


FIGURE 1

KC PACKAGE
CASE TEMPERATURE
DISSIPATION DERATING CURVE

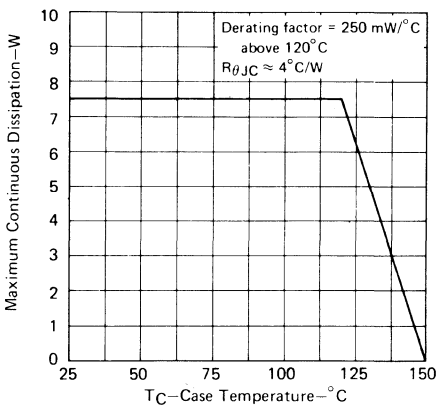


FIGURE 2

JG PACKAGE
FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

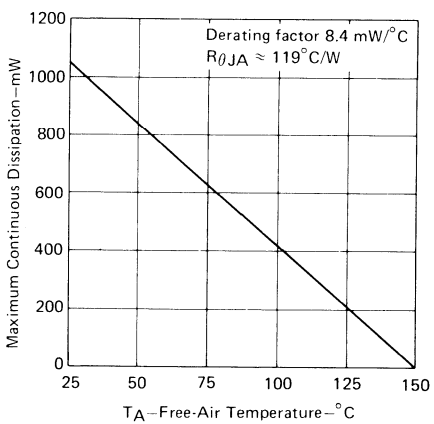


FIGURE 3

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Special Functions 5

Voltage Regulators 6

Data Acquisition 7

Appendix A

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TLC532, TLC533, LinCMOS 8-bit A/D Converter with 5 Analog and 6 Dual-purpose Inputs 7-221
TLC540, TLC541, LinCMOS 8-bit A/D Peripherals with Serial Control and 11 Inputs 7-231
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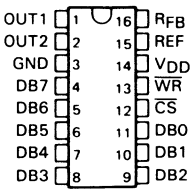
TLC7524, Advanced LinCMOS Multiplying D/A Converter 7-255
TLC7528, Advanced LinCMOS Dual Multiplying D/A Converter 7-263

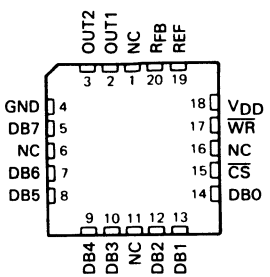
- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonicity Over Entire A/D Conversion Range**
- **Segmented High-Order Bits Ensure Low-Glitch Output**
- **Designed to be Interchangeable with Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320**

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	½ LSB Max
Power dissipation at V_{DD} = 5 V	5 mW Max
Settling time	100 ns Max
Propagation delay	80 ns Max

N PACKAGE
(TOP VIEW)



AD7524J . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The AD7524 is an Advanced LinCMOS™ 8-bit digital-to-analog converter (DAC) designed for easy interface to most popular microprocessors.

The AD7524 is an 8-bit multiplying DAC with input latches and with a load cycle similar to the "write" cycle of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most-significant bits, which produce the highest glitch impulse. The AD7524 provides accuracy to ½ LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5 mW typically.

Featuring operation from a 5-V to 15-V single supply, the AD7524 interfaces easily to most microprocessor buses or output ports. Excellent multiplying (2 or 4 quadrant) makes the AD7524 an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

The AD7524A is characterized for operation from −25°C to 85°C, and the AD7524J is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING
DEVICE	PACKAGE SUFFIXES	TEMPERATURE RANGE
AD7524A	N	−25°C to 85°C
AD7524J	N, FN	0°C to 70°C

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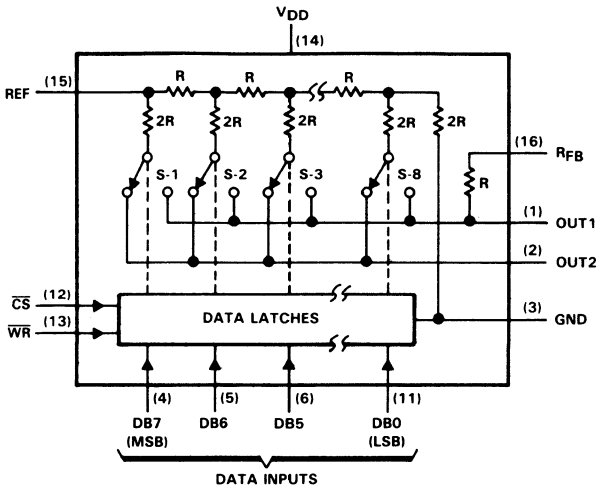
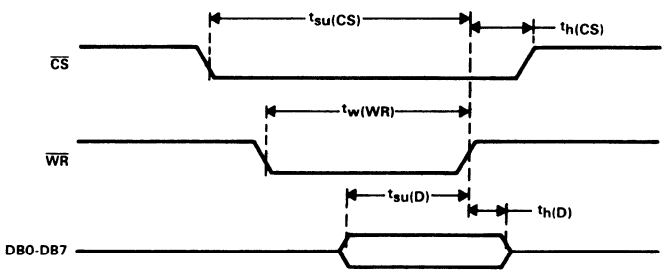
functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD}	−0.3 V to 17 V
Voltage between R_{FB} and GND	±25 V
Digital input voltage, V_I	−0.3 V to V_{DD} +0.3 V
Reference voltage, V_{ref}	±25 V
Peak digital input current, I_I	10 μA
Operating free-air temperature range: AD7524A	−25°C to 85°C
AD7524J	0°C to 70°C
Storage temperature range	−65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

recommended operating conditions

		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V_{ref}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input voltage, V_{IL}				0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$		40			40			ns
$\overline{CS}$ hold time, $t_{h(CS)}$		0			0			ns
Data bus input setup time, $t_{su(D)}$		25			25			ns
Data bus input hold time, $t_{h(D)}$		10			10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		40			40			ns
Operating free-air temperature, T_A	AD7524A	−25		85	−25		85	°C
	AD7524J	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{IH}	High-level input current		$V_I = V_{DD}$	Full range			10			10	μA
				25°C			1			1	
I_{IL}	Low-level input current		V_I = 0	Full range			−10			−10	μA
				25°C			−1			−1	
I_{lkg}	Output leakage current	OUT1	DB0-DB7 at 0, $\overline{WR}$ and $\overline{CS}$ at 0 V, V_{ref} = ±10 V	Full range			±400			±200	nA
				25°C			±50			±50	
		OUT2	DB0-DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0 V, V_{ref} = ±10 V	Full range			±400			±200	
				25°C			±50			±50	
I_{DD}	Supply current	Quiescent	DB0-DB7 at V_{IH}min or V_{IL}max	Full range			2			2	mA
				25°C			1			2	
		Standby	DB0-DB7 at 0 V or V_{DD}	Full range			500			500	μA
				25°C			100			100	
k_{SVS}	Supply voltage sensitivity, $\Delta gain/\Delta V_{DD}$		ΔV_{DD} = 10%	Full range		0.01	0.16		0.005	0.04	%/%
				25°C		0.002	0.08		0.001	0.02	
C_i	Input capacitance, DB0-DB7, $\overline{WR}$, $\overline{CS}$		V_I = 0				5			5	pF
C_o	Output capacitance	OUT1	DB0-DB7 at 0, $\overline{WR}$ and $\overline{CS}$ at 0 V				30			30	pF
		OUT2					120			120	
		OUT1	DB0-DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0 V				120			120	
		OUT2					30			30	
	Reference input impedance (REF to GND)				5		20	5		20	kΩ

operating characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC} = 5 V		V_{DD} = 15 V		UNIT
			MIN	MAX	MIN	MAX	
Linearity error				±0.2		±0.2	%FSR
Gain error	See Note 1	Full range		±1.4		±0.6	%FSR
		25°C		±1		±0.5	
Settling time (to 1/2 LSB)	See Note 2			100		100	ns
Propagation delay from digital input to 90% of final analog output current	See Note 2			80		80	ns
Feedthrough at OUT1 or OUT2	V_{ref} = ±10 V (100 kHz sinewave), $\overline{WR}$ and $\overline{CS}$ at 0, DB0-DB7 at 0	Full range		0.5		0.5	%FSR
		25°C		0.25		0.25	
Temperature coefficient of gain	T_A = 25°C to t_{min} or t_{max}			±0.004		±0.001	%FSR/°C

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
2. OUT1 load = 100 Ω, C_{ext} = 13 pF, $\overline{WR}$ at 0 V, $\overline{CS}$ at 0 V, DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.

PRINCIPLES OF OPERATION

The AD7524 is an 8-bit multiplying D/A converter consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded and these decoded bits, through a modification in the R-2R ladder, control three equally weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 1. With all digital inputs low, the entire reference current, I_{ref}, is switched to OUT2. The current source I/256 represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30 pF maximum) appears at OUT2 and the on-state switch capacitance (120 pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 1. Analysis of the circuit for all digital inputs high is similar to Figure 1; however, in this case, I_{ref} would be switched to OUT1.

Interfacing the AD7524 D/A converter to a microprocessor is accomplished via the data bus and the $\overline{CS}$ and $\overline{WR}$ control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the AD7524 analog output responds to the data activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs are latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The AD7524 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

PRINCIPLES OF OPERATION

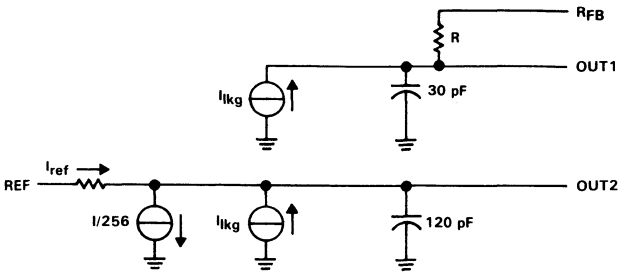


FIGURE 1. AD7524 EQUIVALENT CIRCUIT WITH ALL DIGITAL INPUTS LOW

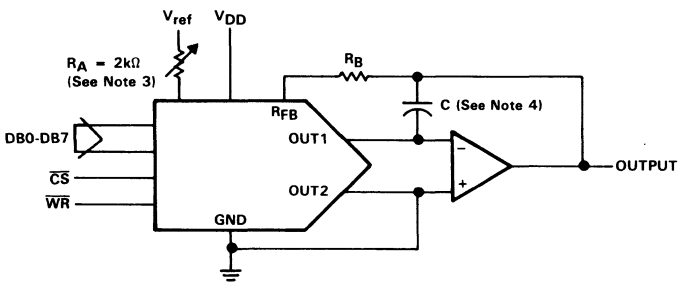


FIGURE 2. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

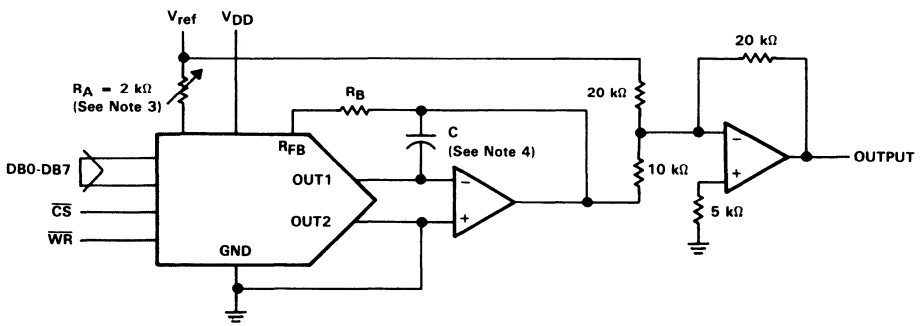


FIGURE 3. BIPOLAR OPERATION (4-QUADRANT OPERATION)

NOTES: 3. R_A and R_B used only if gain adjustment is required.
4. C phase compensation (10-15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

PRINCIPLES OF OPERATION

Table 1. Unipolar Binary Code

DIGITAL INPUT (SEE NOTE 5) MSB LSB	ANALOG OUTPUT
11111111	$-V_{ref}$ (255/256)
10000001	$-V_{ref}$ (129/256)
10000000	$-V_{ref}$ (128/256) = $-V_{ref}/2$
01111111	$-V_{ref}$ (127/256)
00000001	$-V_{ref}$ (1/256)
00000000	0

Table 2. Bipolar (Offset Binary) Code

DIGITAL INPUT (SEE NOTE 6) MSB LSB	ANALOG OUTPUT
11111111	V_{ref} (127/128)
10000001	V_{ref} (1/128)
10000000	0
01111111	$-V_{ref}$ (1/128)
00000001	$-V_{ref}$ (127/128)
00000000	$-V_{ref}$

NOTES: 5. LSB = 1/256 (V_{ref}).
6. LSB = 1/128 (V_{ref}).

microprocessor interfaces

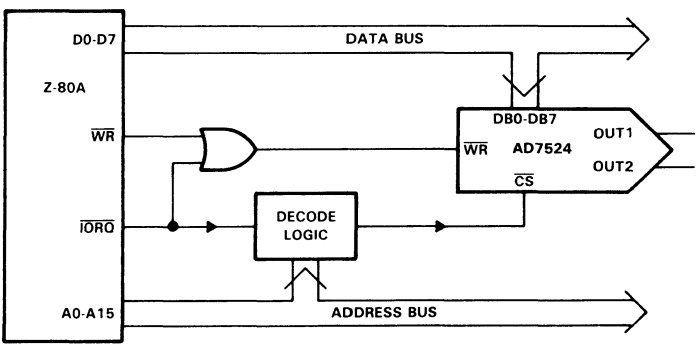


FIGURE 4. AD7524—Z-80A INTERFACE

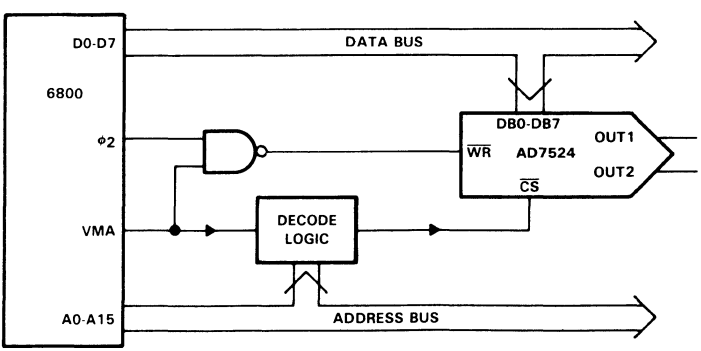


FIGURE 5. AD7524—6800 INTERFACE

microprocessor interfaces (continued)

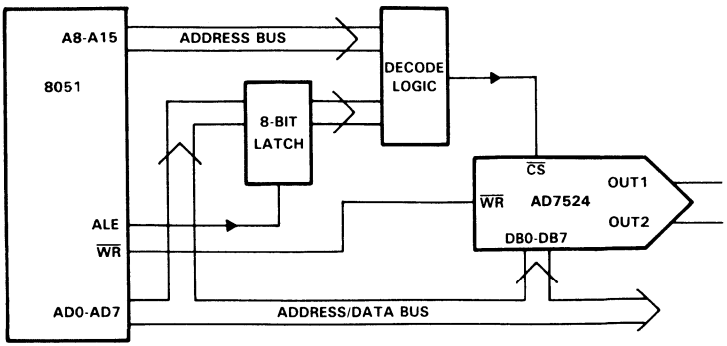


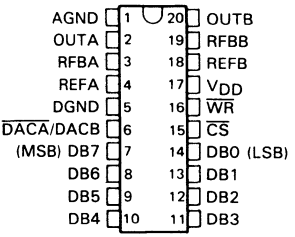
FIGURE 6. AD7524—8051 INTERFACE

Advanced LinCMOS™ DUAL 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

D3112, JULY 1988

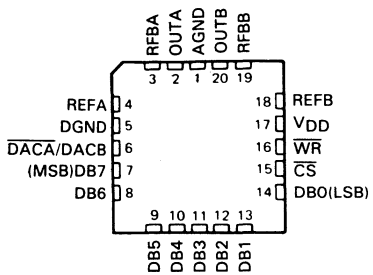
- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonic Over the Entire A/D Conversion Range**
- **Designed to be Interchangeable with Analog Devices AD7528 and PMI PM-7528**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320**

N PACKAGE
(TOP VIEW)



KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 bits
Linearity Error	1/2 LSB
Power Dissipation at V_{DD} = 5 V	5 mW
Settling Time at V_{DD} = 5 V	100 ns
Propagation Delay at V_{DD} = 5 V	80 ns

FN PACKAGE
(TOP VIEW)



description

The AD7528 is a dual 8-bit digital-to-analog converter designed with separate on-chip data latches and featuring excellent DAC-to-DAC matching. Data is transferred to either of the two DAC data latches via a common 8-bit input port. Control input DACA/DACB determines which DAC is to be loaded. The "load" cycle of the AD7528 is similar to the "write" cycle of a random-access memory, allowing easy interface to most popular microprocessor busses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

The AD7528 operates from a 5-V to 15-V power supply and dissipates less than 15 mW (typical). Excellent 2- or 4-quadrant multiplying makes the AD7528 a sound choice for many microprocessor-controlled gain-setting and signal-control applications.

The AD7528B is characterized for operation from −25°C to 85°C. The AD7528K is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING
DEVICE	PACKAGE SUFFIX	TEMPERATURE RANGE
AD7528B	FN, N	−25°C to 85°C
AD7528K	FN, N	0°C to 70°C

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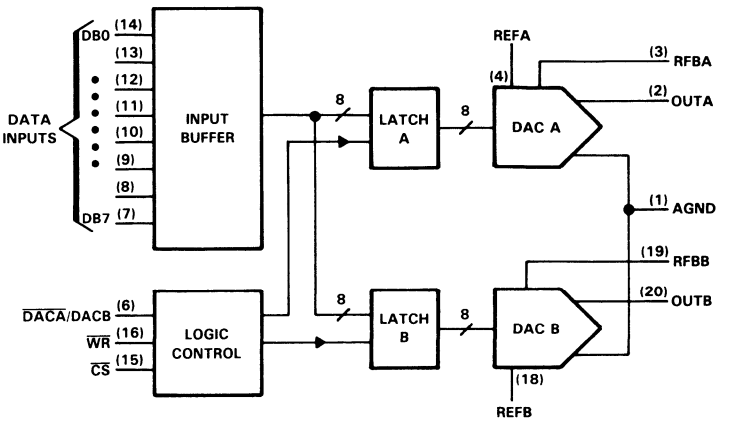
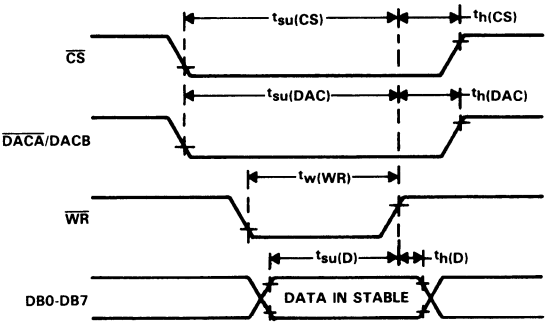
functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (to AGND or DGND) . . . . . −0.3 V to 17 V
Voltage between AGND and DGND . . . . . ±V_{DD}
Input voltage, V_I (to DGND) . . . . . −0.3 V to V_{DD} +0.3 V
Reference voltage, V_{refA} or V_{refB} (to AGND) . . . . . ±25 V
Feedback voltage, V_{RFBA} or V_{RFBB} (to AGND) . . . . . ±25 V
Output voltage, V_{OA} or V_{OB} (to AGND) . . . . . ±25 V
Peak input current . . . . . 10 μA
Operating free-air temperature range: AD7528B . . . . . −25°C to 85°C
AD7528K . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

recommended operating conditions

		V_{DD} = 4.75 V to 5.25 V			V_{DD} = 14.5 V to 15.5 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Reference voltage, V_{refA} or V_{refB}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input voltage, V_{IL}				0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$		50			50			ns
$\overline{CS}$ hold time, $t_{h(CS)}$		0			0			ns
DAC select setup time, $t_{su(DAC)}$		50			50			ns
DAC select hold time, $t_{h(DAC)}$		10			10			ns
Data bus input setup time $t_{su(D)}$		25			25			ns
Data bus input hold time $t_{h(D)}$		0			0			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		50			50			ns
Operating free-air temperature, T_A	AD7528B	−25		85	−25		85	°C
	AD7528K	0		70	0		70	

electrical characteristics over recommended operating temperature range, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 15 V		UNIT
					MIN	MAX	MIN	MAX	
I_{IH}	High-level input current		$V_I = V_{DD}$	Full Range		10		10	μA
				25°C		1		1	
I_{IL}	Low-level input current		V_I = 0	Full Range		−10		−10	μA
				25°C		−1		−1	
	Reference input impedance (Pin 15 to GND)				8	15	8	15	kΩ
I_{lkg}	Output leakage current	OUTA	DAC data latch loaded with 00000000, V_{refA} = ±10 V	Full Range		±400		±200	nA
				25°C		±50		±50	
		OUTB	DAC data latch loaded with 00000000, V_{refB} = ±10 V	Full Range		±400		±200	
				25°C		±50		±50	
	Input resistance match (REFA to REFB)					±1%		±1%	
	DC supply sensitivity Δgain/ΔV_{DD}		V_{DD} = ±10%	Full Range		0.04		0.02	%/%
				25°C		0.02		0.01	
I_{DD}	Supply current	Quiescent	DB0-DB7 at V_{IH}min or V_{IL}max			1		1	mA
		Standby	DB0-DB7 at 0 V or V_{DD}	Full Range		0.5		0.5	
				25°C		0.1		0.1	
C_i	Input capacitance	DB0-DB7	V_I = 0 or V_{DD}			10		10	pF
		$\overline{WR}$, $\overline{CS}$, $\overline{DACA}$/DACB				15		15	
C_o	Output capacitance (OUTA, OUTB)		DAC Data latches loaded with 00000000			50		50	pF
			DAC Data latches loaded with 11111111			120		120	

operating characteristics over recommended operating free-air temperature range, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Linearity error						±1/2			±1/2	LSB
Setting time (to 1/2 LSB)		See Note 1				100			100	ns
Gain error		See Note 2	Full Range			±4			±3	LSB
			25°C			±2			±2	
AC feedthrough	REFA to OUTA	See Note 3	Full Range			−65			−65	dB
	REFB to OUTB		25°C			−70			−70	
Temperature coefficient of gain						0.007			0.0035	%FSR/°C
Propagation delay (from digital input to 90% of final analog output current)		See Note 4				80			80	ns
Channel-to-channel isolation	REFA to OUTB	See Note 5	25°C		77			77		dB
	REFB to OUTA	See Note 6	25°C		77			77		
Digital-to-analog glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C			160			440		nVs
Digital crosstalk glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C			30			60		nVs
Harmonic distortion		V_i = 6 V, f = 1 kHz, T_A = 25°C			−85			−85		dB

NOTES: 1. OUTA, OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
2. Gain error is measured using an internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
3. V_{ref} = 20 V peak-to-peak, 100-kHz sine wave; DAC data latches loaded with 0000000.
4. V_{refA} = V_{refB} = 10 V; OUTA/OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
5. Both DAC latches loaded with 11111111; V_{refA} = 20 V peak-to-peak, 100-kHz sine wave; V_{refB} = 0.
6. Both DAC latches loaded with 11111111; V_{refB} = 20 V peak-to-peak, 100-kHz sine wave; V_{refA} = 0.

principles of operation

The AD7528 contains two identical 8-bit multiplying D/A converters, DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA with all digital inputs low is shown in Figure 1.

Figure 2 shows the DACA equivalent circuit. A similar equivalent circuit can be drawn for DACB. Both DACs share the analog ground pin 1 (AGND). With all digital inputs high, the entire reference current flows to OUTA. A small leakage current (I_{lkg}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. C_O is due to the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_O is 50 pF to 120 pF maximum. The equivalent output resistance r_O varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

Interfacing the AD7528 to a microprocessor is accomplished via the data bus, $\overline{CS}$, $\overline{WR}$, and $\overline{DACA}$/DACB control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the AD7528 analog output, specified by the $\overline{DACA}$/DACB control line, responds to the activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs is latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The digital inputs of the AD7528 provide TTL compatibility when operated from a supply voltage of 5 V. The AD7528 may be operated with any supply voltage in the range from 5 V to 15 V, however, input logic levels are not TTL compatible above 5 V.

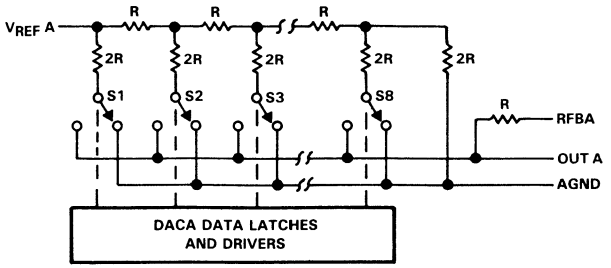


FIGURE 1. SIMPLIFIED FUNCTIONAL CIRCUIT FOR DACA

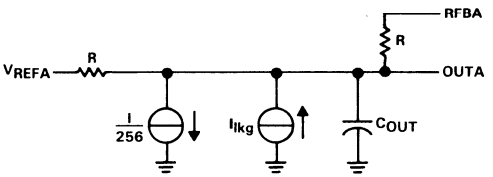


FIGURE 2. AD7528 EQUIVALENT CIRCUIT, DACA LATCH LOADED WITH 11111111.

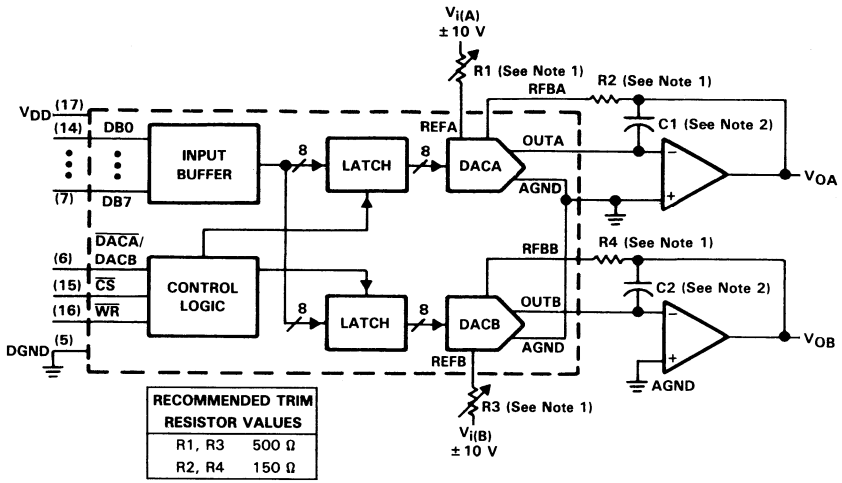
MODE SELECTION TABLE

$\overline{DACA}$/DACB	$\overline{CS}$	$\overline{WR}$	DACA	DACB
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = low level, H = high level, X = don't care

TYPICAL APPLICATION DATA

The AD7528 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 3 and 4. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

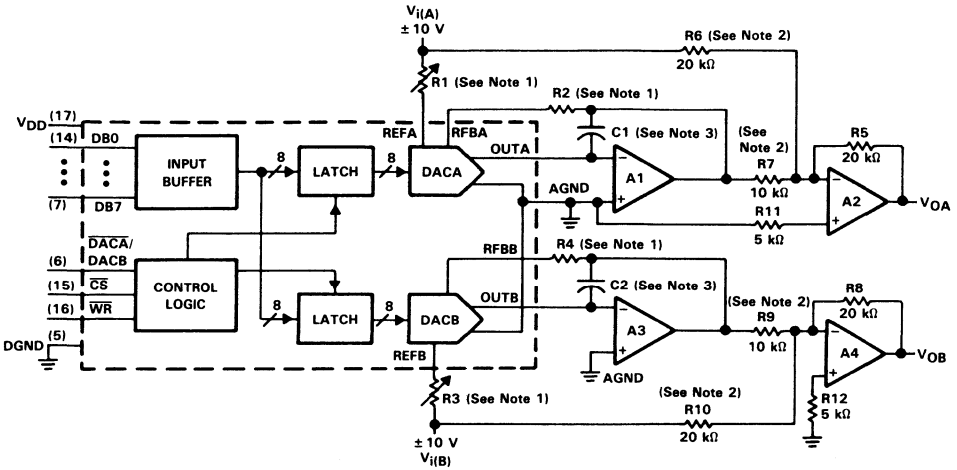


RECOMMENDED TRIM RESISTOR VALUES	
R1, R3	500 Ω
R2, R4	150 Ω

NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.
2. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

FIGURE 3. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

TYPICAL APPLICATION DATA



NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table in Figure 3 for recommended values. Adjust R1 for V_{OA} = 0 V with code 10000000 in DACA latch. Adjust R3 for V_{OB} = 0 V with 10000000 in DACB latch.
2. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
3. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

FIGURE 4. BIPOLAR OPERATION (4-QUADRANT OPERATION)

TABLE 1. UNIPOLAR BINARY CODE

DAC LATCH CONTENTS MSB LSB†	ANALOG OUTPUT
11111111	$-V_i$ (255/256)
10000001	$-V_i$ (129/256)
10000000	$-V_i$ (128/256) = $-V_i/2$
01111111	$-V_i$ (127/256)
00000001	$-V_i$ (1/256)
00000000	$-V_i$ (0/256) = 0

† 1 LSB = $(2^{-8})V_i$

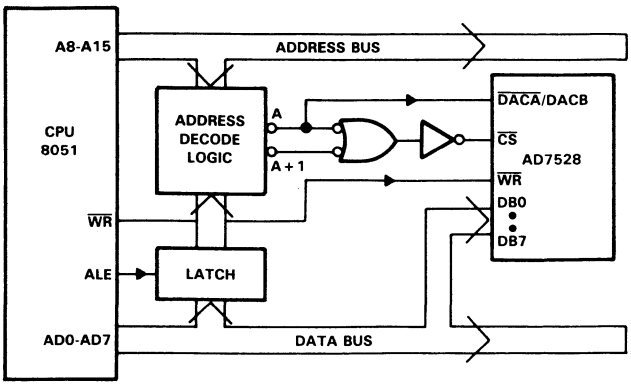
TABLE 2. BIPOLAR (OFFSET BINARY) CODE

DAC LATCH CONTENTS MSB LSB‡	ANALOG OUTPUT
11111111	V_i (127/128)
10000001	V_i (1/128)
10000000	0 V
01111111	$-V_i$ (1/128)
00000001	$-V_i$ (127/128)
00000000	$-V_i$ (128/128)

‡ 1 LSB = $(2^{-7})V_i$

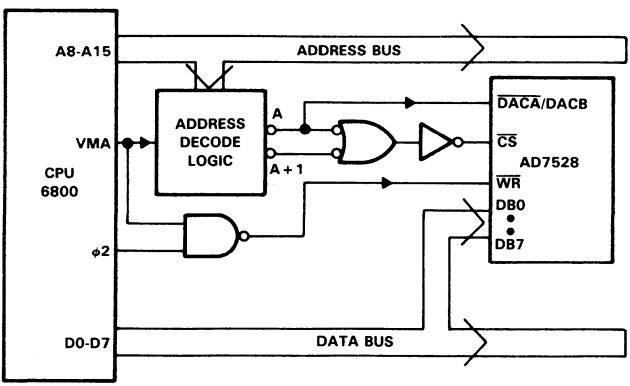
TYPICAL APPLICATION DATA

microprocessor interface information



NOTE: A = decoded address for AD7528 DACA.
A + 1 = decoded address for AD7528 DACB.

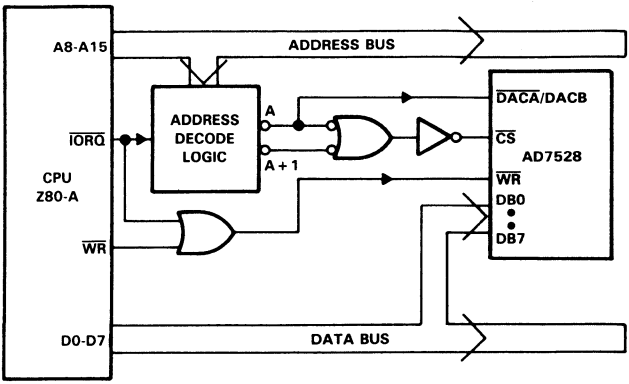
FIGURE 5. AD7528 — INTEL 8051 INTERFACE



NOTE: A = decoded address for AD7528 DACA.
A + 1 = decoded address for AD7528 DACB.

FIGURE 6. AD7528 — 6800 INTERFACE

TYPICAL APPLICATION DATA



NOTE: A = decoded address for AD7528 DACA.
A + 1 = decoded address for AD7528 DACB.

FIGURE 7. AD7528 TO Z-80A INTERFACE

programmable window detector

The programmable window comparator shown in Figure 8 will determine if voltage applied to the DAC feedback resistors are within the limits programmed into the AD7528 data latches. Input signal range depends on the reference and polarity, that is, the test input range is 0 to $-V_{ref}$. The DACA and DACB data latches are programmed with the upper and lower test limits. A signal within the programmed limits will drive the output high.

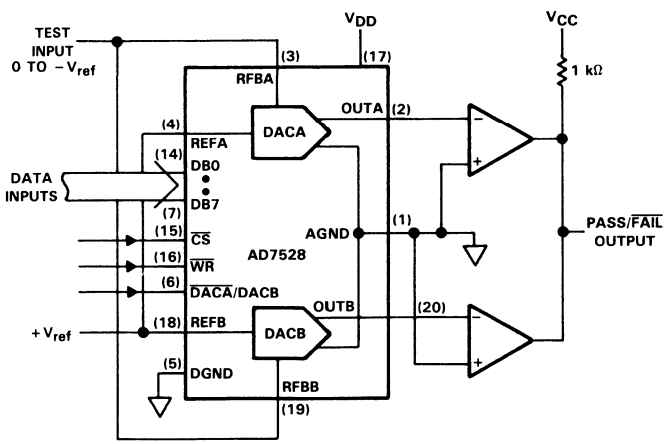


FIGURE 8. DIGITALLY PROGRAMMABLE WINDOW COMPARATOR (UPPER- AND LOWER-LIMIT TESTER)

TYPICAL APPLICATION DATA

digitally controlled signal attenuator

Figure 9 shows the AD7528 configured as a two-channel programmable attenuator. Applications include stereo audio and telephone signal level control. Table 3 shows input codes vs attenuation for a 0 to 15.5 dB range.

Attentuation db = $-20 \log_{10} D/256$, D = digital input code

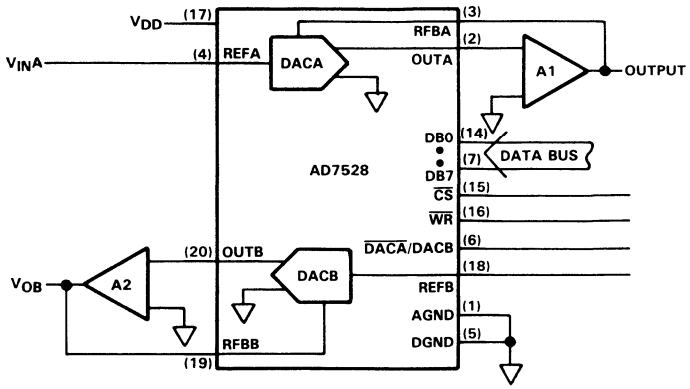


FIGURE 9. DIGITALLY CONTROLLED DUAL TELEPHONE ATTENUATOR

TABLE 3. ATTENUATION vs DACA, DACB CODE

ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL	ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL
0	11111111	255	8.0	01100110	102
0.5	11110010	242	8.5	01100000	96
1.0	11100100	228	9.0	01011011	91
1.5	11010111	215	9.5	01010110	86
2.0	11001011	203	10.0	01010001	81
2.5	11000000	192	10.5	01001100	76
3.0	10110101	181	11.0	01001000	72
3.5	10101011	171	11.5	01000100	68
4.0	10100010	162	12.0	01000000	64
4.5	10011000	152	12.5	00111101	61
5.0	10010000	144	13.0	00111001	57
5.5	10001000	136	13.5	00110110	54
6.0	10000000	128	14.0	00110011	51
6.5	01111001	121	14.5	00110000	48
7.0	01110010	114	15.0	00101110	46
7.5	01101100	108	15.5	00101011	43

TYPICAL APPLICATION DATA

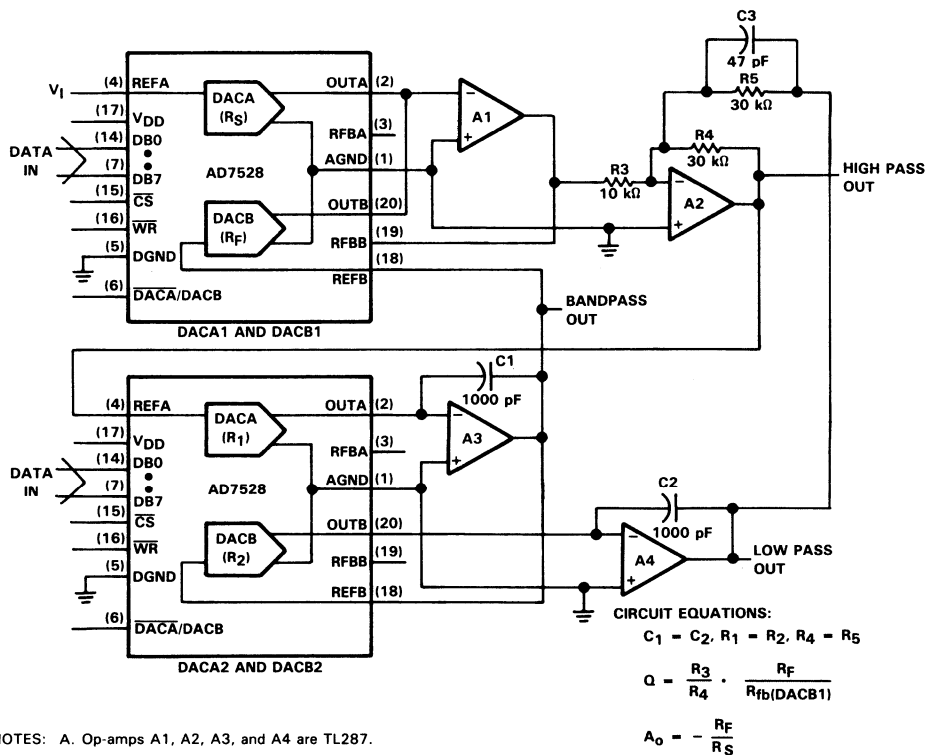
programmable state-variable filter

This programmable state-variable or universal filter configuration provides low-pass, high-pass, and band-pass outputs, and is suitable for applications in which microprocessor control of filter parameters is required.

As shown in Figure 10, DACA1 and DACB1 control the gain and Q of the filter while DACA2 and DACB2 control the cutoff frequency. Both halves of the DACA2 and DACB2 must track accurately in order for the cutoff-frequency equation to be true. With the AD7528, this is easily achieved.

$$f_C = \frac{1}{2\pi\, R1\, C1}$$

The programmable range for the cutoff or center frequency is 0 to 15 kHz with a Q ranging from 0.3 to 4.5. This defines the limits of the component values.



NOTES: A. Op-amps A1, A2, A3, and A4 are TL287.

B. C3 compensates for the op-amp gain-bandwidth limitations.

C. DAC equivalent resistance equals $\frac{256 \times \text{(DAC ladder resistance)}}{\text{DAC digital code}}$

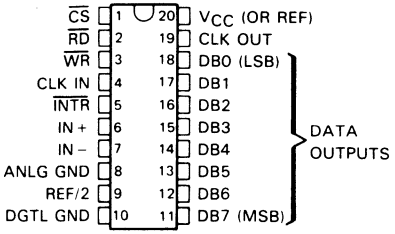
FIGURE 10. DIGITALLY CONTROLLED STATE-VARIABLE FILTER

ADC0801, ADC0802, ADC0803, ADC0805
8-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH DIFFERENTIAL INPUTS

D2754, NOVEMBER 1983 - REVISED FEBRUARY 1985

- **8-Bit Resolution**
- **Ratiometric Conversion**
- **100 μs Conversion Time**
- **135 ns Access Time**
- **Guaranteed Monotonicity**
- **High Reference Ladder Impedance 8 kΩ Typical**
- **No Zero Adjust Requirement**
- **On-Chip Clock Generator**
- **Single 5-Volt Power Supply**
- **Operates with Microprocessor or as Stand-Alone**
- **Designed to be Interchangeable with National Semiconductor and Signetics ADC0801,ADC0802, ADC0803, ADC0805**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



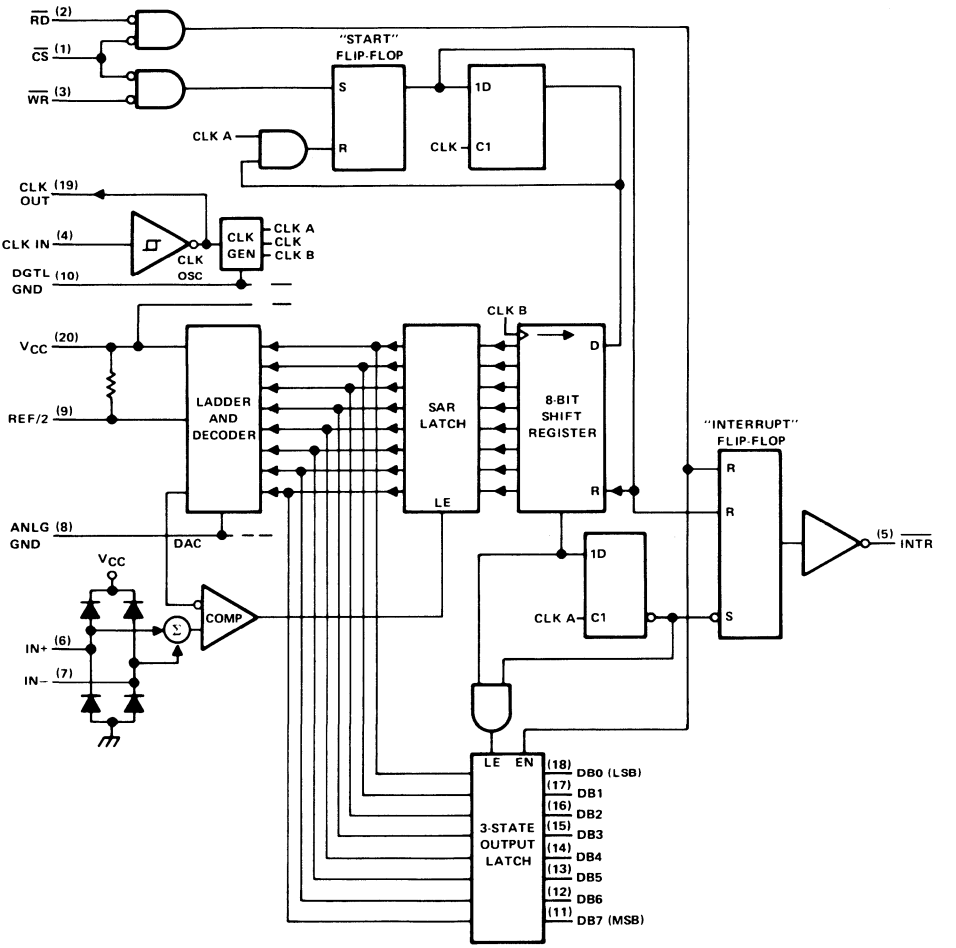
description

The ADC0801, ADC0802, ADC0803, and ADC0805 are CMOS 8-bit successive-approximation analog-to-digital converters that use a modified potentiometric (256R) ladder. These devices are designed to operate from common microprocessor control buses, with the three-state output latches driving the data bus. The devices can be made to appear to the microprocessor as a memory location or an I/O port. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

A differential analog voltage input allows increased common-mode rejection and offset of the zero-input analog voltage value. Although a reference input (REF/2) is available to allow 8-bit conversion over smaller analog voltage spans or to make use of an external reference, ratiometric conversion is possible with the REF/2 input open. Without an external reference, the conversion takes place over a span from V_{CC} to analog ground (ANLG GND). The devices can operate with an external clock signal or, with an additional resistor and capacitor, can operate using an on-chip clock generator.

The ADC0801I, ADC0802I, ADC0803I, and ADC0805I are characterized for operation from $-40°C$ to $85°C$. The ADC0801C, ADC0802C, ADC0803C, and ADC0805C are characterized from $0°C$ to $70°C$.

functional block diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range CS, RD, WR . . . . . −0.3 V to 18 V
Other inputs . . . . . −0.3 V to V_{CC} +0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} +0.3 V
Operating free-air temperature range: ADC080_I . . . . . −40°C to 85°C
ADC080_C . . . . . 0°C to 70°C

NOTE 1: All voltage values are with respect to digital ground (DGTL GND) with DGTL GND and ANLG GND connected together unless otherwise noted.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	6.3	V
	Analog input voltage (see Note 2)		−0.05		V_{CC} +0.05	V
$V_{REF/2}$	Voltage at REF/2 (see Note 3)		0.25	2.5		V
V_{IH}	High-level input voltage at $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$		2		15	V
V_{IL}	Low-level input voltage at $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$				0.8	V
	Analog ground voltage (see Note 4)		−0.05	0	1	V
f_{clock}	Clock input frequency (see Note 5)		100	640	1460	kHz
	Duty cycle for f_{clock} above 640 kHz (see Note 5)		40%		60%	
$t_{w(CLK)}$	Pulse duration, clock input (high or low) for f_{clock} below 640 kHz		275	781		ns
$t_{w(WR)}$	Pulse duration, $\overline{WR}$ input low		100			ns
T_A	Operating free-air temperature	ADC080_I	−40		85	°C
		ADC080_C	0		70	

NOTES: 2. When the differential input voltage ($V_{I+} - V_{I-}$) is less than or equal to 0 V, the output code is 0000 0000.
3. The internal reference voltage is equal to the voltage applied to REF/2 or approximately equal to one-half of the V_{CC} when REF/2 is left open. The voltage at REF/2 should be one-half the full-scale differential input voltage between the analog inputs. Thus, the differential input voltage range when REF/2 is open and V_{CC} = 5 V is 0 V to 5 V. $V_{REF/2}$ for an input voltage range from 0.5 V to 3.5 V (full-scale differential voltage of 3 V) is 1.5 V.
4. These values are with respect to DGTL GND.
5. Total unadjusted error is guaranteed only at an f_{clock} of 640 kHz with a duty cycle of 40% to 60% (pulse duration 625 ns to 937 ns). For frequencies above this limit or pulse duration below 625 ns, error may increase. The duty cycle limits should be observed for an f_{clock} greater than 640 kHz. Below 640 kHz, this duty cycle limit can be exceeded provided $t_{w(CLK)}$ remains within limits.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V, f_{clock} = 640 kHz, $V_{REF/2}$ = 2.5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	All outputs	V_{CC} = 4.75 V,	I_{OH} = −360 μA	2.4			V
		DB and $\overline{INTR}$	V_{CC} = 4.75 V,	I_{OH} = −10 μA	4.5			
V_{OL}	Low-level output voltage	Data outputs	V_{CC} = 4.75 V,	I_{OL} = 1.6 mA			0.4	V
		$\overline{INTR}$ output	V_{CC} = 4.75 V,	I_{OL} = 1 mA			0.4	
		CLK OUT	V_{CC} = 4.75 V,	I_{OL} = 360 μA			0.4	
V_{T+}	Clock positive-going threshold voltage				2.7	3.1	3.5	V
V_{T-}	Clock negative-going threshold voltage				1.5	1.8	2.1	V
$V_{T+} - V_{T-}$	Clock input hysteresis				0.6	1.3	2	V
I_{IH}	High-level input current					0.005	1	μA
I_{IL}	Low-level input current					−0.005	−1	μA
I_{OZ}	Off-state output current		V_O = 0				−3	μA
			V_O = 5 V				3	
I_{OHS}	Short-current output current	Output high	V_O = 0,	T_A = 25°C	−4.5	−6		mA
I_{OLS}	Short-circuit output current	Output low	V_O = 5 V,	T_A = 25°C	9	16		mA
I_{CC}	Supply current plus reference current		$V_{REF/2}$ = open, $\overline{CS}$ at 5 V	T_A = 25°C,		1.1	1.8	mA
$R_{REF/2}$	Input resistance to reference ladder		See Note 6		2.5	8		kΩ
C_i	Input capacitance (control)					5	7.5	pF
C_o	Output capacitance (DB)					5	7.5	pF

NOTE 6: Resistance is calculated from the current drawn from a 5-volt supply applied to pins 8 and 9.

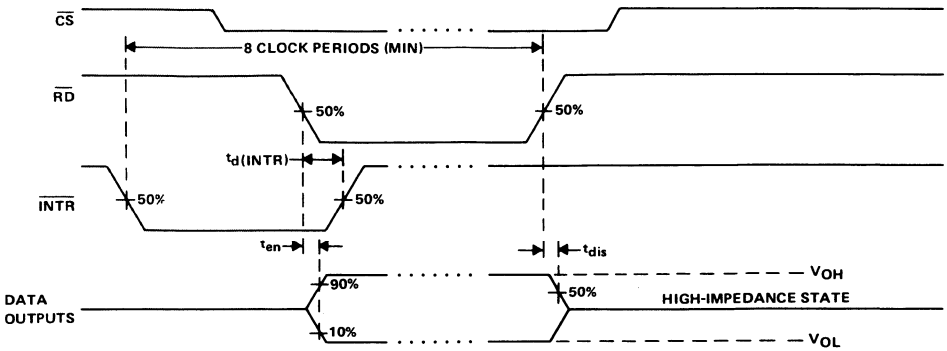
operating characteristics over recommended operating free-air temperature, V_{CC} = 5 V, $V_{REF/2}$ = 2.5 V, f_{clock} = 640 kHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
	Supply-voltage-variation error		V_{CC} = 4.5 V to 5.5 V,	See Note 7		±1/16	±1/8	LSB
	Total adjusted error	ADC0801	With full-scale adjust,	See Notes 7 and 8			±1/4	LSB
		ADC0803					±1/2	
	Total unadjusted error	ADC0802	$V_{REF/2}$ = 2.5 V,	See Notes 7 and 8			±1/2	LSB
		ADC0805	$V_{REF/2}$ open,	See Notes 7 and 8			±1	
	DC common-mode error		See Note 7 and 8			±1/16	±1/8	LSB
t_{en}	Output enable time		C_L = 100 pF			135	200	ns
t_{dis}	Output disable time		C_L = 10 pF,	R_L = 10 kΩ		125	200	ns
$t_{d(INTR)}$	Delay time to reset $\overline{INTR}$					300	450	ns
t_{conv}	Conversion cycle time		f_{clock} = 100 kHz to 1.46 MHz, See Note 9		66		73	clock cycles
CR	Free-running conversion rate		$\overline{INTR}$ connected to $\overline{WR}$, $\overline{CS}$ at 0 V				8770	conv/s

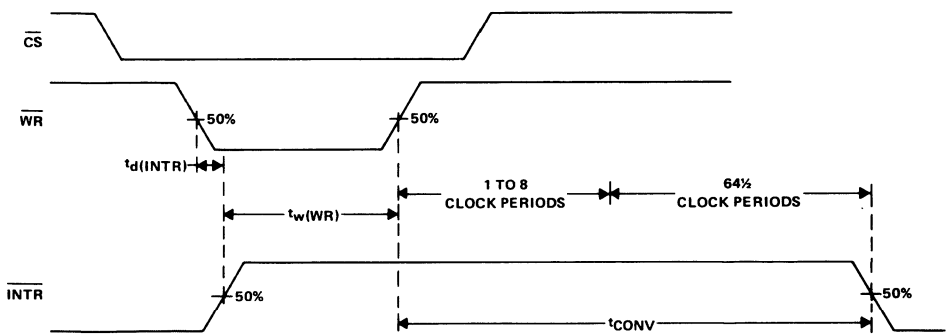
†All typical values are at T_A = 25°C.

NOTES: 7. These parameters are guaranteed over the recommended analog input voltage range.
8. All errors are measured with reference to an ideal straight line through the end-points of the analog-to-digital transfer characteristic.
9. Although internal conversion is completed in 64 clock periods, a $\overline{CS}$ or $\overline{WR}$ low-to-high transition is followed by 1 to 8 clock periods before conversion starts. After conversion is completed, part of another clock period is required before a high-to-low transition of $\overline{INTR}$ completes the cycle.

PARAMETER MEASUREMENT INFORMATION



READ OPERATION TIMING DIAGRAM



WRITE OPERATION TIMING DIAGRAM

PRINCIPLES OF OPERATION

The ADC0801, ADC0802, ADC0803, and ADC0805 each contain a circuit equivalent to a 256-resistor network. Analog switches are sequenced by successive approximation logic to match an analog differential input voltage ($V_{in+} - V_{in-}$) to a corresponding tap on the 256R network. The most-significant bit (MSB) is tested first. After eight comparisons (64 clock periods), an eight-bit binary code (1111 1111 = full scale) is transferred to an output latch and the interrupt ($\overline{INTR}$) output goes low. The device can be operated in a free-running mode by connecting the $\overline{INTR}$ output to the write ($\overline{WR}$) input and holding the conversion start ($\overline{CS}$) input at a low level. To ensure start-up under all conditions, a low-level $\overline{WR}$ input is required during the power-up cycle. Taking $\overline{CS}$ low anytime after that will interrupt a conversion in process.

When the $\overline{WR}$ input goes low, the internal successive approximation register (SAR) and eight-bit shift register are reset. As long as both $\overline{CS}$ and $\overline{WR}$ remain low, the analog-to-digital converter will remain in a reset state. One to eight clock periods after $\overline{CS}$ or $\overline{WR}$ makes a low-to-high transition, conversion starts.

When the $\overline{CS}$ and $\overline{WR}$ inputs are low, the start flip-flop is set and the interrupt flip-flop and eight-bit register are reset. The next clock pulse transfers a logic high to the output of the start flip-flop. The logic high is ANDed with the next clock pulse placing a logic high on the reset input of the start flip-flop. If either $\overline{CS}$ or $\overline{WR}$ have gone high, the set signal to the start flip-flop is removed causing it to be reset. A logic high is placed on the D input of the eight-bit shift register and the conversion process is started. If the $\overline{CS}$ and $\overline{WR}$ inputs are still low, the start flip-flop, the eight-bit shift register, and the SAR remain reset. This action allows for wide $\overline{CS}$ and $\overline{WR}$ inputs with conversion starting from one to eight clock periods after one of the inputs goes high.

When the logic high input has been clocked through the eight-bit shift register, completing the SAR search, it is applied to an AND gate controlling the output latches and to the D input of a flip-flop. On the next clock pulse, the digital word is transferred to the three-state output latches and the interrupt flip-flop is set. The output of the interrupt flip-flop is inverted to provide an $\overline{INTR}$ output that is high during conversion and low when the conversion is completed.

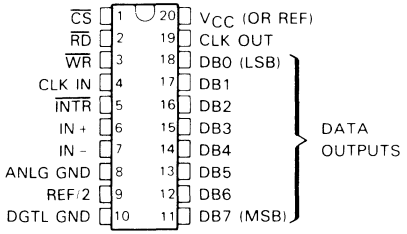
When a low is at both the $\overline{CS}$ and $\overline{RD}$ inputs, an output is applied to the DB0 through DB7 outputs and the interrupt flip-flop is reset. When either the $\overline{CS}$ or $\overline{RD}$ inputs return to a high state, the DB0 through DB7 outputs are disabled (returned to the high-impedance state). The interrupt flip-flop remains reset.

TYPE ADC0804C
8-BIT ANALOG-TO-DIGITAL CONVERTER WITH DIFFERENTIAL INPUTS

D2755, OCTOBER 1983

- 8-Bit Resolution
- Ratiometric Conversion
- 100 μs Conversion Time
- 135 ns Access Time
- No Zero Adjust Requirement
- On-Chip Clock Generator
- Single 5-Volt Power Supply
- Operates With Microprocessor or as Stand-Alone
- Designed to be Interchangeable with National Semiconductor ADC0804LCN

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



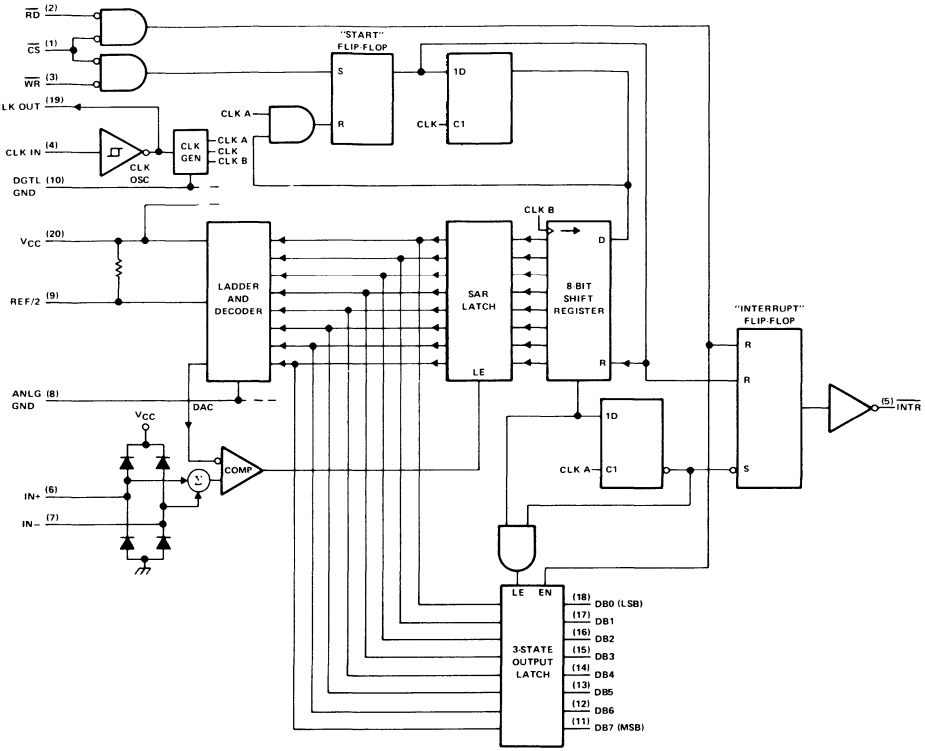
description

The ADC0804C is a CMOS 8-bit successive-approximation analog-to-digital converter that uses a modified potentiometric (256R) ladder. The ADC0804 is designed to operate from common microprocessor control buses, with the three-state output latches driving the data bus. The ADC0804 can be made to appear to the microprocessor as a memory location or an I/O port.

A differential analog voltage input allows increased common-mode rejection and offset of the zero-input analog voltage value. Although a reference input (REF/2) is available to allow 8-bit conversion over smaller analog voltage spans or to make use of an external reference, ratiometric conversion is possible with the REF/2 input open. Without an external reference, the conversion takes place over a span from V_{CC} to analog ground (ANLG GND). The ADC0804 can operate with an external clock signal or, with an additional resistor and capacitor, can operate using an on-chip clock generator.

The ADC0804C is characterized for operation from 0°C to 70°C.

functional block diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ . . . . . −0.3 V to 18 V
other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} + 0.3 V
Continuous total power dissipation at 25°C free-air temperature (see Note 2) . . . . . 875 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to digital ground (DGTL GND) with DGTL GND and ANLG GND connected together (unless otherwise noted).
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	6.3	V
$V_{REF/2}$	Voltage at REF/2 (see Note 3)	0.25	2.5		V
V_{IH}	High-level input voltage at $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$	2		15	V
V_{IL}	Low-level input voltage at $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$			0.8	V
	Analog ground voltage (see Note 4)	−0.05	0	1	V
	Analog input voltage (see Note 5)	GND − 0.05		V_{CC} + 0.05	V
f_{clock}	Clock input frequency (see Note 6)	100	640	1460	kHz
	Duty cycle above 640 kHz (see Note 6)	40		60	%
$t_{w(CLK)}$	Pulse duration clock input (high or low) (see Note 6)	275	781		ns
$t_{w(WR)}$	Pulse duration, $\overline{WR}$ input low	100			ns
T_A	Operating free-air temperature	0		70	°C

NOTES: 3. Proper operation is achieved over a differential input range of 0 V to V_{CC} when the REF 2 input is open.
4. These values are with respect to digital ground (pin 10).
5. When the positive analog input with respect to the negative analog input (V_{in+} − V_{in-}) is zero or negative, the output code is 0000 0000.
6. Total unadjusted error is guaranteed only at an f_{clock} of 640 kHz this with a duty cycle of 40% to 60% (pulse duration 625 ns to 937 ns). For frequencies above this limit or pulse duration below 625 ns, error may increase. The duty cycle limits should be observed for an f_{clock} greater than 640 kHz. Below 640 kHz, this duty cycle limit can be exceeded provided $t_{w(CLK)}$ remains within limits.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V, f_{clock} = 640 kHz, REF/2 = 2.5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	All outputs	V_{CC} = 4.75 V, I_{OH} = −360 μA	2.4			V
		DB and $\overline{INTR}$	V_{CC} = 4.75 V, I_{OH} = −10 μA	4.5			
V_{OL}	Low-level output voltage	Data outputs	V_{CC} = 4.75 V, I_{OL} = 1.6 mA			0.4	V
		$\overline{INTR}$ output	V_{CC} = 4.75 V, I_{OL} = 1 mA			0.4	
		CLK OUT	V_{CC} = 4.75 V, I_{OL} = 360 μA			0.4	
V_{T+}	Clock positive-going threshold voltage			2.7	3.1	3.5	V
V_{T-}	Clock negative-going threshold voltage			1.5	1.8	2.1	V
$V_{T+} - V_{T-}$	Clock input hysteresis			0.6	1.3	2	V
I_{IH}	High-level input current				0.005	1	μA
I_{IL}	Low-level input current				−0.005	−1	μA
I_{OZ}	Off-state output current		V_O = 0			−3	μA
			V_O = 5 V			3	
I_{OHS}	Short-circuit output current	Output high	V_O = 0, T_A = 25°C	−4.5	−6		mA
I_{OLS}	Short-circuit output current	Output low	V_O = 5 V, T_A = 25°C	9	16		mA
I_{CC}	Supply current plus reference current		REF/2 open, $\overline{CS}$ at 5 V, T_A = 25°C		1.9	2.5	mA
$R_{REF/2}$	Input resistance to reference ladder		See Note 7	1	1.3		kΩ
C_i	Input capacitance (control)				5	7.5	pF
C_o	Output capacitance (DB)				5	7.5	pF

†All typical values are at T_A = 25°C.

NOTE 7: The resistance is calculated from the current drawn from a 5-volt supply applied to pins 8 and 9.

operating characteristics over recommended operating free-air temperature, V_{CC} = 5 V, $V_{REF/2}$ = 2.5 V, f_{clock} = 640 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Supply-voltage-variation error	V_{CC} = 4.5 V to 5.5 V, See Note 8		±1/16	±1/8	LSB
	Total unadjusted error	See Notes 8 and 9			±1	LSB
	DC common-mode error	See Note 9		±1/16	±1/8	LSB
t_{en}	Output enable time	C_L = 100 pF		135	200	ns
t_{dis}	Output disable time	C_L = 10 pF, R_L = 10 kΩ		125	200	ns
$t_{d(INTR)}$	Delay time to reset $\overline{INTR}$			300	450	ns
t_{conv}	Conversion cycle time	f_{clock} = 100 kHz to 1.46 MHz, See Note 10	66		73	clock cycles
CR	Free-running conversion rate	$\overline{INTR}$ connected to $\overline{WR}$, $\overline{CS}$ at 0 V			8770	conv/s

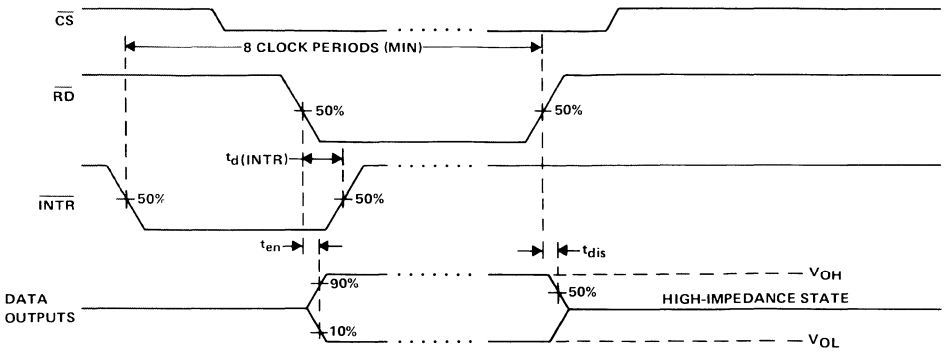
†All typical values are at T_A = 25°C.

NOTES: 8. These parameters are guaranteed over the recommended analog input voltage range.

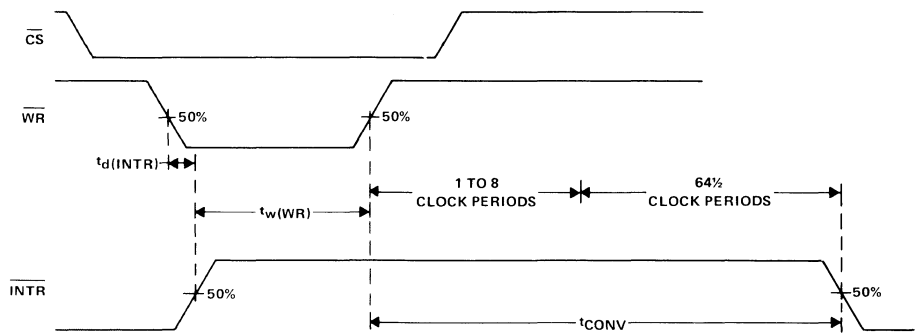
9. All errors are measured with reference to an ideal straight line through the end-points of the analog-to-digital transfer characteristic.

10. Although internal conversion is completed in 64 clock periods, a $\overline{CS}$ or $\overline{WR}$ low-to-high transition is followed by 1 to 8 clock periods before conversion starts. After conversion is completed, part of another clock period is required before a high-to-low transition of $\overline{INTR}$ completes the cycle.

timing diagrams



READ OPERATION TIMING DIAGRAM



WRITE OPERATION TIMING DIAGRAM

PRINCIPLES OF OPERATION

The ADC0804 contains a circuit equivalent to a 256-resistor network. Analog switches are sequenced by successive approximation logic to match an analog differential input voltage ($V_{in+} - V_{in-}$) to a corresponding tap on the 256-resistor network. The most-significant bit (MSB) is tested first. After eight comparisons (64 clock periods), an eight-bit binary code (1111 1111 = full scale) is transferred to an output latch and the interrupt ($\overline{INTR}$) output goes low. The device can be operated in a free-running mode by connecting the $\overline{INTR}$ output to the write ($\overline{WR}$) input and holding the conversion start ($\overline{CS}$) input at a low level. To ensure start-up under all conditions, a low-level $\overline{WR}$ input is required during the power-up cycle. Taking $\overline{CS}$ low anytime after that will interrupt a conversion in process.

When the $\overline{WR}$ input goes low, the ADC0804 successive approximation register (SAR) and eight-bit shift register are reset. As long as both $\overline{CS}$ and $\overline{WR}$ remain low, the ADC0804C will remain in a reset state. One to eight clock periods after $\overline{CS}$ or $\overline{WR}$ makes a low-to-high transition, conversion starts.

When the $\overline{CS}$ and $\overline{WR}$ inputs are low, the start flip-flop is set and the interrupt flip-flop and eight-bit register are reset. The next clock pulse transfers a logic high to the output of the start flip-flop. The logic high is ANDed with the next clock pulse placing a logic high on the reset input of the start flip-flop. If either $\overline{CS}$ or $\overline{WR}$ have gone high, the set signal to the start flip-flop is removed causing it to be reset. A logic high is placed on the D input of the eight-bit shift register and the conversion process is started. If the $\overline{CS}$ and $\overline{WR}$ inputs are still low, the start flip-flop, the eight-bit shift register, and the SAR remain reset. This action allows for wide $\overline{CS}$ and $\overline{WR}$ inputs with conversion starting from one to eight clock periods after one of the inputs goes high.

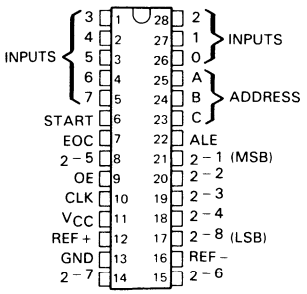
When the logic high input has been clocked through the eight-bit shift register, completing the SAR search, it is applied to an AND gate controlling the output latches and to the D input of a flip-flop. On the next clock pulse, the digital word is transferred to the three-state output latches and the interrupt flip-flop is set. The output of the interrupt flip-flop is inverted to provide an $\overline{INTR}$ output that is high during conversion and low when the conversion is completed.

When a low is at both the $\overline{CS}$ and $\overline{RD}$ inputs, an output is applied to the DB0 through DB7 outputs and the interrupt flip-flop is reset. When either the $\overline{CS}$ or $\overline{RD}$ inputs return to a high state, the DB0 through DB7 outputs are disabled (returned to the high-impedance state). The interrupt flip-flop remains reset.

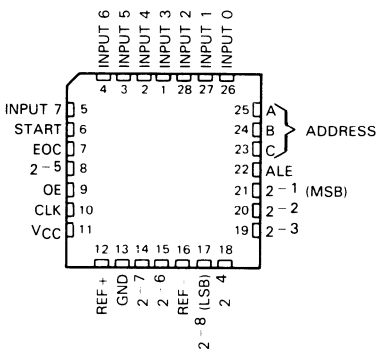
D2642, JUNE 1981—REVISED FEBRUARY 1986

- **Total Unadjusted Error . . . ±0.75 LSB Max for ADC0808 and ±1.25 LSB Max for ADC0809**
- **Resolution of 8 Bits**
- **100 μs Conversion Time**
- **Ratiometric Conversion**
- **Guaranteed Monotonicity**
- **No Missing Codes**
- **Easy Interface with Microprocessors**
- **Latched 3-State Outputs**
- **Latched Address Inputs**
- **Single 5-Volt Supply**
- **Low Power Consumption**
- **Designed to be Interchangeable with National Semiconductor ADC0808, ADC0809**

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



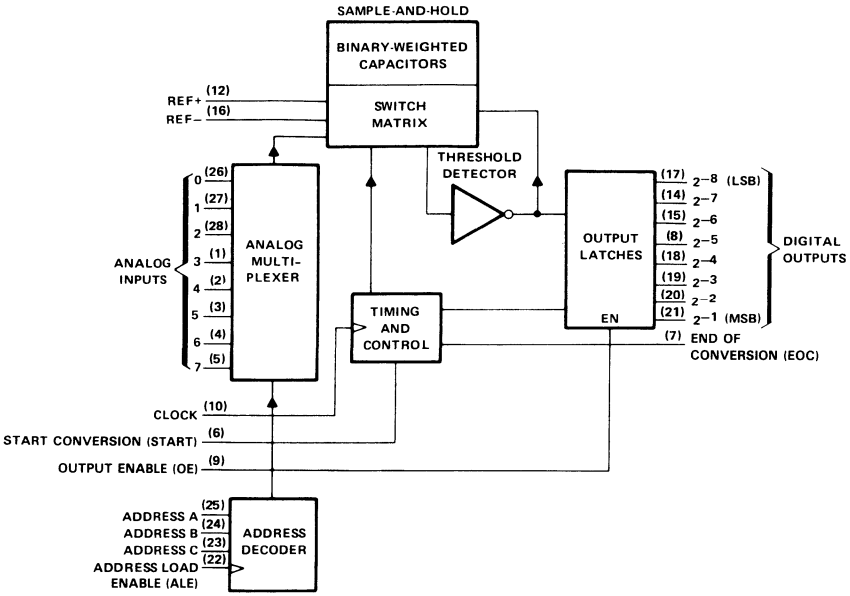
description

The ADC0808 and ADC0809 are monolithic CMOS devices with an 8-channel multiplexer, an 8-bit analog-to-digital (A/D) converter, and microprocessor-compatible control logic. The 8-channel multiplexer can be controlled by a microprocessor through a 3-bit address decoder with address load to select any one of eight single-ended analog switches connected directly to the comparator. The 8-bit A/D converter uses the successive-approximation conversion technique featuring a high-impedance threshold detector, a switched-capacitor array, a sample-and-hold, and a successive-approximation register (SAR). Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The comparison and converting methods used eliminate the possibility of missing codes, nonmonotonicity, and the need for zero or full-scale adjustment. Also featured are latched 3-state outputs from the SAR and latched inputs to the multiplexer address decoder. The single 5-volt supply and low power requirements make the ADC0808 and ADC0809 especially useful for a wide variety of applications. Ratiometric conversion is made possible by access to the reference voltage input terminals.

The ADC0808 and ADC0809 are characterized for operation from −40°C to 85°C.

functional block diagram (positive logic)

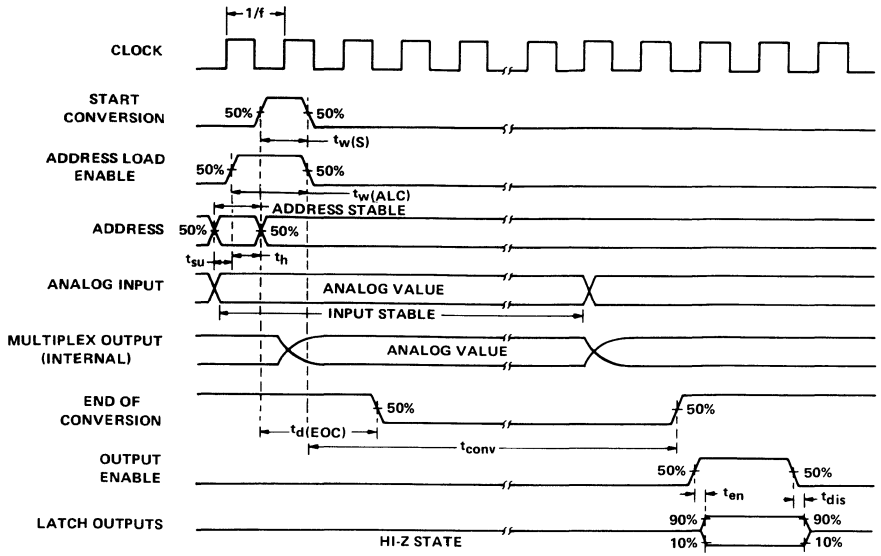


MULTIPLEXER FUNCTION TABLE

INPUTS				SELECTED
ADDRESS			ADDRESS	ANALOG
C	B	A	STROBE	CHANNEL
L	L	L	↑	0
L	L	H	↑	1
L	H	L	↑	2
L	H	H	↑	3
H	L	L	↑	4
H	L	H	↑	5
H	H	L	↑	6
H	H	H	↑	7

H = high level, L = low level
↑ = low-to-high transition

operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: control inputs . . . . . −0.3 to 15 V
all other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	6	V
Positive reference voltage, V_{ref+} (see Note 2)		V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{ref-}		0	−0.1	V
Differential reference voltage, $V_{ref+} - V_{ref-}$		5		V
High-level input voltage, V_{IH}	$V_{CC}-1.5$			V
Low-level input voltage, V_{IL}			1.5	V
Start pulse duration, $t_{w(S)}$	200			ns
Address load control pulse duration, $t_{w(ALC)}$	200			ns
Address setup time, t_{su}	50			ns
Address hold time, t_h	50			ns
Clock frequency, f_{clock}	10	640	1280	kHz
Operating free-air temperature, T_A	−40		85	°C

NOTE 2: Care must be taken that this rating is observed even during power-up.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 4.75 V to 5.25 V (unless otherwise noted)

total device

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_O = −360 μA	V_{CC} − 0.4			V
V_{OL}	Low-level output voltage	Data outputs	I_O = 1.6 mA			0.45	V
		End of conversion	I_O = 1.2 mA			0.45	
I_{OZ}	Off-state (high-impedance-state) output current		V_O = V_{CC}			3	μA
			V_O = 0			−3	
I_I	Control input current at maximum input voltage		V_I = 15 V			1	μA
I_{IL}	Low-level control input current		V_I = 0			−1	μA
I_{CC}	Supply current		f_{clock} = 640 kHz		0.3	3	mA
C_i	Input capacitance, control inputs		T_A = 25°C		10	15	pF
C_o	Output capacitance, data outputs		T_A = 25°C		10	15	pF
	Resistance from pin 12 to pin 16				1000		kΩ

analog multiplexer

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{on}	Channel on-state current (see Note 3)	V_I = 5 V,	f_{clock} = 640 kHz			2	μA
		V_I = 0,	f_{clock} = 640 kHz			−2	
I_{off}	Channel off-state current	V_{CC} = 5 V, T_A = 25°C	V_I = 5 V		10	200	nA
			V_I = 0		−10	−200	
		V_{CC} = 5 V	V_I = 5 V			1	μA
			V_I = 0			−1	

†Typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTE 3: Channel on-state current is primarily due to the bias current into or out of the threshold detector, and it varies directly with clock frequency.

operating characteristics, T_A = 25°C, V_{CC} = V_{REF+} = 5 V, V_{REF-} = 0 V, f_{clock} = 640 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADC0808			ADC0809			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
k_{SVS}	Supply voltage sensitivity	V_{CC} = V_{ref+} = 4.75 V to 5.25 V, T_A = −40°C to 85°C, See Note 4		±0.05			±0.05		%/V
	Linearity error (see Note 5)			±0.25			±0.5		LSB
	Zero error (see Note 6)			±0.25			±0.25		LSB
	Total unadjusted error (See Note 7)	T_A = 25°C		±0.25	±0.5		±0.5		LSB
		T_A = −40°C to 85°C			±0.75			±1.25	
		T_A = 0°C to 70°C						±1	
t_{en}	Output enable time	C_L = 50 pF, R_L = 10 kΩ		80	250		80	250	ns
t_{dis}	Output disable time	C_L = 10 pF, R_L = 10 kΩ		105	250		105	250	ns
t_{conv}	Conversion time	See Note 8	90	100	116	90	100	116	μs
$t_{d(EOC)}$	Delay time, end of conversion output	See Notes 8 and 9	0		14.5	0		14.5	μs

†Typical values for all except supply voltage sensitivity are at V_{CC} = 5 V, and all are at T_A = 25°C.

NOTES:
4. Supply voltage sensitivity relates to the ability of an analog-to-digital converter to maintain accuracy as the supply voltage varies. The supply and V_{ref+} are varied together and the change in accuracy is measured with respect to full-scale.
5. Linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic.
6. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error is the maximum sum of linearity error, zero error, and full-scale error.
8. Refer to the operating sequence diagram.
9. For clock frequencies other than 640 kHz, $t_{d(EOC)}$ maximum is 8 clock periods plus 2 μs.

PRINCIPLES OF OPERATION

The ADC0808 and ADC0809 each consists of an analog signal multiplexer, an 8-bit successive-approximation converter, and related control and output circuitry.

multiplexer

The analog multiplexer selects 1 of 8 single-ended input channels as determined by the address decoder. Address load control loads the address code into the decoder on a low-to-high transition. The output latch is reset by the positive-going edge of the start pulse. Sampling also starts with the positive-going edge of the start pulse and lasts for 32 clock periods. The conversion process may be interrupted by a new start pulse before the end of 64 clock periods. The previous data will be lost if a new start of conversion occurs before the 64th clock pulse. Continuous conversion may be accomplished by connecting the End-of-Conversion output to the start input. If used in this mode an external pulse should be applied after power up to assure start up.

converter

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (Figure 1). In the first phase of the conversion process, the analog input is sampled by closing switch S_C and all S_T switches, and by simultaneously charging all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all 8 bits are identified, and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 128). Node 128 of this capacitor is switched to the reference voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF−. If the voltage at the summing node is greater than the trip-point of the threshold detector (approximately one-half the V_{CC} voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to REF−. If the voltage at the summing node is less than the trip point of the threshold detector, this 128-weight capacitor remains connected to REF+ through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, the 32-weight capacitor, and so forth down the line, until all bits are counted.

With each step of the capacitor-sampling process, the initial charge is redistributed among the capacitors. The conversion process is successive approximation, but relies on charge redistribution rather than a successive-approximation register (and reference DAC) to count and weigh the bits from MSB to LSB.

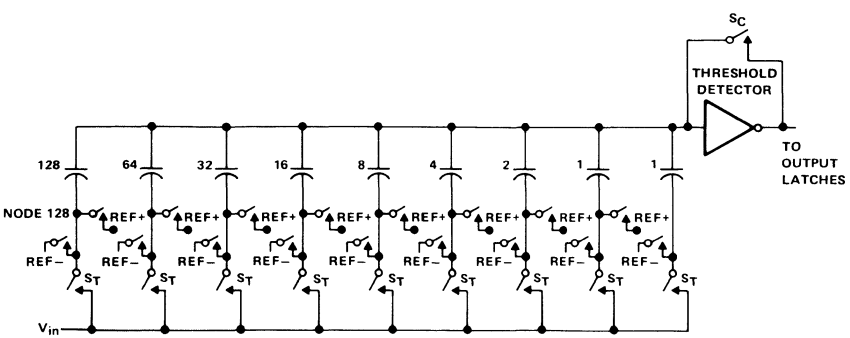
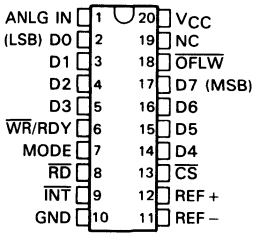


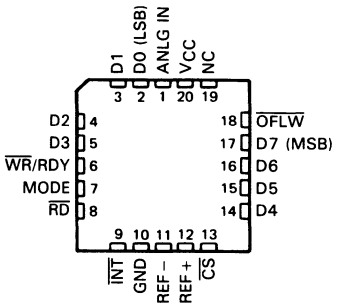
FIGURE 1. SIMPLIFIED MODEL OF THE SUCCESSIVE-APPROXIMATION SYSTEM

- **Advanced LinCMOS™ Silicon-Gate Technology**
- **8-Bit Resolution**
- **Differential Reference Inputs**
- **Parallel Microprocessor Interface**
- **Conversion and Access Time Over Temperature Range**
  Write-Read Mode . . . 1.18 μs and 1.92 μs
  Read Mode . . . 2.5 μs Max
- **No External Clock or Oscillator Components Required**
- **On-Chip Track-and-Hold**
- **Low Power Consumption . . . 50 mW Typ**
- **Single 5-V Supply**
- **TLC0820B is Direct Replacement for National Semiconductor ADC0820B/BC and Analog Devices AD7820L/C/U; TLC0820A is Direct Replacement for National Semiconductor ADC0820C/CC and Analog Devices AD7820K/B/T**

ALL TYPES . . . DW OR N PACKAGE
TLC0820_M . . . J PACKAGE
(TOP VIEW)



TLC0820_M . . . FK PACKAGE
ADC0820_CI, ADC0820_C . . . FN PACKAGE
TLC0820_I, TLC0820_C . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The ADC0820B, ADC0820C, TLC0820A, and TLC0820B are Advanced LinCMOS™ 8-bit analog-to-digital converters each consisting of two 4-bit "flash" converters, a 4-bit digital-to-analog converter, a summing (error) amplifier, control logic, and a result latch circuit. The modified "flash" technique allows low-power integrated circuitry to complete an 8-bit conversion in 1.18 μs over temperature. The on-chip track-and-hold circuit has a 100-ns sample window and allows these devices to convert continuous analog signals having slew rates of up to 100 mV/μs without external sampling components. TTL-compatible three-state output drivers and two modes of operation allow interfacing to a variety of microprocessors. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The C-suffix devices are characterized for operation from 0°C to 70°C. See Available Options.

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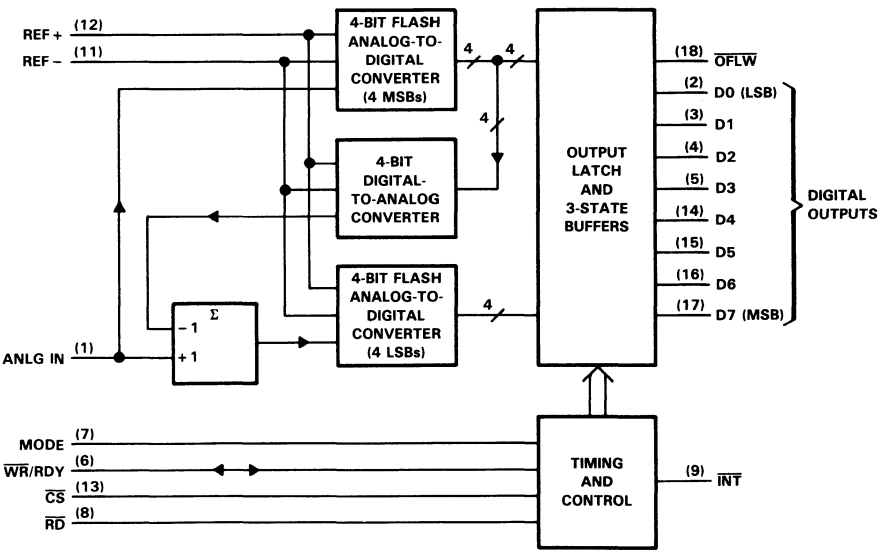
AVAILABLE OPTIONS

SYMBOLIZATION†		OPERATING TEMPERATURE RANGE	TOTAL UNADJUSTED ERROR
DEVICE	PACKAGE SUFFIX		
ADC0820BC	DW, FN, N	0°C to 70°C	±0.5 LSB
ADC0820BCI	DW, FN, N	−40°C to 85°C	±0.5 LSB
ADC0820CC	DW, FN, N	0°C to 70°C	±1 LSB
ADC0820CCI	DW, FN, N	−40°C to 85°C	±1 LSB
TLC0820AC	DW, FN, N	0°C to 70°C	±1 LSB
TLC0820AI	DW, FN, N	−40°C to 85°C	±1 LSB
TLC0820AM	DW, FK, J, N	−55°C to 125°C	±1 LSB
TLC0820BC	DW, FN, N	0°C to 70°C	±0.5 LSB
TLC0820BI	DW, FN, N	−40°C to 85°C	±0.5 LSB
TLC0820BM	DW, FK, J, N	−55°C to 125°C	±0.5 LSB

†In many instances, these ICs may have both ADC0820 and TLC0820 labeling on the package.

functional block diagram



PIN NAME	PIN NUMBER	DESCRIPTION
ANLG IN	1	Analog input
$\overline{CS}$	13	This input must be low in order for $\overline{RD}$ or $\overline{WR}$ to be recognized by the ADC.
D0	2	Three-state data output, bit 1 (LSB)
D1	3	Three-state data output, bit 2
D2	4	Three-state data output, bit 3
D3	5	Three-state data output, bit 4
D4	14	Three-state data output, bit 5
D5	15	Three-state data output, bit 6
D6	16	Three-state data output, bit 7
D7	17	Three-state data output, bit 8 (MSB)
GND	10	Ground
$\overline{INT}$	9	In the WRITE-READ mode, the interrupt output, $\overline{INT}$, going low indicates that the internal count-down delay time, $t_{d(int)}$, is complete and the data result is in the output latch. $t_{d(int)}$ is typically 800 ns starting after the rising edge of the $\overline{WR}$ input (see operating characteristics and Figure 3). If $\overline{RD}$ goes low prior to the end of $t_{d(int)}$, $\overline{INT}$ goes low at the end of t_{dRIL} and the conversion results are available sooner (see Figure 2). $\overline{INT}$ is reset by the rising edge of either $\overline{RD}$ or $\overline{CS}$.
MODE	7	Mode-selection input. It is internally tied to GND through a 50-μA current source, which acts like a pull-down resistor. READ mode: Occurs when this input is low. WRITE-READ mode: Occurs when this input is high.
NC	19	No internal connection
$\overline{OFLW}$	18	Normally the $\overline{OFLW}$ output is a logical high. However, if the analog input is higher than the V_{REF+}, $\overline{OFLW}$ will be low at the end of conversion. It can be used to cascade 2 or more devices to improve resolution (9 or 10-bits).
$\overline{RD}$	8	In the WRITE-READ mode with $\overline{CS}$ low, the 3-state data outputs D0 through D7 are activated when $\overline{RD}$ goes low. $\overline{RD}$ can also be used to increase the conversion speed by reading data prior to the end of the internal count-down delay time. As a result, the data transferred to the output latch is latched after the falling edge of $\overline{RD}$. In the READ mode with $\overline{CS}$ low, the conversion starts with $\overline{RD}$ going low. $\overline{RD}$ also enables the three-state data outputs upon completion of the conversion. The RDY output going into the high-impedance state and $\overline{INT}$ going low indicates completion of the conversion.
REF−	11	This input voltage is placed on the bottom of the resistor ladder.
REF+	12	This input voltage is placed on the top of the resistor ladder.
V_{CC}	20	Power supply voltage
$\overline{WR}$/RDY	6	In the WRITE-READ mode with $\overline{CS}$ low, the conversion is started on the falling edge of the $\overline{WR}$ input signal. The result of the conversion is strobed into the output latch after the internal count-down delay time, $t_{d(int)}$, provided that the $\overline{RD}$ input does not go low prior to this time. $t_{d(int)}$ is approximately 800 ns. In the READ mode, RDY (an open-drain output) will go low after the falling edge of $\overline{CS}$, and will go into the high-impedance state when the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TLC0820_M	ADC0820_CI TLC0820_I	ADC0820_C TLC0820_C	UNIT
Supply voltage, V_{CC} (see Note 1)	10	10	10	V
Input voltage range, all inputs (see Note 1)	−0.2 to V_{CC}+0.2	−0.2 to V_{CC}+0.2	−0.2 to V_{CC}+0.2	V
Output voltage range, all outputs (see Note 1)	−0.2 to V_{CC}+0.2	−0.2 to V_{CC}+0.2	−0.2 to V_{CC}+0.2	V
Operating free-air temperature range	−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package	260			°C
Case temperature for 10 seconds: FN package		260	260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300			°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package	260	260	260	°C

NOTE 1: All voltages are with respect to network ground terminal, pin 10.

recommended operating conditions

			TLC0820_M			ADC0820_CI TLC0820_I			ADC0820_C TLC0820_C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	8	4.5	5	8	4.5	5	8	V
Analog input voltage			−0.1		V_{CC}+0.1	−0.1		V_{CC}+0.1	−0.1		V_{CC}+0.1	V
Positive reference voltage, V_{REF+}			V_{REF-}		V_{CC}	V_{REF-}		V_{CC}	V_{REF-}		V_{CC}	V
Negative reference voltage, V_{REF-}			GND		V_{REF+}	GND		V_{REF+}	GND		V_{REF+}	V
High-level input voltage, V_{IH}	V_{CC} = 4.75 V to 5.25 V	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$	2			2			2			V
		MODE	3.5			3.5			3.5			
Low-level input voltage, V_{IL}	V_{CC} = 4.75 V to 5.25 V	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$			0.8			0.8			0.8	V
		MODE			1.5			1.5			1.5	
Delay to next conversion, $t_{d(NC)}$ (see Figures 1, 2, 3, and 4)			500			500			500			ns
Delay time from $\overline{WR}$ to $\overline{RD}$ in write-read mode, t_{dWR} (see Figure 2)			0.4			0.4			0.4			μs
Write-pulse duration in write-read mode, t_{wW} (see Figures 2, 3, and 4)			0.5		50	0.5		50	0.5		50	μs
Operating free-air temperature, T_A			−55		125	−40		85	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Any D, $\overline{INT}$, or $\overline{OFLW}$	V_{CC} = 4.75 V, I_{OH} = −360 μA	Full range	2.4			V
			V_{CC} = 4.75 V, I_{OH} = −10 μA	Full range	4.5			
				25°C	4.6			
V_{OL}	Low-level output voltage	Any D, $\overline{OFLW}$, $\overline{INT}$, or $\overline{WR}$/RDY	V_{CC} = 5.25 V, I_{OL} = 1.6 mA	Full range			0.4	V
				25°C			0.34	
I_{IH}	High-level input current	$\overline{CS}$ or $\overline{RD}$	V_{IH} = 5 V	Full range		0.005	1	μA
		$\overline{WR}$/RDY		Full range			3	
				25°C		0.1	0.3	
		MODE		Full range			200	
				25°C		50	170	
I_{IL}	Low-level input current	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$, or MODE	V_{IL} = 0	Full range		−0.005	−1	μA
I_{OZ}	Off-state (high-impedance state) output current	Any D or $\overline{WR}$/RDY	V_O = 5 V	Full range			3	μA
				25°C		0.1	0.3	
			V_O = 0	Full range			−3	
				25°C		−0.1	−0.3	
I_I	Analog input current		$\overline{CS}$ at 5 V, V_I = 5 V	Full range			3	μA
				25°C			0.3	
			$\overline{CS}$ at 5 V, V_I = 0	Full range			−3	
				25°C			−0.3	
I_{OS}	Short-circuit output current	Any D, $\overline{OFLW}$, $\overline{INT}$, or $\overline{WR}$/RDY	V_O = 5 V	Full range	7			mA
				25°C	8.4	14		
		Any D or $\overline{OFLW}$	V_O = 0	Full range	−6			
				25°C	−7.2	−12		
		$\overline{INT}$		Full range	−4.5			
				25°C	−5.3	−9		
R_{ref}	Reference resistance			Full range	1.25		6	kΩ
				25°C	1.4	2.3	5.3	
I_{CC}	Supply current		$\overline{CS}$, $\overline{WR}$/RDY, and $\overline{RD}$ at 0 V	Full range			15	mA
				25°C		7.5	13	
C_i	Input capacitance	Any digital		Full range		5		pF
		ANLG IN				45		
C_o	Output capacitance	Any digital		Full range			5	pF

†All typical values are at T_A = 25°C.

operating characteristics, V_{CC} = 5 V, V_{REF+} = 5 V, V_{REF-} = 0, $t_r = t_f$ = 20 ns, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		ADC0820B TLC0820B			ADC0820C TLC0820A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
k_{SVS}	Supply voltage sensitivity	V_{CC} = 5 V ± 5%, T_A = MIN to MAX			±1/16	±1/4		±1/16	±1/4	LSB
	Total unadjusted error†	MODE pin at 0 V, T_A = MIN to MAX				1/2			1	LSB
t_{convR}	Read mode conversion time	MODE pin at 0 V, See Figure 1			1.6	2.5		1.6	2.5	μs
$t_{d(int)}$	Internal count-down delay time	MODE pin at 5 V, See Figures 3 and 4	C_L = 50 pF,		800	1300		800	1300	ns
t_{aR}	Access time from $\overline{RD}$↓	MODE pin at 0 V, See Figure 1			t_{convR} +20	t_{convR} +50		t_{convR} +20	t_{convR} +50	ns
t_{aR1}	Access time from $\overline{RD}$↓	MODE pin at 5 V, $t_{dWR} < t_{d(int)}$, See Figure 2	C_L = 15 pF		190	280		190	280	ns
			C_L = 100 pF		210	320		210	320	
t_{aR2}	Access time from $\overline{RD}$↓	MODE pin at 5 V, $t_{dWR} > t_{d(int)}$ See Figure 3	C_L = 15 pF		70	120		70	120	ns
			C_L = 100 pF		90	150		90	150	
t_{aINT}	Access time from $\overline{INT}$↓	MODE pin at 5 V, See Figure 4			20	50		20	50	ns
t_{dis}	Disable time from $\overline{RD}$↑	R_L = 1 kΩ, See Figures 1, 2, 3, and 5	C_L = 10 pF,		70	95		70	95	ns
t_{dRDY}	Delay time from $\overline{CS}$↓ to RDY↓	MODE pin at 0 V, See Figure 1	C_L = 50 pF,		50	100		50	100	ns
t_{dRIH}	Delay time from $\overline{RD}$↑ to $\overline{INT}$↑	C_L = 50 pF, See Figures 1, 2, and 3			125	225		125	225	ns
t_{dRIL}	Delay time from $\overline{RD}$↓ to $\overline{INT}$↓	MODE pin at 5 V, See Figure 2	$t_{dWR} < t_{d(int)}$,		200	290		200	290	ns
t_{dWIH}	Delay time from $\overline{WR}$↑ to $\overline{INT}$↑	MODE pin at 5 V, See Figure 4	C_L = 50 pF,		175	270		175	270	ns
	Slew rate tracking				0.1			0.1		V/μs

† Total unadjusted error includes offset, full-scale, and linearity errors.

PARAMETER MEASUREMENT INFORMATION

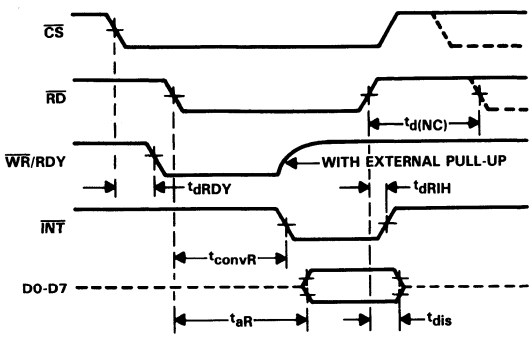


FIGURE 1. READ MODE WAVEFORMS (MODE PIN LOW)

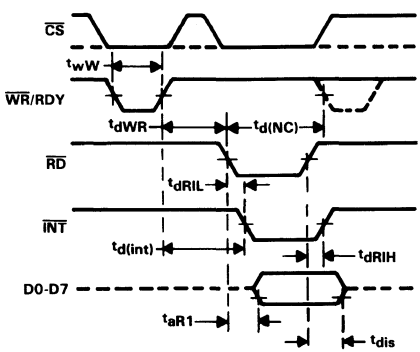


FIGURE 2. WRITE-READ MODE WAVEFORMS [MODE PIN HIGH AND $t_{dWR} < t_{d(int)}$]

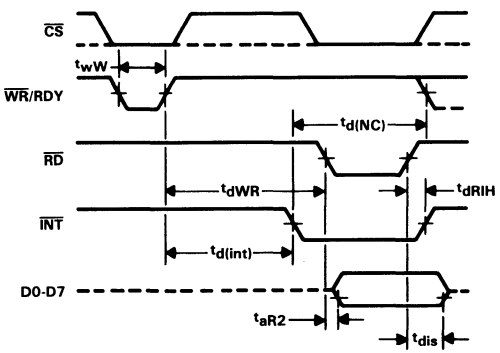


FIGURE 3. WRITE-READ WAVEFORMS [MODE PIN HIGH AND $t_{dWR} > t_{d(int)}$]

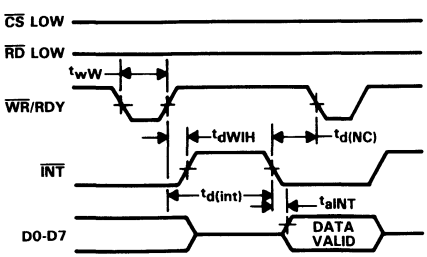


FIGURE 4. WRITE-READ MODE WAVEFORMS
(STAND-ALONE OPERATION, MODE PIN HIGH, AND RD LOW)

PARAMETER MEASUREMENT INFORMATION

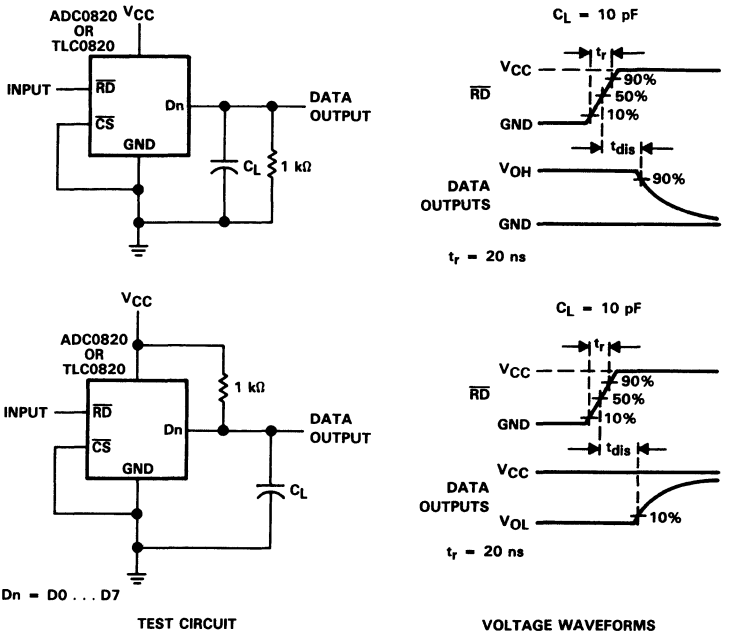


FIGURE 5. TEST CIRCUIT AND VOLTAGE WAVEFORMS

PRINCIPLES OF OPERATION

The ADC0820B, ADC0820C, TLC0820A, and TLC0820B each employ a combination of "sampled-data" comparator techniques and "flash" techniques common to many high-speed converters. Two 4-bit "flash" analog-to-digital conversions are used to give a full 8-bit output.

The recommended analog input voltage range for conversion is -0.1 V to $V_{CC}+0.1$ V. Analog input signals that are less than V_{REF-} + ½ LSB or greater than V_{REF+} − ½ LSB convert to 00000000 or 11111111 respectively. The reference inputs are fully differential with common-mode limits defined by the supply rails. The reference input values define the full-scale range of the analog input. This allows the gain of the ADC to be varied for ratiometric conversion by changing the V_{REF+} and V_{REF-} voltages.

The device operates in two modes, read (only) and write-read, which are selected by the MODE pin (pin 7). The converter is set to the read (only) mode when pin 7 is low. In the read mode, the $\overline{WR}$/RDY pin is used as an output and is referred to as the "ready" pin. In this mode, a low on the "ready" pin while $\overline{CS}$ is low indicates that the device is busy. Conversion starts on the falling edge of $\overline{RD}$ and is completed no more than 2.5 μs later when $\overline{INT}$ falls and the "ready" pin returns to a high-impedance state. Data outputs also change from high-impedance to active states at this time. After the data is read, $\overline{RD}$ is taken high, $\overline{INT}$ returns high, and the data outputs return to their high-impedance states.

The converter is set to the write-read mode when pin 7 is high and $\overline{WR}$/RDY is referred to as the "write" pin. Taking $\overline{CS}$ and the "write" pin low selects the converter and initiates measurement of the input signal. Approximately 600 ns after the "write" pin returns high, the conversion is completed. Conversion starts on the rising edge of $\overline{WR}$/RDY in the write-read mode.

The high-order 4-bit "flash" ADC measures the input by means of 16 comparators operating simultaneously. A high precision 4-bit DAC then generates a discrete analog voltage from the result of that conversion. After a time delay, a second bank of comparators does a low-order conversion on the analog difference between the input level and the high-order DAC output. The results from each of these conversions enter an 8-bit latch and are output to the three-state buffers on the falling edge of $\overline{RD}$.

TYPICAL APPLICATION DATA

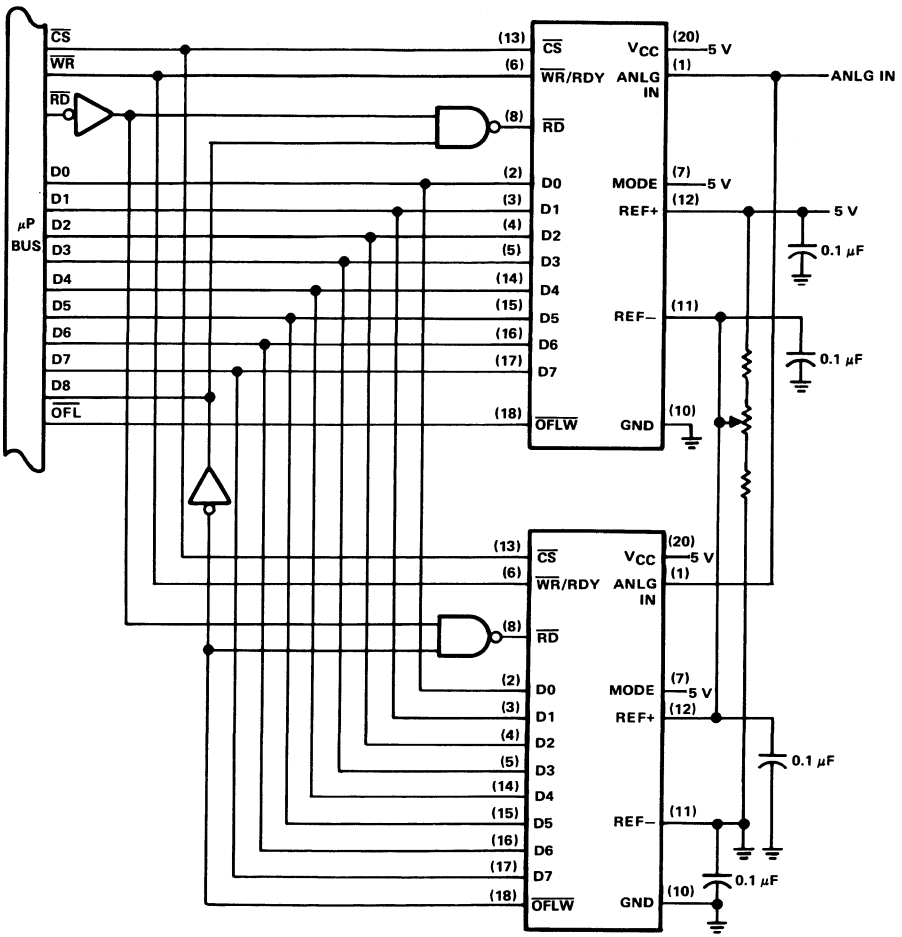


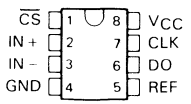
FIGURE 6. CONFIGURATION FOR 9-BIT RESOLUTION

ADC0831A, ADC0832A, ADC0831B, ADC0832B
A/D PERIPHERALS WITH SERIAL CONTROL

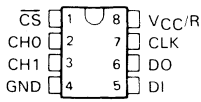
D2795, AUGUST 1985

- 8-Bit Resolution
- Easy Interface to Microprocessors or Stand-Alone Operation
- Operates Ratiometrically or with 5-V Reference
- Single Channel or Multiplexed Twin Channels with Single-Ended or Differential Input Options
- Input Range 0 to 5 V with Single 5-V Supply
- Inputs and Outputs are Compatible with TTL and MOS
- Conversion Time of 32 μs at CLK = 250 kHz
- Designed to be Interchangeable with National Semiconductor ADC0831 and ADC0832

ADC0831 . . . P DUAL-IN-LINE PACKAGE
(TOP VIEW)



ADC0832 . . . P DUAL-IN-LINE PACKAGE
(TOP VIEW)



DEVICE	TOTAL UNADJUSTED ERROR	
	A-SUFFIX	B-SUFFIX
ADC0831	±1 LSB	±½ LSB
ADC0832	±1 LSB	±½ LSB

description

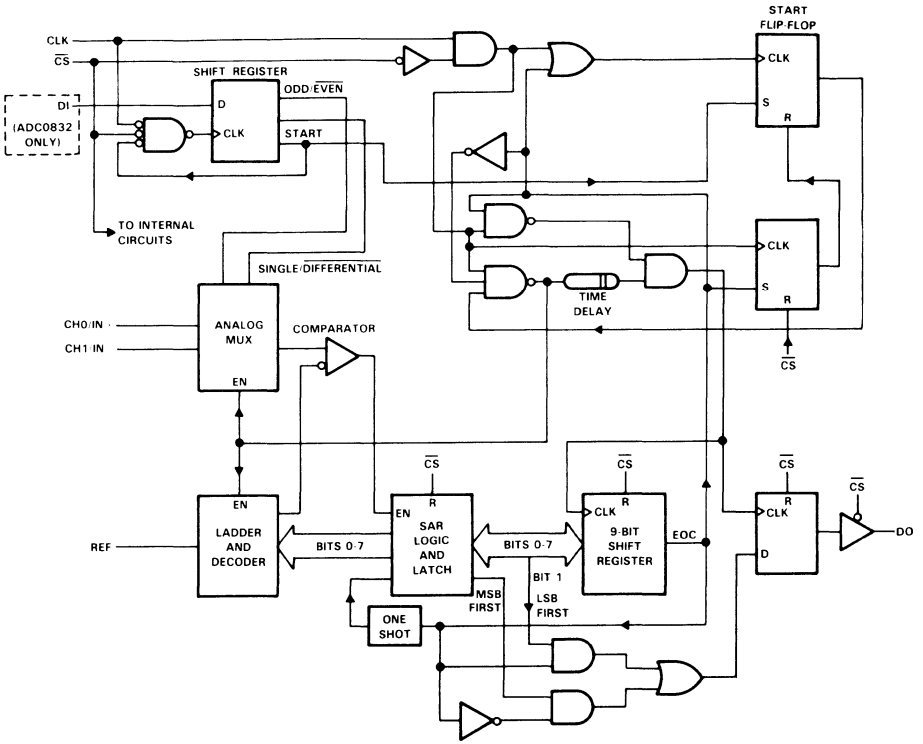
These devices are 8-bit successive-approximation analog-to-digital converters. The ADC0831A and ADC0831B have single input channels; the ADC0832A and ADC0832B have multiplexed twin input channels. The serial output is configured to interface with standard shift registers or microprocessors. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The ADC0832 multiplexer is software configured for single-ended or differential inputs. The differential analog voltage input allows for common-mode rejection or offset of the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

The operation of the ADC0831 and ADC0832 devices is very similar to the more complex ADC0834 and ADC0838 devices. Ratiometric conversion can be attained by setting the REF input equal to the maximum analog input signal value, which gives the highest possible conversion resolution. Typically, REF is set equal to V_{CC} (done internally on the ADC0832). For more detail on the operation of the ADC0831 and ADC0832 devices, refer to the ADC0834/ADC0838 data sheet.

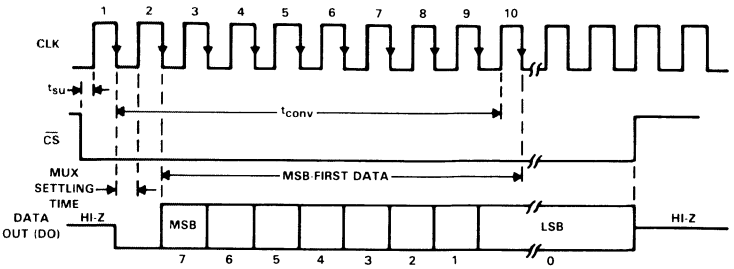
The ADC0831AI, ADC0831BI, ADC0832AI, and ADC0832BI are characterized for operation from −40°C to 85°C. The ADC0831AC, ADC0831BC, ADC0832AC, and ADC0832BC are characterized for operation from 0°C to 70°C.

functional block diagram

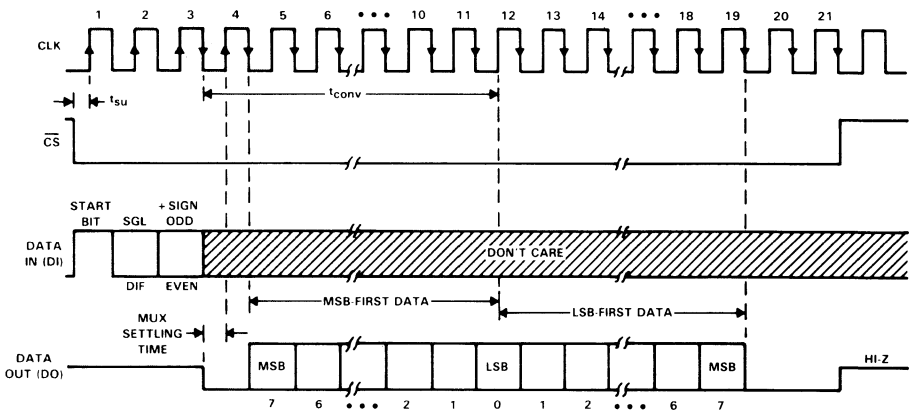


sequence of operation

ADC0831



ADC0832



ADC0832 MUX ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS		CHANNEL NUMBER	
SGL/$\overline{\text{DIF}}$	ODD/$\overline{\text{EVEN}}$	0	1
L	L	+	−
L	H	−	+
H	L	+	
H	H		+

H = high level, L = low level, − or + = polarity of selected input pin

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: Logic . . . . . −0.3 V to 15 V
Analog . . . . . −0.3 V to V_{CC} +0.3 V
Input current . . . . . ±5 mA
Total input current for package . . . . . ±20 mA
Operating free-air temperature range: AI and BI suffixes . . . . . −40°C to 85°C
AC and BC suffixes . . . . . 0°C to 70°C

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	6.3	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
f_{clock}	Clock frequency		10		400	kHz
	Clock duty cycle (see Note 2)		40		60	%
$t_{wH(CS)}$	Pulse duration, $\overline{CS}$ high		120			ns
t_{su}	Setup time, $\overline{CS}$ low or ADC0832 data valid before clock↑		250			ns
t_h	Hold time, ADC0832 data valid after clock↑		90			ns
T_A	Operating free-air temperature	AI and BI suffixes	−40		85	°C
		AC and BC suffixes	0		70	

NOTE 2: The clock duty cycle range ensures proper operation at all clock frequencies. If a clock frequency is used outside the recommended duty cycle range, the minimum pulse duration (high or low) is 1 μs.

electrical characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V, f_{clock} = 250 kHz (unless otherwise noted)

digital section

PARAMETER		TEST CONDITIONS†		AI, BI SUFFIX			AC, BC SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	V_{CC} = 4.75 V,	I_{OH} = −360 μA	2.4			2.8			V
		V_{CC} = 4.75 V,	I_{OH} = −10 μA	4.5			4.6			
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V,	I_{OL} = 1.6 mA	0.4			0.34			V
I_{IH}	High-level input current	V_{IH} = 5 V			0.005	1		0.005	1	μA
I_{IL}	Low-level input current	V_{IL} = 0			−0.005	−1		−0.005	−1	μA
I_{OH}	High-level output (source) current	V_{OH} = 0,	T_A = 25°C	−6.5	−14		−6.5	−14		mA
I_{OL}	Low-level output (sink) current	V_{OL} = V_{CC},	T_A = 25°C	8	16		8	16		mA
I_{OZ}	High-impedance-state output current (DO)	V_O = 5 V,	T_A = 25°C		0.01	3		0.01	3	μA
		V_O = 0,	T_A = 25°C		−0.01	−3		−0.01	−3	
C_i	Input capacitance				5			5		pF
C_o	Output capacitance				5			5		pF

† All parameters are measured under open-loop conditions with zero common-mode input voltage.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V, f_{clock} = 250 kHz (unless otherwise noted)

analog and converter section

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{ICR}	Common-mode input voltage range		See Note 3	−0.05 to V_{CC} + 0.05			V
$I_{I(stdby)}$	Standby input current (see Note 4)	On-channel	V_I = 5 V at on-channel,			1	μA
		Off-channel	V_I = 0 at off-channel			−1	
		On-channel	V_I = 0 at on-channel,			−1	
		Off-channel	V_I = 5 V at off-channel			1	
$r_{i(REF)}$	Input resistance to reference ladder			1.3	2.4	5.9	kΩ

total device

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
I_{CC}	Supply current	ADC0831			1	2.5	mA
		ADC0832			3	5.2	

† All parameters are measured under open-loop conditions with zero common-mode input voltage.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Includes ladder current.

NOTES: 3. If channel IN− is more positive than channel IN+, the digital output code will be 0000 0000. Connected to each analog input are two on-chip diodes that will conduct forward current for analog input voltages one diode drop above V_{CC}. Care must be taken during testing at low V_{CC} levels (4.5 V) because high-level analog input voltage (5 V) can, especially at high temperatures, cause this input diode to conduct and cause errors for analog inputs that are near full-scale. As long as the analog voltage does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V to 5 V input voltage range requires a minimum V_{CC} of 4.95 volts for all variations of temperature and load.

4. Standby input currents are currents going into or out of the on or off channels when the A/D converter is not performing conversion and the clock is in a high or low steady-state condition.

operating characteristics V_{CC} = REF = 5 V, f_{clock} = 250 kHz, t_r = t_f = 20 ns, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	BI, BC SUFFIX			AI, AC SUFFIX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Supply-voltage variation error			V_{CC} = 4.75 V to 5.25 V		±1/16	±1/4		±1/16	±1/4	LSB
Total unadjusted error (see Note 5)			V_{ref} = 5 V, T_A = MIN to MAX			±1/2			±1	LSB
Common-mode error			Differential mode		±1/16	±1/4		±1/16	±1/4	LSB
t_{pd}	Propagation delay time, output data after CLK↓ (see Note 6)	MSB-first data	C_L = 100 pF		650	1500		650	1500	ns
		LSB-first data			250	600		250	600	
t_{dis}	Output disable time, DO after $\overline{CS}$↑		C_L = 10 pF, R_L = 10 kΩ		125	250		125	250	ns
			C_L = 100 pF, R_L = 2 kΩ			500			500	
t_{conv}	Conversion time (multiplexer addressing time not included)					8			8	clock periods

† All parameters are measured under open-loop conditions with zero common-mode input voltage. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 5. Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.

6. The most significant-bit-first data is output directly from the comparator and therefore requires additional delay to allow for comparator response time. Least-significant-bit-first data applies only to ADC0832.

PARAMETER MEASUREMENT INFORMATION

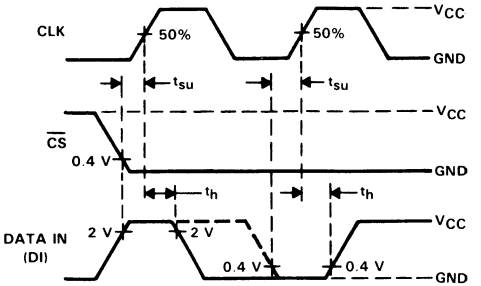


FIGURE 1. ADC0832 DATA INPUT TIMING

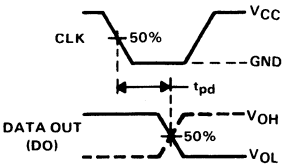
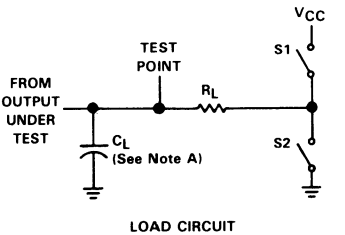
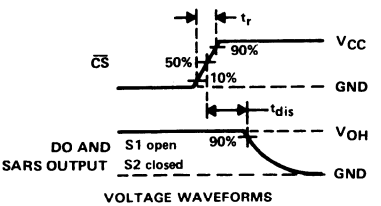


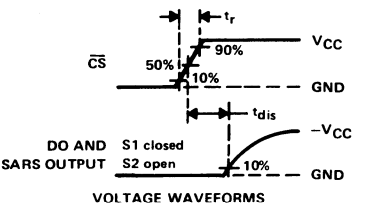
FIGURE 2. DATA OUTPUT TIMING



LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. OUTPUT DISABLE TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

UNADJUSTED OFFSET ERROR
vs
REFERENCE VOLTAGE

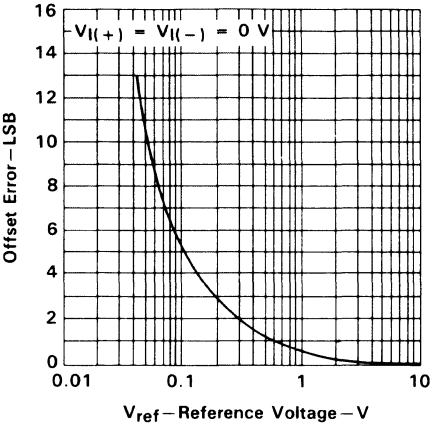


FIGURE 4

LINEARITY ERROR
vs
REFERENCE VOLTAGE

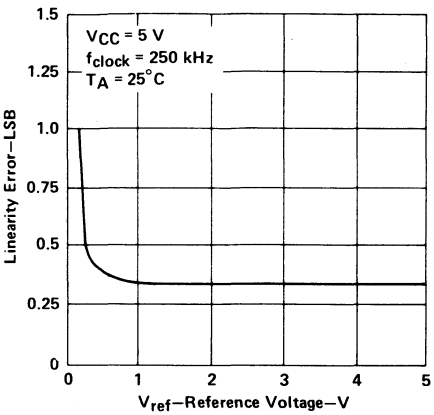


FIGURE 5

LINEARITY ERROR
vs
FREE-AIR TEMPERATURE

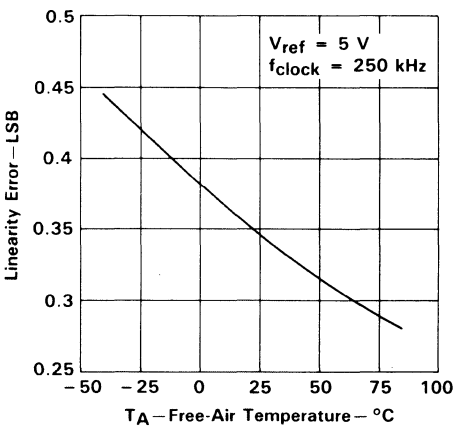


FIGURE 6

LINEARITY ERROR
vs
CLOCK FREQUENCY

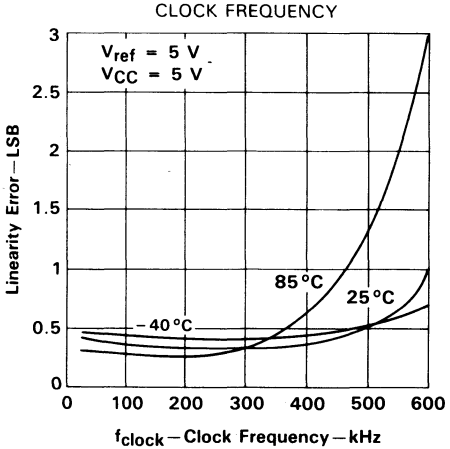


FIGURE 7

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

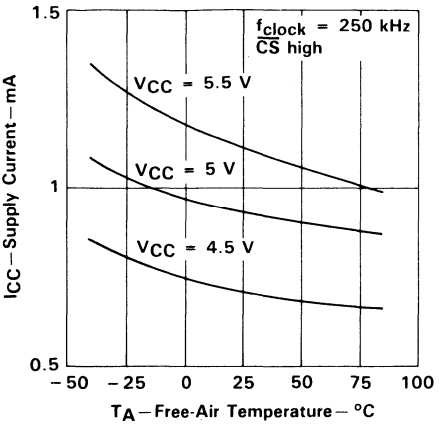


FIGURE 8

SUPPLY CURRENT
vs
CLOCK FREQUENCY

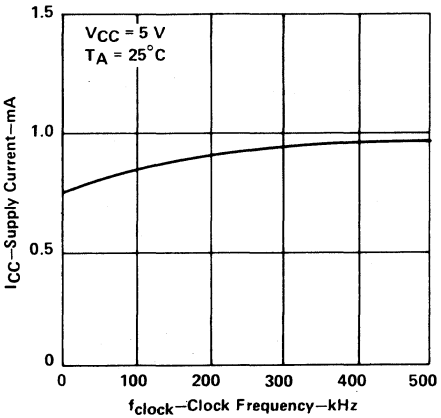


FIGURE 9

OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

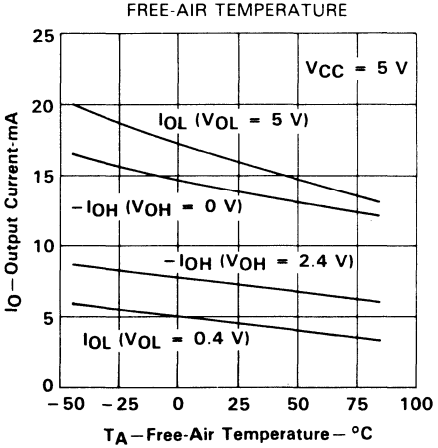


FIGURE 10

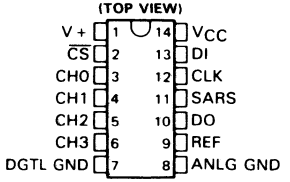
ADC0834A, ADC0838A, ADC0834B, ADC0838B
A/D PERIPHERALS WITH SERIAL CONTROL

D2795, AUGUST 1985

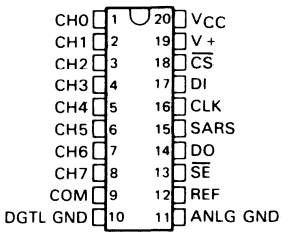
- 8-Bit Resolution
- Easy Interface to Microprocessors or Stand-Alone Operation
- Operates Ratiometrically or with 5-V Reference
- 4- or 8-Channel Multiplexer Options with Address Logic
- Shunt Regulator Allows Operation with High-Voltage Supplies
- Input Range 0 to 5 V with Single 5-V Supply
- Remote Operation with Serial Data Link
- Inputs and Outputs are Compatible with TTL and MOS
- Conversion Time of 32 μs at f_{clock} = 250 kHz
- Designed to be Interchangeable with National Semiconductor ADC0834 and ADC0838

DEVICE	TOTAL UNADJUSTED ERROR	
	A SUFFIX	B SUFFIX
ADC0834	±1 LSB	±1/2 LSB
ADC0838	±1 LSB	±1/2 LSB

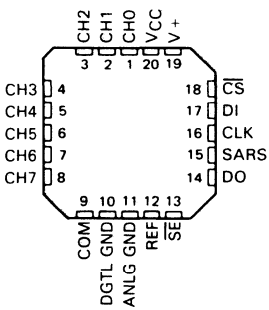
ADC0834 . . . N DUAL-IN-LINE PACKAGE
(TOP VIEW)



ADC0838 . . . N DUAL-IN-LINE PACKAGE
(TOP VIEW)



ADC0838 . . . FN CHIP CARRIER PACKAGE
(TOP VIEW)



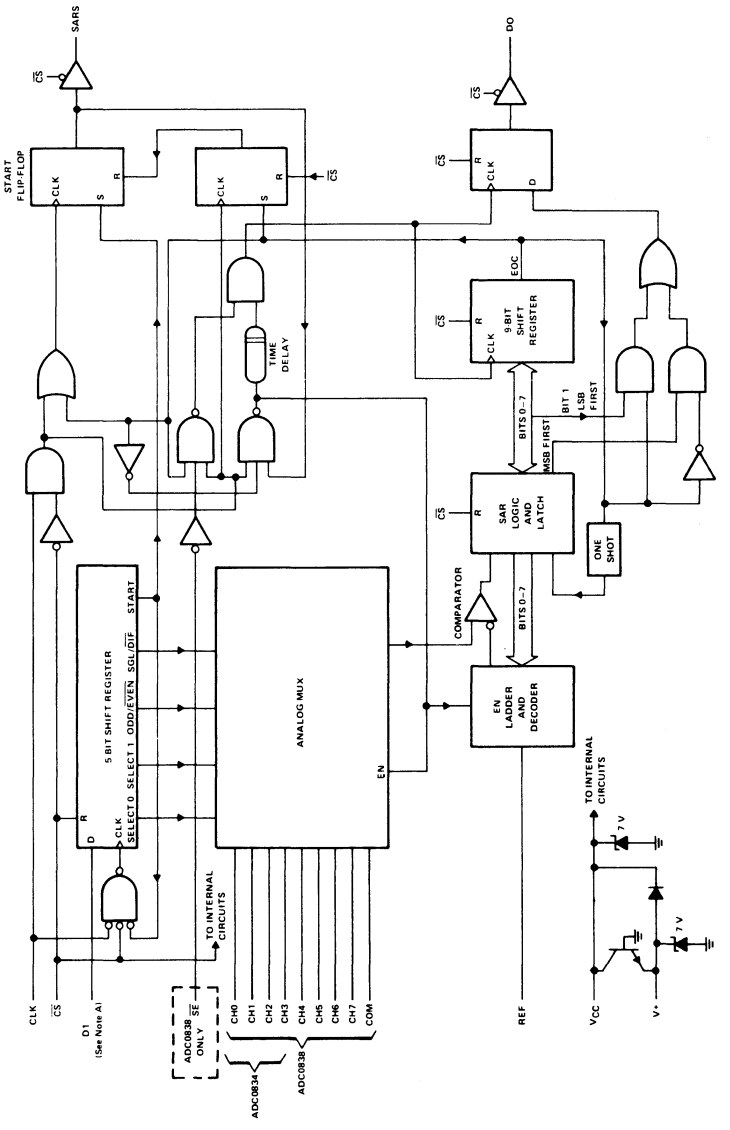
description

These devices are 8-bit successive-approximation analog-to-digital converters each with an input-configurable multichannel multiplexer and serial input/output. The serial input/output is configured to interface with standard shift registers or microprocessors. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The ADC0834 (4-channel) and ADC0838 (8-channel) multiplexer is software configured for single-ended or differential inputs as well as pseudo-differential input assignments. The differential analog voltage input allows for common-mode rejection or offset of the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

The ADC0834AI, ADC0834BI, ADC0838AI, and ADC0838BI are characterized for operation from −40°C to 85°C. The ADC0834AC, ADC0834BC, ADC0838AC, and ADC0838BC are characterized for operation from 0°C to 70°C.

functional block diagram



NOTE A: For the ADC0834, DI is input directly to the D input of SELECT 1, SELECT 0 is forced to a high.

functional description

The ADC0834 and ADC0838 use a sample data comparator structure that converts differential analog inputs by a successive-approximation routine. Operation of both devices is similar with the exception of a select enable ($\overline{SE}$) input, analog common input, and multiplexer addressing. The input voltage to be converted is applied to a channel terminal and is compared to ground (single-ended), to an adjacent input (differential), or to a common terminal (pseudo-differential) that can be an arbitrary voltage. The input terminals are assigned a positive (+) or negative (−) polarity. If the signal inputs applied to the assigned positive terminal is less than the signal on the negative terminal, the converter output is all zeros.

Channel selection and input configuration are under software control using a serial data link from the controlling processor. A serial communication format allows more functions to be included in a converter package with no increase in size. In addition, it eliminates the transmission of low-level analog signals by locating the converter at the analog sensor and communicating serially with the controlling processor. This process returns noise-free digital data to the processor.

A particular input configuration is assigned during the multiplexer addressing sequence. The multiplexer address is shifted into the converter through the data input (DI) line. The multiplexer address selects the analog inputs to be enabled and determines whether the input is single-ended or differential. When the input is differential, the polarity of the channel input is assigned. Differential inputs are assigned to adjacent channel pairs. For example, channel 0 and channel 1 may be selected as a differential pair. These channels cannot act differentially with any other channel. In addition to selecting the differential mode, the polarity may also be selected. Either channel of the channel pair may be designated as the negative or positive input.

The common input on the ADC0838 can be used for a pseudo-differential input. In this mode, the voltage on the common input is considered to be the negative differential input for all channel inputs. This voltage can be any reference potential common to all channel inputs. Each channel input can then be selected as the positive differential input. This feature is useful when all analog circuits are biased to a potential other than ground.

A conversion is initiated by setting the chip select ($\overline{CS}$) input low. This enables all logic circuits. The $\overline{CS}$ input must be held low for the complete conversion process. A clock input is received from the processor. On each low-to-high transition of the clock input, the data on the DI input is clocked into the multiplexer address shift register. The first logic high on the input is the start bit. A 3- to 4-bit assignment word follows the start bit. On each successive low-to-high transition of the clock input, the start bit and assignment word are shifted through the shift register. When the start bit has been shifted into the start location of the multiplexer register, the input channel has been selected and conversion starts. The SAR Status output (SARS) goes high to indicate that a conversion is in progress and the DI input to the multiplexer shift register is disabled for the duration of the conversion.

An interval of one clock period is automatically inserted to allow for the selected multiplexed channel to settle. The data output DO comes out of the high-impedance state and provides a leading low for this one clock period of multiplexer settling time. The SAR comparator compares successive outputs from the resistive ladder with the incoming analog signal. The comparator output indicates whether the analog input is greater than or less than the resistive ladder output. As the conversion proceeds, conversion data is simultaneously output from the DO output pin with the most significant bit (MSB) first.

After eight clock periods the conversion is complete and the SAR Status (SARS) output goes low.

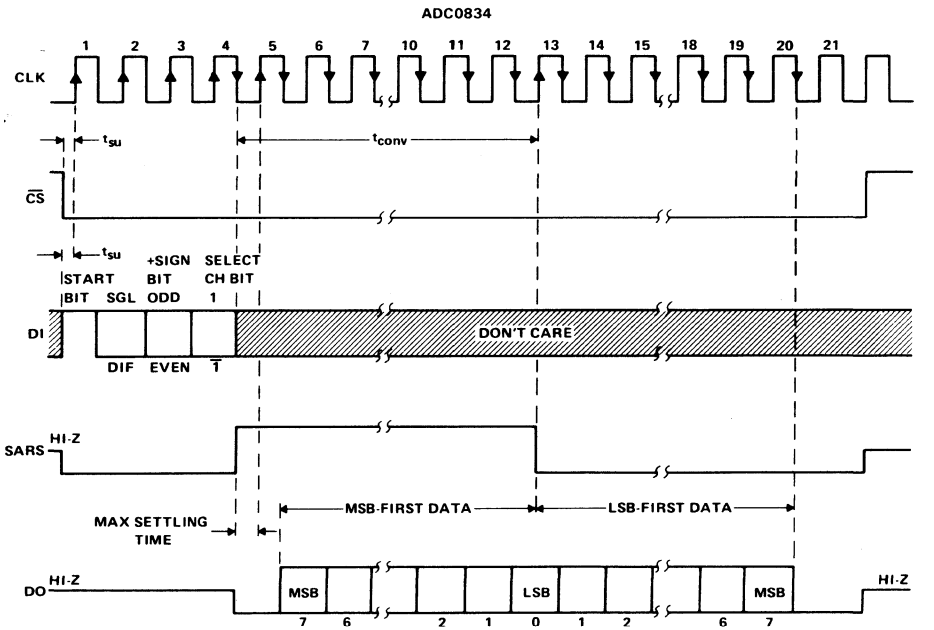
The ADC0834 outputs the least-significant-bit-first data after the MSB-first data stream. If the shift enable ($\overline{SE}$) line is held high on the ADC0838, the value of the least significant bit (LSB) will remain on the data line. When $\overline{SE}$ is forced low, the data is then clocked out as LSB-first data. (To output LSB first, the $\overline{SE}$ control input must first go low, then the data stored in the 9-bit shift register will output with LSB first.) When $\overline{CS}$ goes high, all internal registers are cleared. At this time the output circuits go to the high-impedance state. If another conversion is desired, the $\overline{CS}$ line must make a high-to-low transition followed by address information.

functional description (continued)

The DI and DO pins can be tied together and controlled by a bidirectional processor I/O bit received on a single wire. This is possible because the DI input is only examined during the multiplexer addressing interval and the DO output is still in a high-impedance state.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.

sequence of operation

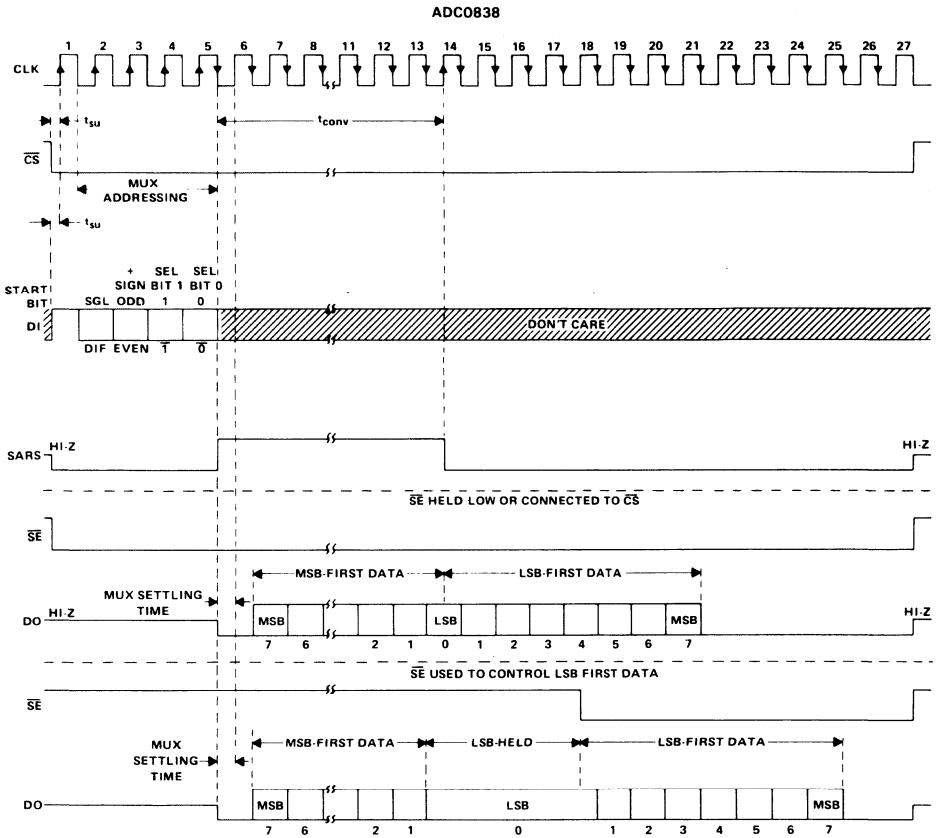


ADC0834 MUX ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS			CHANNEL NUMBER			
SGL/DIF	ODD/EVEN	SELECT BIT 1	0	1	2	3
L	L	L	+	−		
L	L	H			+	−
L	H	L	−	+		
L	H	H			−	+
H	L	L	+			
H	L	H			+	
H	H	L		+		
H	H	H				+

H = high level, L = low level, − or + = polarity of selected input pin

sequence of operation



ADC0838 MUX ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS				SELECTED CHANNEL NUMBER								COM
SGL/$\overline{DIF}$	ODD/$\overline{EVEN}$	SELECT		0		1		2		3		
		1	0	0	1	2	3	4	5	6	7	
L	L	L	L	+	−							
L	L	L	H			+	−					
L	L	H	L					+	−			
L	L	H	H							+	−	
L	H	L	L	−	+							
L	H	L	H			−	+					
L	H	H	L					+	−			
L	H	H	H							−	+	
H	L	L	L	+								−
H	L	L	H			+						−
H	L	H	L					+				−
H	L	H	H							+		−
H	H	L	L		+							−
H	H	L	H				+					−
H	H	H	L						+			−
H	H	H	H								+	−

H = high level, L = low level, − or + = polarity of selected input

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Notes 1 and 2) . . . . . 6.5 V
Input voltage range: Logic . . . . . −0.3 V to 15 V
Analog . . . . . −0.3 V to V_{CC} +0.3 V
Input current: V+ input . . . . . 15 mA
Any other input . . . . . ±5 mA
Total input current for package . . . . . ±20 mA
Operating free-air temperature range: AI and BI suffixes . . . . . −40°C to 85°C
AC and BC suffixes . . . . . 0°C to 70°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Internal zener diodes are connected from the V_{CC} input to ground and from the V+ input to ground. The breakdown voltage of each zener diode is approximately 7 volts. One zener diode can be used as a shunt regulator and connects to V_{CC} through a regular diode. When the voltage regulator powers the converter, this zener and regular diode combination ensures that the V_{CC} input (6.4 V) is less than the zener breakdown voltage. A series resistor is recommended to limit current into the V+ input.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	6.3	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
f_{clock}	Clock frequency		10		400	kHz
	Clock duty cycle (see Note 3)		40		60	%
$t_{wH(CS)}$	Pulse duration, $\overline{CS}$ high		120			ns
t_{su}	Setup time, $\overline{CS}$ low, $\overline{SE}$ low, or data valid before clock↑		250			ns
t_h	Hold time, data valid after clock↑		90			ns
T_A	Operating free-air temperature	AI and BI suffixes	−40		85	°C
		AC and BC suffixes	0		70	

NOTE 3: The clock duty cycle range ensures proper operation at all clock frequencies. If a clock frequency is used outside the recommended duty cycle range, the minimum pulse duration (high or low) is 1 μs.

electrical characteristics over recommended range of operating free-air temperature, V_{CC} = V+ = 5 V, f_{clock} = 250 kHz (unless otherwise noted)

digital section

PARAMETER		TEST CONDITIONS†		AI, BI SUFFIX			AC, BC SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	V_{CC} = 4.75 V,	I_{OH} = −360 μA	2.4			2.8			V
		V_{CC} = 4.75 V,	I_{OH} = −10 μA	4.5			4.6			
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V,	I_{OL} = 1.6 mA	0.4			0.34			V
I_{IH}	High-level input current	V_{IH} = 5 V			0.005	1		0.005	1	μA
I_{IL}	Low-level input current	V_{IL} = 0			−0.005	−1		−0.005	−1	μA
I_{OH}	High-level output (source) current	V_{OH} = 0,	T_A = 25°C	−6.5	−14		−6.5	−14		mA
I_{OL}	Low-level output (sink) current	V_{OL} = V_{CC},	T_A = 25°C	8	16		8	16		mA
I_{OZ}	High-impedance-state output current (DO or SARS)	V_O = 5 V,	T_A = 25°C		0.01	3		0.01	3	μA
		V_O = 0,	T_A = 25°C		−0.01	−3		−0.01	−3	
C_i	Input capacitance				5			5		pF
C_o	Output capacitance				5			5		pF

†All parameters are measured under open-loop conditions with zero common-mode input voltage (unless otherwise specified).
‡All typical values are at V_{CC} = V+ = 5 V, T_A = 25°C.

electrical characteristics over recommended range of operating free-air temperature, V_{CC} = V+ = 5 V, f_{clock} = 250 kHz (unless otherwise noted)

analog and converter section

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{ICR}	Common-mode input voltage range		See Note 4	−0.05 to V_{CC} +0.05			V
$I_{I(stdby)}$	Standby input current (see Note 5)	On-channel	V_I = 5 V at on-channel,			1	μA
		Off-channel	V_I = 0 at off-channel			−1	
		On-channel	V_I = 0 at on-channel,			−1	
		Off-channel	V_I = 5 V at off-channel			1	
$r_{i(ref)}$	Input resistance to reference ladder			1.3	2.4	5.9	kΩ

total device

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_Z	Internal zener diode breakdown voltage	I_I = 15 mA at V+ pin, See Note 2	6.3	7	8.5	V
I_{CC}	Supply current			1	2.5	mA

†All parameters are measured under open-loop conditions with zero common-mode input voltage.
‡All typical values are at V_{CC} = 5 V, V+ = 5 V, T_A = 25°C.

NOTES: 2. Internal zener diodes are connected from the V_{CC} input to ground and from the V+ input to ground. The breakdown voltage of each zener diode is approximately 7 volts. One zener diode can be used as a shunt regulator and connects to V_{CC} through a regular diode. When the voltage regulator powers the converter, this zener and regular diode combination ensures that the V_{CC} input (6.4 V) is less than the zener breakdown voltage. A series resistor is recommended to limit current into the V+ input.

4. If channel IN− is more positive than channel IN+, the digital output code will be 0000 0000. Connected to each analog input are two on-chip diodes that will conduct forward current for analog input voltages one diode drop above V_{CC}. Care must be taken during testing at low V_{CC} levels (4.5 V) because high-level analog input voltage (5 V) can, especially at high temperatures, cause this input diode to conduct and cause errors for analog inputs that are near full-scale. As long as the analog voltage does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V to 5 V input voltage range requires a minimum V_{CC} of 4.950 volts for all variations of temperature and load.
5. Standby input currents are currents going into or out of the on or off channels when the A/D converter is not performing conversion and the clock is in a high or low steady-state condition.

operating characteristics V+ = V_{CC} = 5 V, f_{clock} = 250 kHz, $t_r = t_f$ = 20 ns, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	BI, BC SUFFIX			AI, AC SUFFIX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
	Supply-voltage variation error		V_{CC} = 4.75 V to 5.25 V		±1/16	±1/4		±1/16	±1/4	LSB
	Total unadjusted error (see Note 6)		V_{ref} = 5 V, T_A = MIN to MAX			±1/2			±1	LSB
	Common-mode error		Differential mode		±1/16	±1/4		±1/16	±1/4	LSB
	Change in zero-error from V_{CC} = 5 V to internal zener diode operation (see Note 2)		I_I = 15 mA at V+ pin, V_{ref} = 5 V, V_{CC} open			1			1	LSB
t_{pd}	Propagation delay time, output data after CLK↓ (see Note 7)	MSB-first data	C_L = 100 pF		650	1500		650	1500	ns
		LSB-first data			250	600		250	600	
t_{dis}	Output disable time, DO or SARS after $\overline{CS}$↑		C_L = 10 pF, R_L = 10 kΩ		125	250		125	250	ns
			C_L = 100 pF, R_L = 2 kΩ			500			500	
t_{conv}	Conversion time (multiplexer addressing time not included)					8			8	clock periods

†All parameters are measured under open-loop conditions with zero common-mode input voltage. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 2. Internal zener diodes are connected from the V_{CC} input to ground and from the V+ input to ground. The breakdown voltage of each zener diode is approximately 7 volts. One zener diode can be used as a shunt regulator and connects to V_{CC} through a regular diode. When the voltage regulator powers the converter, this zener and regular diode combination ensures that the V_{CC} input (6.4 V) is less than the zener breakdown voltage. A series resistor is recommended to limit current into the V+ input.

6. Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.
7. The most significant bit (MSB) data is output directly from the comparator and therefore requires additional delay to allow for comparator response time.

PARAMETER MEASUREMENT INFORMATION

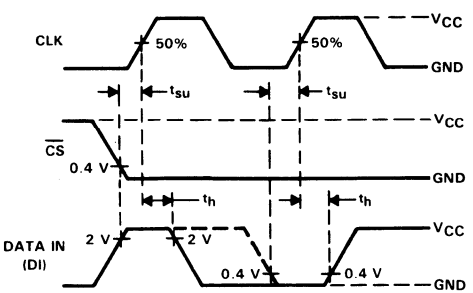


FIGURE 1. DATA INPUT TIMING

PARAMETER MEASUREMENT INFORMATION

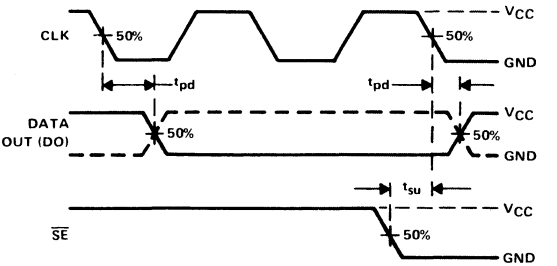
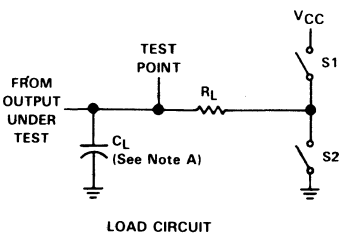
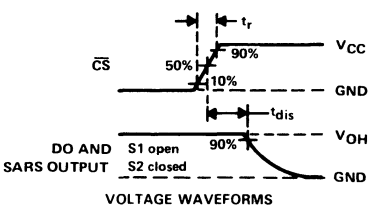


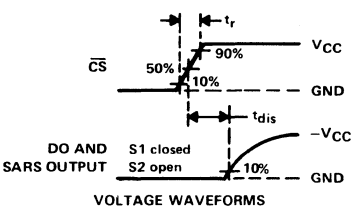
FIGURE 2. DATA OUTPUT TIMING



LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. OUTPUT DISABLE TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

UNADJUSTED OFFSET ERROR
vs
REFERENCE VOLTAGE

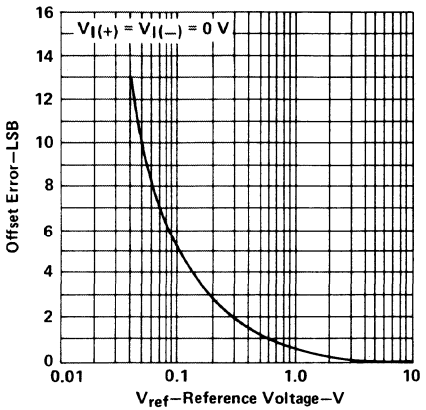


FIGURE 4

LINEARITY ERROR
vs
REFERENCE VOLTAGE

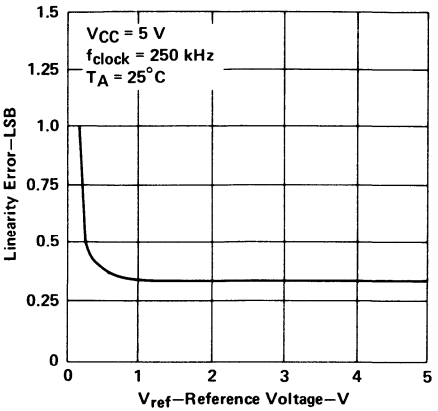


FIGURE 5

LINEARITY ERROR
vs
FREE-AIR TEMPERATURE

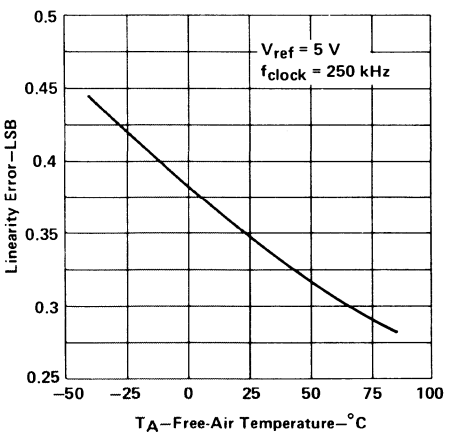


FIGURE 6

LINEARITY ERROR
vs
CLOCK FREQUENCY

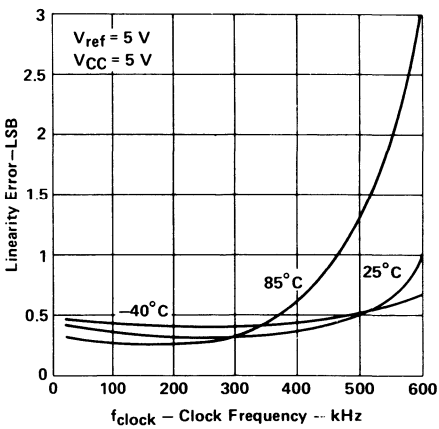


FIGURE 7

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

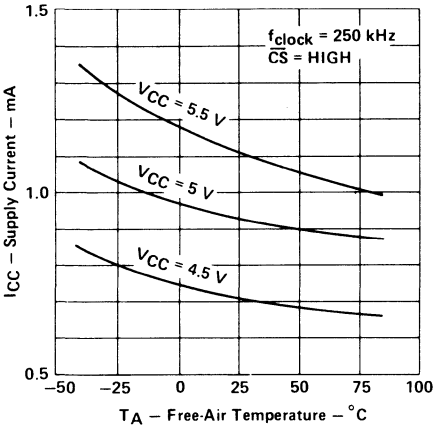


FIGURE 8

SUPPLY CURRENT
vs
CLOCK FREQUENCY

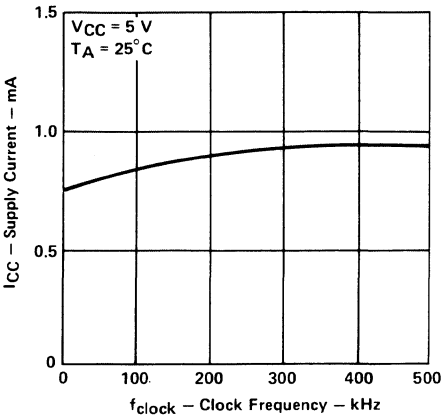


FIGURE 9

OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

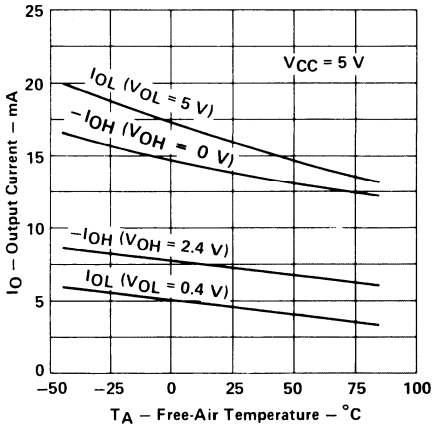
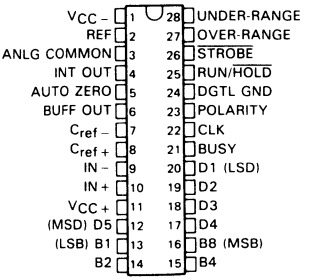


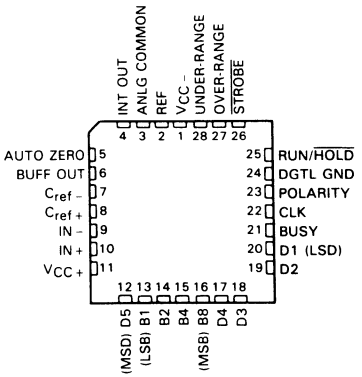
FIGURE 10

- **Advanced LinCMOS™ Technology**
- **Zero Reading for 0-V Input**
- **Precision Null Detection with True Polarity at Zero**
- **1-pA Typical Input Current**
- **True Differential Input**
- **Multiplexed Binary-Coded-Decimal Output**
- **Low Rollover Error: ±1 Count Maximum**
- **Control Signals Allow Interfacing with UARTs or Microprocessors**
- **Autoranging Capability with Over- and Under-Range Signals**
- **TTL-Compatible Outputs**
- **Direct Replacement for Teledyne TSC7135, Intersil ICL7135, Maxim ICL7135, and Siliconix Si7135**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The ICL7135C and TLC7135C converters are manufactured with Texas Instruments highly efficient Advanced LinCMOS™ technology. This 4 1/2-digit dual-slope-integrating analog-to-digital converter is designed to provide interfaces to both a microprocessor and a visual display. The digit-drive outputs D1 through D4 and multiplexed binary-coded-decimal outputs, B1 through B4, provide an interface for LED or LCD decoder/drivers as well as microprocessors.

The ICL7135C and TLC7135C offer 50-ppm (one part in 20,000) resolution with a maximum linearity error of one count. The zero error is less than 10 μV and zero drift is less than 0.5 μV/°C. Source-impedance errors are minimized by low input current (less than 10 pA). Rollover error is limited to ±1 count.

The BUSY, $\overline{\text{STROBE}}$, RUN/$\overline{\text{HOLD}}$, OVER-RANGE, and UNDER-RANGE control signals support microprocessor-based measurement systems. The control signals also can support remote data acquisition systems with data transfer via universal asynchronous receiver transmitters (UARTs).

AVAILABLE OPTIONS†

SYMBOLIZATION		OPERATING
DEVICE	PACKAGE SUFFIX	TEMPERATURE RANGE
ICL7135C	FN, N	0°C to 70°C
TLC7135C	FN, N	0°C to 70°C

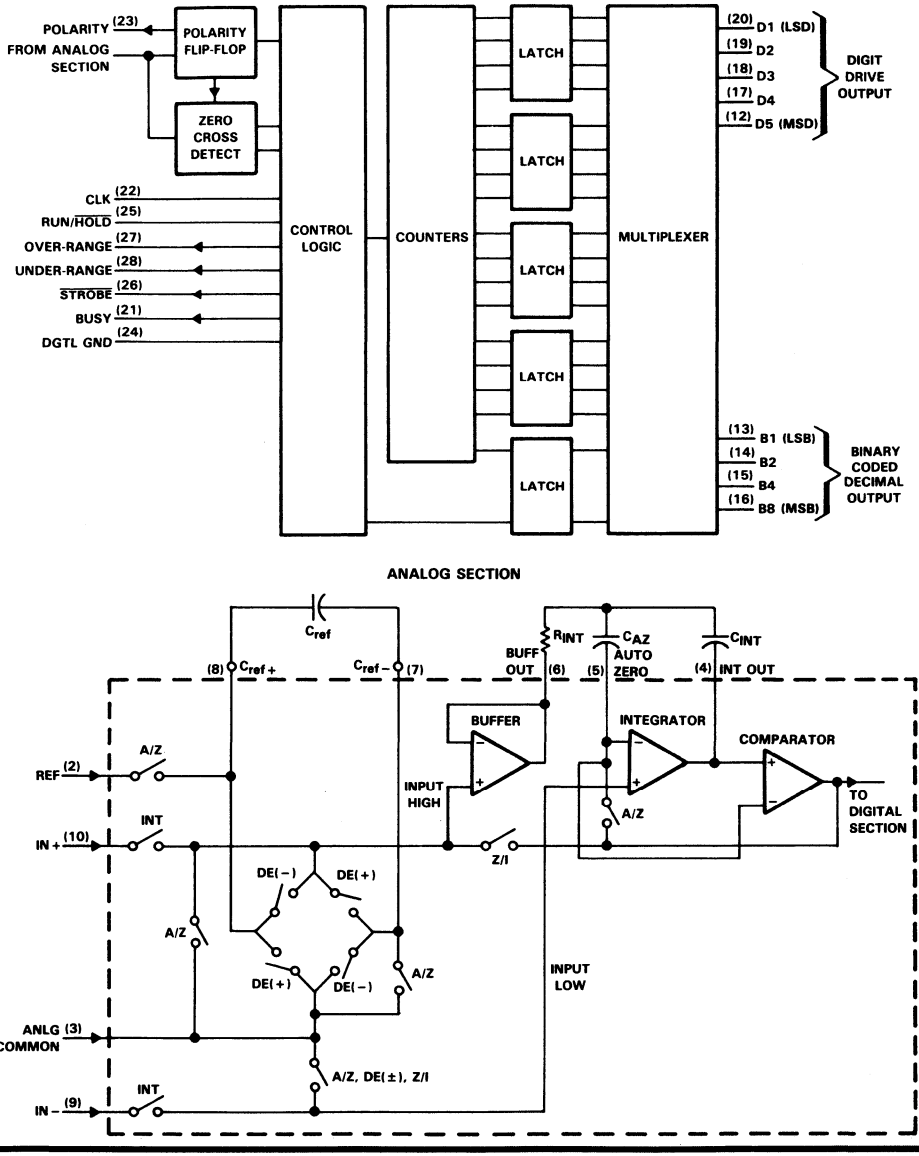
† In many instances, these ICs may have ICL7135C and TLC7135C symbolization on the package.

The ICL7135C and TLC7135C are characterized for operation from 0°C to 70°C.

Caution. This device has limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage.

Advanced LinCMOS™ is a trademark of Texas Instruments Incorporated.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (V_{CC+} with respect to V_{CC-}) . . . . . 15 V
Analog input voltage (pin 9 or pin 10) . . . . . V_{CC-} to V_{CC+}
Reference voltage range . . . . . V_{CC-} to V_{CC+}
Clock input voltage range . . . . . 0 V to V_{CC+}
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C
Case temperature for 10 seconds: FN package . . . . . 260°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4	5	6	V
Supply voltage, V_{CC-}	−3	−5	−8	V
Reference voltage, V_{ref}		1		V
High-level input voltage, CLK, RUN/$\overline{HOLD}$, V_{IH}	2.8			V
Low-level input voltage, CLK, RUN/$\overline{HOLD}$, V_{IL}			0.8	V
Differential input voltage, V_{ID}	V_{CC-} +1		V_{CC+} −0.5	V
Maximum operating frequency, f_{clock} (see Note 1)	1.2	2		MHz
Operating free-air temperature range, T_A	0		70	°C

NOTE 1: Clock frequency range extends down to 0 Hz.

electrical characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{ref} = 1 V, f_{clock} = 120 kHz, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	D1-D5,B1,B2,B4,B8	I_O = −1 mA		2.4		5	V
		Other outputs	I_O = −10 μA		4.9		5	
V_{OL}	Low-level output voltage		I_O = 1.6 mA				0.4	V
	Peak-to-peak output noise voltage (see Note 2)		V_{ID} = 0,	Full Scale = 2 V		15		μV
α_{VO}	Zero-reading temperature coefficient of output voltage		V_{ID} = 0,	0°C ≤ T_A ≤ 70°C		0.5	2	μV/°C
I_{IH}	High-level input current		V_I = 5 V,	0°C ≤ T_A ≤ 70°C		0.1	10	μA
I_{IL}	Low-level input current		V_I = 0 V,	0°C ≤ T_A ≤ 70°C		−0.02	−0.1	mA
I_I	Input leakage current, pins 9 and 10		V_{ID} = 0	T_A = 25°C		1	10	pA
				0°C ≤ T_A ≤ 70°C			250	
I_{CC+}	Positive supply current		f_{clock} = 0	T_A = 25°C		1	2	mA
				0°C ≤ T_A ≤ 70°C			3	
I_{CC-}	Negative supply current		f_{clock} = 0	T_A = 25°C		−0.8	−2	mA
				0°C ≤ T_A ≤ 70°C			−3	
C_{pd}	Power dissipation capacitance		See Note 3			40		pF

NOTES: 2. This is the peak-to-peak value that is not exceeded 95% of the time.
3. Factor relating clock-frequency to increase in supply current. At V_{CC+} = 5 V

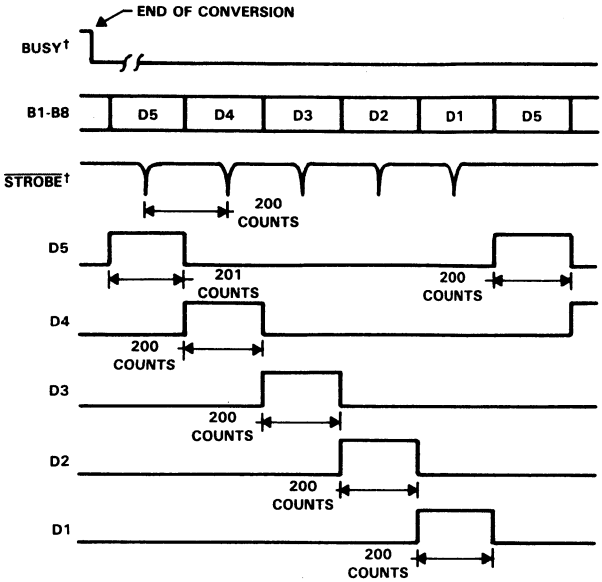
$$I_{CC+} = I_{CC+(f_{clock}=0)} + C_{pd} \times 5\ V \times f_{clock}$$

operating characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{ref} = 1 V, f_{clock} = 120 kHz, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
αFS	Full-scale temperature coefficient (see Note 4)	V_{ID} = 2 V, 0°C ≤ T_A ≤ 70°C			5	ppm/°C
	Linearity error	−2 V ≤ V_{ID} ≤ 2 V		0.5	1	count
	Differential linearity error (see Note 5)	−2 V ≤ V_{ID} ≤ 2 V		0.01		LSB
	± Full-scale symmetry error (see Note 6) (rollover error)	V_{ID} = ±2 V		0.5	1	count
	Display reading with 0-V input	V_{ID} = 0, 0°C ≤ T_A ≤ 70°C	−0.0000	±0.0000	+0.0000	Digital Reading
	Display reading in ratiometric operation	V_{ID} = V_{ref}, T_A = 25°C	+0.9998	+0.9999	+1.0000	Digital Reading
		0°C ≤ T_A ≤ 70°C	+0.9995	+0.9999	+1.0005	

NOTES: 4. This parameter is measured with an external reference having a temperature coefficient of less than 0.01 ppm/°C.
5. The magnitude of the difference between the worst case step of adjacent counts and the ideal step.
6. Rollover error is the difference between the absolute values of the conversion for 2 V and −2 V.

timing diagrams



† Delay between BUSY going low and the first STROBE pulse is dependent upon the analog input.

FIGURE 1

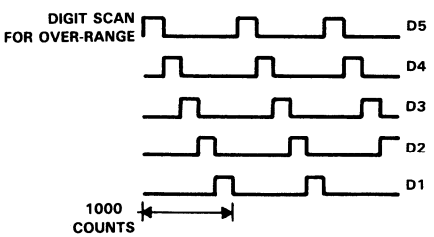


FIGURE 2

timing diagrams (continued)

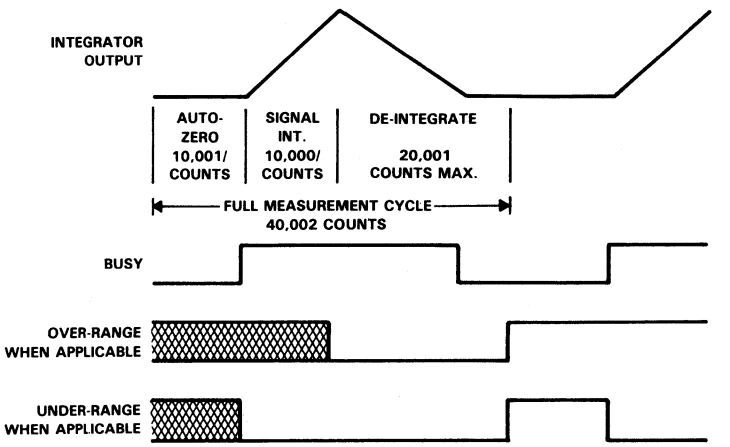
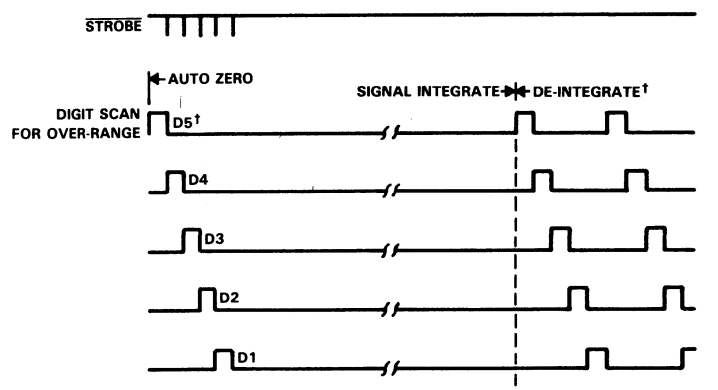


FIGURE 3



†First D5 of AUTO ZERO and DE-INTEGRATE is one count longer.

FIGURE 4

PRINCIPLES OF OPERATION

A measurement cycle for the ICL7135C and TLC7135C consists of the following four phases.

1. Auto-Zero Phase. The internal IN+ and IN− inputs are disconnected from the pins and internally connected to ANLG COMMON. The reference capacitor is charged to the reference voltage. The system is configured in a closed loop and the auto-zero capacitor is charged to compensate for offset voltages in the buffer amplifier, integrator, and comparator. The auto-zero accuracy is limited only by the system noise, and the overall offset, as referred to the input, is less than 10 μV.
2. Signal Integrate Phase. The auto-zero loop is opened and the internal IN+ and IN− inputs are connected to the external pins. The differential voltage between these inputs is integrated for a fixed period of time. If the input signal has no return with respect to the converter power supply, IN− can be tied to ANLG COMMON to establish the correct common-mode voltage. Upon completion of this phase, the polarity of the input signal is recorded.
3. De-integrate Phase. The reference is used to perform the de-integrate task. The internal IN− is internally connected to ANLG COMMON and IN+ is connected across the previously charged reference capacitor. The recorded polarity of the input signal is used to ensure that the capacitor will be connected with the correct polarity so that the integrator output polarity will return to zero. The time, which is required for the output to return to zero, is proportional to the amplitude of the input signal. The return time is displayed as a digital reading and is determined by the equation 10,000 x (V_{ID}/V_{ref}). The maximum or full-scale conversion occurs when V_{ID} is two times V_{ref}.
4. Zero Integrator Phase. The internal IN− is connected to ANLG COMMON. The system is configured in a closed loop to cause the integrator output to return to zero. Typically this phase requires 100 to 200 clock pulses. However, after an over-range conversion, 6200 pulses are required.

description of analog circuits

input signal range

The common mode range of the input amplifier extends from 1 V above the negative supply to 1 V below the positive supply. Within this range, the common mode rejection ratio (CMRR) is typically 86 dB. Both differential and common mode voltages cause the integrator output to swing. Therefore, care must be exercised to assure the integrator output does not saturate.

analog common

Analog common (ANLG COMMON) is connected to the internal IN− during the auto-zero, de-integrate, and zero integrator phases. If IN− is connected to a voltage which is different than analog common during the signal integrate phase, the resulting common mode voltage will be rejected by the amplifier. However, in most applications, IN LO will be set at a known fixed voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common mode voltage from the converter. Removing the common mode voltage in this manner will slightly increase conversion accuracy.

reference

The reference voltage is positive with respect to analog common. The accuracy of the conversion result is dependent upon the quality of the reference. Therefore, to obtain a high accuracy conversion, a high quality reference should be used.

description of digital circuits

RUN/$\overline{\text{HOLD}}$ input

When the RUN/$\overline{\text{HOLD}}$ input is high or open, the device will continuously perform measurement cycles every 40,002 clock pulses. If this input is taken low, the IC will continue to perform the ongoing measurement cycle and then hold the conversion reading for as long as the pin is held low. If the pin is held low after completion of a measurement cycle, a short positive pulse (greater than 300 ns) will initiate a new measurement cycle. If this positive pulse occurs before the completion of a measurement cycle, it will not be recognized. The first STROBE pulse, which occurs 101 counts after the end of a measurement cycle, is an indication of the completion of a measurement cycle. Thus, the positive pulse could be used to trigger the start of a new measurment after the first STROBE pulse.

$\overline{\text{STROBE}}$ input

Negative going pulses from this input are used to transfer the BCD conversion data to external latches, UARTS, or microprocesors. At the end of the measurement cycle, the digit-drive (D5) input goes high and remains high for 201 counts. The most significant digit (MSD) BCD bits are placed on the BCD pins. After the first 101 counts, halfway through the duration of output D1-D5 going high, the $\overline{\text{STROBE}}$ pin goes low for 1/2 clock pulse width. The placement of the $\overline{\text{STROBE}}$ pulse at the midpoint of the D5 high pulse allows the information to be latched into an external device on either a low-level or an edge. Such placement of the $\overline{\text{STROBE}}$ pulse also ensures that the BCD bits for the second MSD will not yet be competing for the BCD lines and latching of the correct bits is assured. The above process is repeated for the second MSD and the D4 output. Similarly, the process is repeated through the least significant digit (LSD). Subsequently, inputs D5 through D1 and the BCD lines will continue scanning without the inclusion of $\overline{\text{STROBE}}$ pulses. This subsequent continuous scanning causes the conversion results to be continuously displayed. Such subsequent scanning does not occur when an over-range condition occurs.

BUSY output

The BUSY output goes high at the beginning of the signal integrate phase and remains high until the first clock pulse after zero-crossing or at the end of the measurement cycle if an over-range condition occurs. It is possible to use the BUSY pin to serially transmit the conversion result. Serial transmission can be accomplished by ANDing the BUSY and CLOCK signals and transmitting the ANDed output. The transmitted output consists of 10,001 clock pulses, which occur during the signal integrate phase, and the number of clock pulses, which occur during the de-integrate phase. The conversion result can be obtained by subtracting 10,001 from the total number of clock pulses.

OVER-RANGE output

When an over-range condition occurs, this pin goes high after the BUSY signal goes low at the end of the measurement cycle. As previously noted, the BUSY signal remains high until the end of the measurement cycle when an over-range condition occurs. The OVER-RANGE output goes high at end of BUSY and goes low at the beginning of the de-integrate phase in the next measurement cycle.

UNDER-RANGE output

At the end of the BUSY signal, this pin goes high if the conversion result is less than or equal to 9% (count of 1800) of the full-scale range. The UNDER-RANGE output is brought low at the beginning of the signal integrate phase of the next measurement cycle.

PRINCIPLES OF OPERATION

POLARITY output

The POLARITY output is high for a positive input signal and is updated at the beginning of each de-integrate phase. The polarity output is valid for all inputs including ±0 and over-range signals.

digit-drive (D5, D4, D2 and D1) outputs

Each digit-drive output (D1 through D5) sequentially goes high for 200 clock pulses. This sequential process is continuous unless an over-range occurs. When an over-range occurs, all of the digit drive outputs are blanked from the end of the strobe sequence until the beginning of the de-integrate phase (when the sequential digit drive activation begins again). The blanking activity, during an over-range condition, may be used to cause the display to flash and indicate the over-range condition.

BCD outputs

The BCD bits (B8, B4, B2 and B1) for a given digit are sequentially activated on these outputs. Simultaneously, the appropriate Digit-drive line for the given digit is activated.

system aspects

integrating resistor

The value of the integrating resistor (R_{INT}) is determined by the full scale input voltage and the output current of the integrating amplifier. The integrating amplifier can supply 20 μA of current with negligible non-linearity. The equation for determining the value of this resistor is as follows:

$$R_{INT} = \frac{\text{FULL-SCALE VOLTAGE}}{I_{INT}}$$

Integrating amplifier current, I_{INT}, from 5 to 40 μA will yield good results. However, the nominal and recommended current is 20 μA.

integrating capacitor

The product of the integrating resistor and capacitor should be selected to give the maximum voltage swing without causing the integrating amplifier output to saturate and get too close to the power supply voltages. If the amplifier output is within 0.3 V of either supply, saturation will occur. With ±5-V supplies and ANLG COMMON connected to ground, the designer should design for a ±3.5-V to ±4-V integrating amplifier swing. A nominal capacitor value is 0.47 μF. The equation for determining the value of the integrating capacitor (C_{INT}) is as follows:

$$C_{INT} = \frac{10{,}000 \times \text{CLOCK PERIOD} \times I_{INT}}{\text{INTEGRATOR OUTPUT VOLTAGE SWING}}$$

where: I_{INT} is nominally 20 μA.

Capacitors with large tolerances and high dielectric absorption can induce conversion inaccuracies. A capacitor, which is too small could cause the integrating amplifier to saturate. High dielectric absorption causes the effective capacitor value to be different during the signal integrate and de-integrate phases. Polypropylene capacitors have very low dielectric absorption. Polystyrene and Polycarbonate capacitors have higher dielectric absorption, but also work well.

PRINCIPLES OF OPERATION

auto-zero and reference capacitor

Large capacitors will tend to reduce noise in the system. Dielectric absorption is unimportant except during power-up or overload recovery. Typical values are 1 μF.

reference voltage

For high-accuracy absolute measurements, a high quality reference should be used.

rollover resistor and diode

The ICL7135C and TLC7135C have a small rollover error, however it can be corrected. The correction is to connect the cathode of any silicon diode to the INT OUT pin and the anode to a resistor. The other end of the resistor is connected to ANLG COMMON or ground. For the recommended operating conditions the resistor value is 100 kΩ. This value may be changed to correct any rollover error which has not been corrected. In many non-critical applications, the resistor and diode are not needed.

maximum clock frequency

For most dual-slope A/D converters, the maximum conversion rate is limited by the frequency response of the comparator. In this circuit, the comparator follows the integrator ramp with a 3 μs delay. Therefore, with a 160-kHz clock frequency (6 μs period), half of the first reference integrate clock period is lost in delay. Hence, the meter reading will change from 0 to 1 with a 50-μV input, 1 to 2 with a 150-μV input, 2 to 3 with a 250-μV input, etc. This transition at midpoint is desirable; however, if the clock frequency is increased appreciably above 160 kHz, the instrument will flash "1" on noise peaks even when the input is shorted. The above transition points assume a 2-V input range is equivalent to 20,000 clock cycles.

If the input signal is always of one polarity, comparator delay need not be a limitation. Clock rates of 1 MHz are possible since non-linearity and noise do not increase substantially with frequency. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

For signals with both polarities, the clock frequency can be extended above 160 kHz without error by using a low value resistor in series with the integrating capacitor. This resistor causes the integrator to jump slightly towards the zero-crossing level at the beginning of the de-integrate phase and thus, compensates for the comparator delay. This series resistor should be 10 Ω to 50 Ω. This approach allows clock frequencies up to 480 kHz.

minimum clock frequency

The minimum clock frequency limitations result from capacitor leakage from the auto-zero and reference capacitors. Measurement cycles as high as 10 s are not influenced by leakage error.

rejection of 50 Hz or 60 Hz pickup

To maximize the rejection of 50 Hz or 60 Hz pickup, the clock frequency should be chosen so that an integral multiple of 50 Hz or 60 Hz periods occur during the signal integrate phase. To achieve rejection of these signals, some clock frequencies which could be used are as follows:

50 Hz: 250, 166.66, 125, 100 kHz, etc.
60 Hz: 300, 200, 150, 120, 100, 40, 33.33 kHz, etc.

PRINCIPLES OF OPERATION

zero-crossing flip-flop

This flip-flop interrogates the comparator's zero-crossing status. The interrogation is performed after the previous clock cycle and the positive half of the ongoing clock cycle have occurred so that any comparator transients which result from the clock pulses do not affect the detection of a zero-crossing. This procedure delays the zero-crossing detection by one clock cycle. To eliminate the inaccuracy, which is caused by this delay, the counter is disabled for one clock cycle at the beginning of the de-integrate phase. Therefore, when the zero-crossing is detected one clock cycle later than the zero-crossing actually occurs, the correct number of counts is displayed.

noise

The peak-to-peak noise around zero is approximately 15 μV (peak-to-peak value not exceeded 95% of the time). Near full scale, this value increases to approximately 30 μV. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

analog and digital grounds

For high-accuracy applications, ground loops must be avoided. Return currents from digital circuits must not be sent to the analog ground line.

power supplies

The ICL7135C and TLC7135C are designed to work with $\pm$5-V power supplies. However, 5-V operation is possible if the input signal does not vary more than $\pm$1.5 V from mid-supply.

JULY 1988

FEATURES

- 6μs Max. Acquisition Time
- 0.005% Max. Gain Error
- 1mV Max. Offset Voltage
- 1mV Max. Hold Step
- Very Low Feedthrough 86dB Min.
- High Input Impedance under All Conditions
- Logic Inputs Compatible with All Logic Families

APPLICATIONS

- 12-Bit Data Acquisition Systems
- Ramp Generators
- Analog Switches
- Staircase Generators
- Sample and Difference Circuits

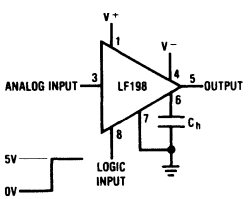
DESCRIPTION

The LF198 is a precision sample and hold amplifier which uses a combination of bipolar and junction FET transistors to provide precision, high speed, and long hold times. A typical offset voltage of 1mV and gain error of 0.002% allow this sample and hold amplifier to be used in 12-bit systems. Dynamic performance can be optimized by proper selection of the external hold capacitor. Acquisition times can be as low as 4μs for small capacitors while hold step and droop errors can be held below 0.1mV and 30μV/sec respectively when using larger capacitors.

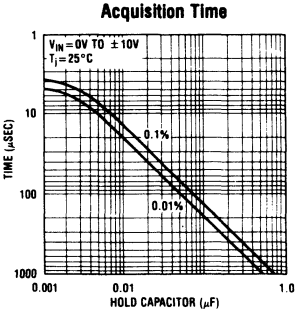
The LF198 is fixed at unity gain with $10^{10}\Omega$ input impedance independent of sample / hold mode. The logic inputs are high impedance differential to allow easy interfacing to any logic family without ground loop problems. A separate offset adjust pin can be used to zero the offset voltage in either the sample or hold mode. Additionally, the hold capacitor can be driven with an external signal to provide precision level shifting or "differencing" operation. The device will operate over a wide supply voltage range from $\pm$5V to $\pm$18V with very little change in performance, and key parameters are specified over this full supply range.

The LF198A version offers tightened electrical specifications for key parameters.

Basic Sample and Hold



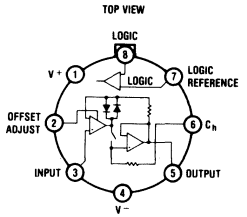
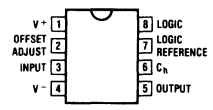
Acquisition Time



ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... Equal to Supply Voltage
Logic to Logic Reference Differential
Voltage (Note 2) ..... +30V, −30V
Output Short Circuit Duration ..... Indefinite
Hold Capacitor Short Circuit Duration ..... 10 sec
Lead Temperature (Soldering, 10 seconds) ..... 300°C
Supply Voltage ..... ±18V
Power Dissipation (Package Limitation)
(Note 1) 500mW
Operating Temperature Range
LF198/LF198A ..... −55°C to 125°C
LF398/LF398A ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
TOP VIEW  L PACKAGE METAL CAN	LF198AL LF198L LF398AL LF398L
TOP VIEW  JG PACKAGE HERMETIC DIP P PACKAGE PLASTIC DUAL IN LINE	LF398JG LF398AP LF398P

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LF198A MIN	LF198A TYP	LF198A MAX	LF398A MIN	LF398A TYP	LF398A MAX	UNITS
Input Offset Voltage (Note 6)		 •		0.5	1 2		1	2 3	mV mV
Input Bias Current (Note 6)		 •		5	25 75		10	25 50	nA nA
Input Impedance				10^{10}			10^{10}		Ω
Gain Error	$R_L = 10k$	 •		0.001	0.005 0.01		0.001	0.005 0.01	% %
Feedthrough Attenuation Ratio at 1kHz	$C_h = 0.01\mu F$		86	96		86	96		dB
Output Impedance	"HOLD" Mode	 •		0.5	1 4		0.5	1 6	Ω Ω
"HOLD" Step (Note 4)	$C_h = 0.01\mu F$, $V_{OUT} = 0$			0.25	1		0.25	1	mV
Supply Current (Note 6)	$T_j \geq 25°C$			4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current				2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	"HOLD" Mode (Note 5)			10	100		10	100	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000pF$ $C_h = 0.01\mu F$			4 16	6 25		4 16	6 25	μs μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$			5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$		90	110		90	110		dB
Differential Logic Threshold			0.8	1.4	2.4	0.8	1.4	2.4	V

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LF198 MIN	LF198 TYP	LF198 MAX	LF398 MIN	LF398 TYP	LF398 MAX	UNITS
Input Offset Voltage (Note 6)				1	3		2	7	mV
		•			5			10	mV
Input Bias Current (Note 6)				5	25		10	50	nA
		•			75			100	nA
Input Impedance				10^{10}			10^{10}		Ω
Gain Error	$R_L = 10k$			0.002	0.005		0.004	0.01	%
		•			0.02			0.02	%
Feedthrough Attenuation Ratio at 1kHz	$C_h = 0.01\mu F$		86	96		80	96		dB
Output Impedance	"HOLD" Mode			0.5	2		0.5	4	Ω
		•			4			6	Ω
"HOLD" Step (Note 4)	$C_h = 0.01\mu F$, $V_{OUT} = 0$			0.5	2.0		0.5	2.5	mV
Supply Current (Note 6)	$T_j \geq 25°C$			4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current				2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	"HOLD" Mode (Note 5)			30	100		30	200	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000pF$			4			4		μs
	$C_h = 0.01\mu F$			16			16		μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$			5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$		80	110		80	110		dB
Differential Logic Threshold			0.8	1.4	2.4	0.8	1.4	2.4	V

The • denotes the specifications which apply over the full operating temperature range.

Note 1: T_j max for the LF198/LF198A is 150°C; T_j max for the LF398/LF398A is 100°C.

Note 2: The logic inputs are protected to ±30V differential as long as the voltage on both pins does not exceed the supply voltage. For proper operation, however, both logic and logic reference pins must be at least 2V below the positive supply and one of these pins must be at least 3V above the negative supply.

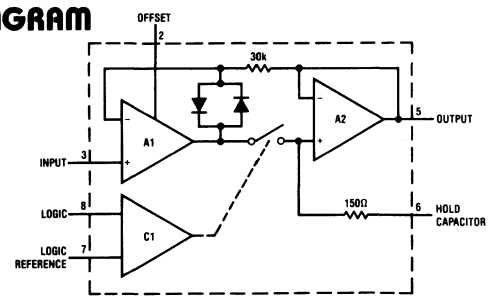
Note 3: Unless otherwise noted, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, $R_L = 10k\Omega$ and unit is in "sample" mode. Logic reference = 0V and logic voltage = 2.5V.

Note 4: The hold step is sensitive to stray capacitance coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a *junction* temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is tested over full input signal range.

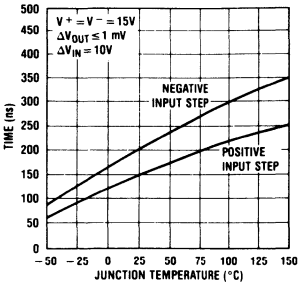
Note 6: These parameters are tested over a supply voltage range of ±5V to ±18V.

FUNCTIONAL DIAGRAM



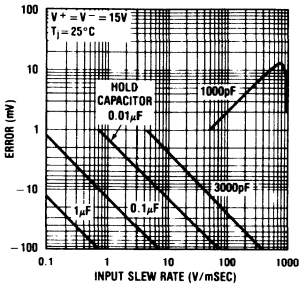
TYPICAL PERFORMANCE CHARACTERISTICS

Aperture Time*



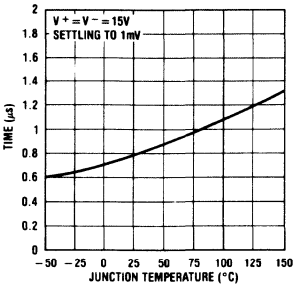
*See Definition of Terms

Dynamic Sampling Error*



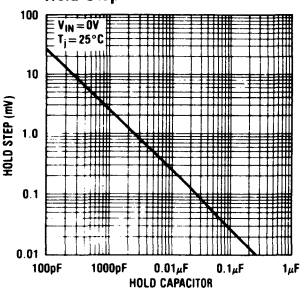
*See Definition of Terms

"Hold" Settling Time*

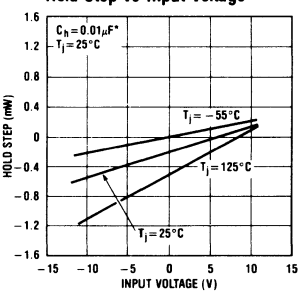


*See Definition of Terms

Hold Step

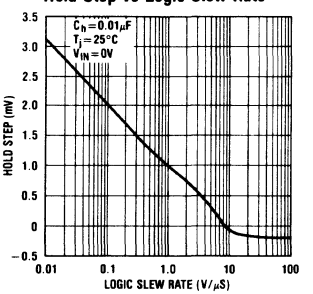


Hold Step vs Input Voltage

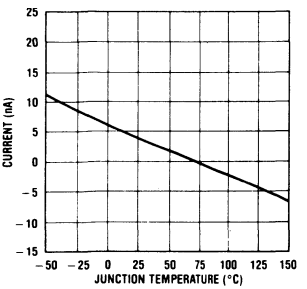


*Amplitude of hold step scales inversely with hold capacitor value

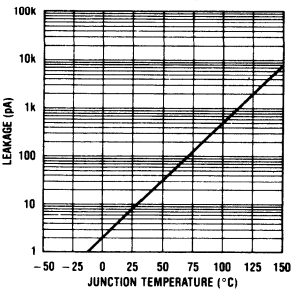
Hold Step vs Logic Slew Rate



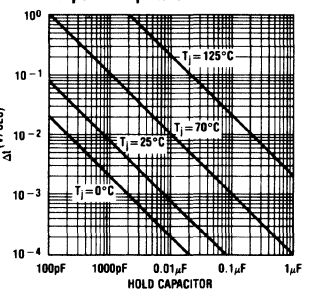
Input Bias Current



Capacitor Pin Leakage

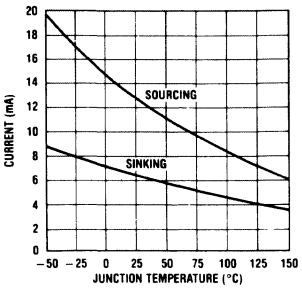


Output Droop Rate

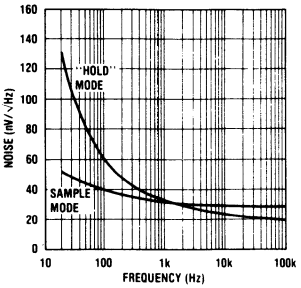


TYPICAL PERFORMANCE CHARACTERISTICS

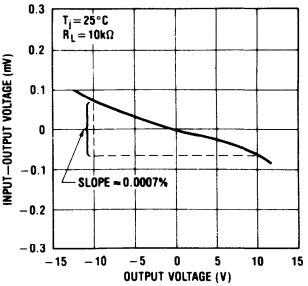
Output Short Circuit Current



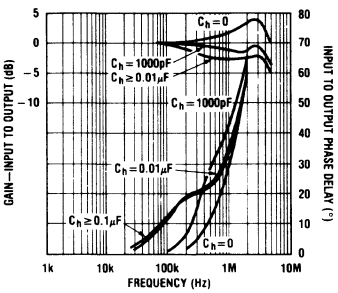
Output Noise



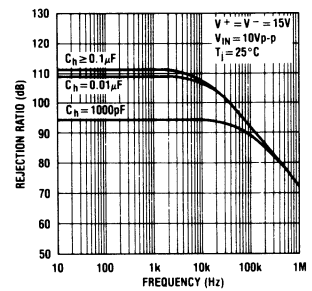
Gain Error



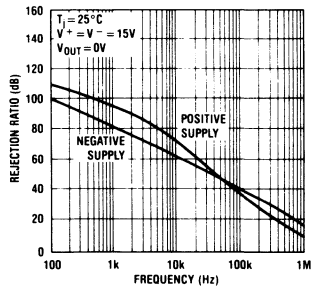
Phase and Gain (Input to Output, Small Signal)



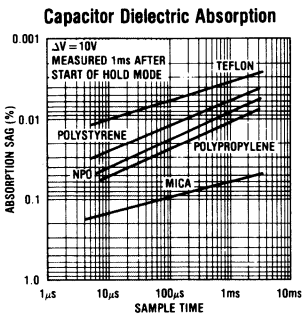
Feedthrough Rejection Ratio



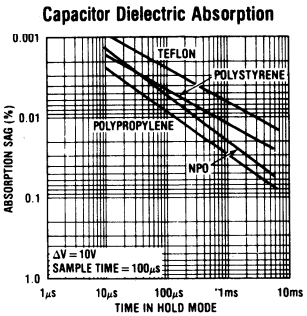
Power Supply Rejection



Capacitor Dielectric Absorption

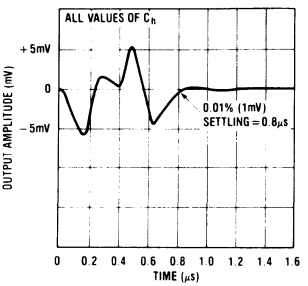


Capacitor Dielectric Absorption

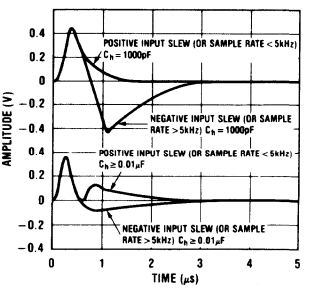


TYPICAL PERFORMANCE CHARACTERISTICS

Output Transient at Start of Hold Mode



Output Transient at Start of Sample Period



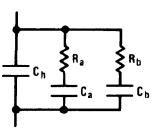
APPLICATIONS INFORMATION

Hold Capacitor

For fast sample and hold applications, the size of the hold capacitor is critical. A low value will give fast acquisition, but will also increase errors due to hold step, and droop caused by amplifier bias current. The capacitor should be made as large as possible, consistent with acquisition time and dynamic sampling error requirements. Capacitors larger than 0.1μF have an additional problem. They are generally not available in the low loss dielectrics like Teflon, Polystyrene, and NPO, at least not at a reasonable price and size. Mylar, even with its poor dielectric absorption properties, may be a reasonable choice where very long sample times are used and low droop rates are needed.

Dielectric absorption in the hold capacitor can often be the major source of error in a sample and hold. The equivalent "circuit" of a typical capacitor is shown below with parallel RC networks used to model dielectric absorption.

Typical Hold Capacitor Equivalent Circuit



C_a, $C_b \approx 0.01$ TO 0.1 C_h
R_a, R_b GENERATE TIME CONSTANTS OF 0.1-50 MILLISECONDS WITH C_a, C_b

One can see that rapid changes in capacitor voltage will not be tracked by the internal parasitic capacitors because of the resistance in series with them. This leads to a "sag" effect in the hold capacitor after a sudden change in voltage followed by rapid switch to the hold mode. The capacitor remembers its previous state via the charge on the internal parasitic capacitance and sags

APPLICATIONS INFORMATION

back slightly toward the previous voltage. The magnitude of the sag depends on the voltage change and the time spent sampling the new voltage. Several time constants are typically evident in the sag, although some capacitors tend to exhibit a single time constant, while others show a sag that indicates a blending of many time constants. The curves labeled CAPACITOR DIELECTRIC ABSORPTION show the amount of sag found after a 10V step with sample time at the new voltage and hold time at the new voltage as variables. It is obvious that sag problems are minimized by long sample times and short hold times. This is often in conflict with basic sampling requirements, but one point should be made: if at all possible, keep the sample and hold amplifier in the "tracking", or sampling, mode as much as possible to maximize the time the hold capacitor spends near the voltage at which it will eventually "hold".

The best capacitor for sample and hold applications is Teflon. It is clearly superior with regard to dielectric absorption and operates over the full −55°C to 125°C temperature range. If size or price becomes a problem, the second choice for full temperature range operation is "NPO", or "COG" ceramic units. Some care must be used here—not all NPO capacitors use the low dielectric constant ceramic necessary for low dielectric absorption. For lower temperatures ($\leq$70°C), Polystyrene has traditionally been the best hold capacitor. The best units are cylindrical and fairly large—there seems to be a strong correlation between small size and poorer dielectric performance. Polypropylene has nearly the same absorption properties as polystyrene and offers 85°C operation. It also tends to be smaller. Again, stay with cylindrically wrapped units. Other standard dielectrics such as mica, glass, mylar, and ordinary ceramic are much worse with regard to dielectric absorption. Mylar is sometimes used for large values when the ratio of sample to hold time is large and extremely low droop is required.

Dynamic Sampling Error

A significant sampling error can occur in any sample and hold if the input is moving when the unit is put into the hold mode. The two major causes for this error are digital delay in switch opening and analog delay across the hold capacitor. The switch opening delay is obvious and leads to a "held" output error of $(dv/dt) \times (T_d)$, where dv/dt is the slew rate of the input signal and T_d is switch delay. In the case of the LF198, T_d is approximately 150ns, giving a 4.5mV error when sampling the zero crossing of a 5V (peak) sine wave at 1kHz ($dv/dt = A \cdot 2\pi f = 5 \cdot 2\pi \cdot 10^3$). The analog delay is the difference between input signal and capacitor voltage. It is determined by the RC product of the hold capacitor and the effective series resistance, which in the case of the LF198 is about 150Ω. This analog delay with a 0.01μF hold capacitor is $R \cdot C = 150 \times 10^{-8} = 1.5\mu s$, or about ten times the delay of the switch. The sign of the analog delay is negative—the held output is related in time to the input voltage *before* the hold command was given. The overall dynamic sampling error is the sum of the digital and analog errors. The curve labeled *Dynamic Sampling Error* will be helpful in estimating these errors as a function of input slew rate and hold capacitor size.

Dynamic sampling error can be reduced by a factor of ten or more by inserting a delay in the logic input so that the "hold" command is delayed by an amount equal to the RC time constant of the LF198 and external hold capacitor. For a 0.01μF hold capacitor and the 150Ω resistor internal to the LF198, this is 1.5μs. A simple RC network can be used in front of the logic input for delays up to $\approx$1μs. Longer delays require the addition of a logic gate to speed up the rise time of the delayed signal. See LOGIC RISE TIME in this section for further details.

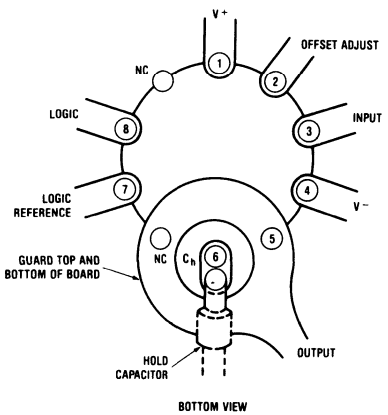
Hold Step

Hold step is the small voltage step (after settling) seen at the output of a sample and hold amplifier when it is switched from the sample mode to the hold mode with a steady DC input. Hold step is typically the result of, or can be modeled as, a fixed quantity of charge transferred to the hold capacitor as a result of the internal switching that occurs during the hold command. In the case of the LF198, that charge is about 5 picocoulombs, giving a hold step of 0.5mV for a 0.01μF hold capacitor and 5mV for a 1000pF hold capacitor. ($V = Q/C$.) Hold step is reasonably independent of logic amplitude if care is taken to minimize the stray capacitance between the logic input

APPLICATIONS INFORMATION

and the hold capacitor. With thoughtful layout, including the guarding technique shown below, stray capacitance should be under 0.3pF, limiting charge variations to less than 0.3 picocoulombs per volt.

Guarding Technique



Use 10-pin layout. Guard around C_h is tied to output.

Hold step varies slightly with analog input voltage (see curves). A typical unit will change at 0.4 picocoulombs per volt. This manifests itself as a gain error when the amplifier is switched to the hold mode. With a 0.01μF capacitor, the resulting gain error will be (0.4 PC/V)/0.01μF = 0.004%. This gain error is in the opposite direction of DC (sample mode) gain error. At high values of hold capacitor, DC gain error will dominate and gain will be slightly below unity (0.002%). For low value capacitors (< 0.01μF), hold step induced gain error will dominate and hold mode gain will be slightly above unity. Zeroing out hold step does not change the variation of hold step with regard to input voltage.

Offset Zeroing

A sample and hold amplifier has two distinct offset voltages. The first is just the DC offset of the amplifier while in the sample or "tracking" mode. It is identical to the input offset of any operational amplifier. The second offset voltage is the sum of the DC offset plus a dynamic term called hold step. Hold step is a change in output voltage when the amplifier is switched from sample mode to hold mode, with the input held steady. This second offset is often called hold mode offset. It can be less than or much greater than the DC offset, depending on the magnitude and sign of hold step.

A fairly accurate model for hold step is a fixed charge injected into the hold capacitor by the switch turn-off circuitry. The magnitude of the charge is reasonably independent of logic input amplitude. The resulting change in hold capacitor voltage is Q/C_h. The charge, Q, is typically 5 picocoulombs, giving a 0.5mV hold step with a 0.01μF hold capacitor. Since most sample and hold amplifiers are "used," i.e., have their outputs read by an A to D converter, etc., during the hold mode, hold mode offset is arguably much more important than sample mode DC offset.

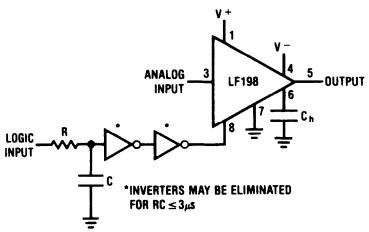
DC offset adjustment is accomplished with a 1k low TC cermet potentiometer tied to V^+ with 0.6mA flowing through it and the wiper tied to pin 2. This allows pin 2 to be moved $\pm$300mV around its nominal voltage (0.3V below V^+). Offset adjustment range is $\pm$9mV, and the adjustment procedure nominally improves offset drift when the DC offset is reduced to zero. This offset method *can* be used to zero out hold mode offset, but at the expense of some induced offset drift. Each millivolt of hold step offset that is corrected by this method introduces 3.3μV/°C drift. For 0.002μF or larger hold capacitors where hold step is a few millivolts or less, this is a practical solution to hold mode offset. In precision wide temperature range applications, or where C_h is less than 0.002μF, a separate hold mode zeroing method should be used. The circuit shown in the application section using a logic inverter and a 5pF capacitor is recommended (DC AND AC ZEROING).

APPLICATIONS INFORMATION

Logic Fall Time

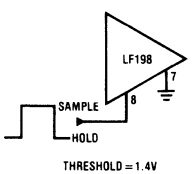
Hold step is independent of logic input fall time only for fall times faster than 10V/μs. For instance, as logic fall time changes from 10V/μs to 1V/μs, hold step with a 0.01μF hold capacitor will typically increase from 0.25mV to 1.0mV. See the curve labeled HOLD STEP vs LOGIC SLEW RATE for further data points. If logic slew rate is not constant, use the value at the threshold point (1.5V with respect to logic reference). An RC network will have a discharge slew rate of V_L/RC, where V_L is the logic threshold of the LF198. The delay generated by the network will be $RC \cdot \ln(V^+/V_L)$, where V^+ is logic amplitude. For a 1μs delay, with 5V logic, an RC time constant of 0.8μs is needed. This has a slew rate of 2V/μs at threshold, which will slightly degrade hold step. It is obvious that an RC delay network significantly longer than 1μs will have a large effect on hold step. If longer delays are required, they should be followed by several inverter stages or a Schmitt trigger to increase slew rate.

Adding Delay to Logic Input

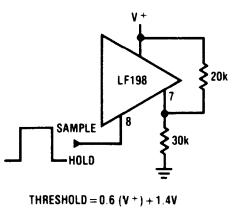


LOGIC INPUT CONFIGURATIONS*

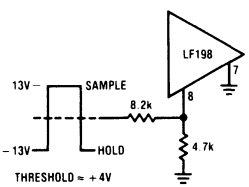
TTL and CMOS
$3V \le V_L$ (Hi State) $\le 10V$

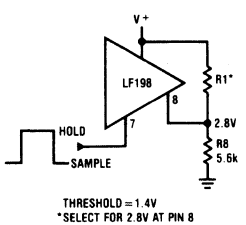


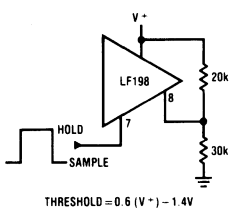
CMOS
$7V \le V_L$ (Hi State) $\le 15V$

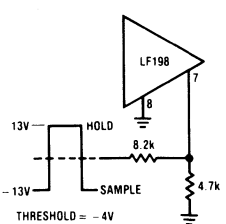


Op Amp Drive





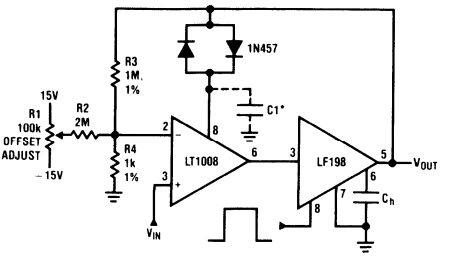




*The logic input signal high state must be at least 2V below the positive supply voltage of the LF198.

TYPICAL APPLICATIONS

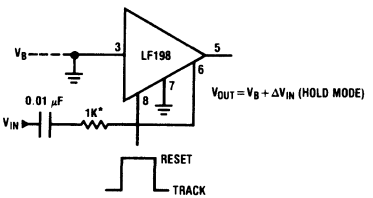
X1000 Sample and Hold



*FOR LOWER GAINS, THE LT1008 MUST BE FREQUENCY COMPENSATED

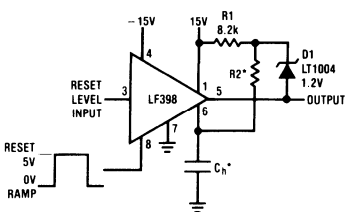
USE $\approx \frac{100}{A_V}$ pF FROM COMP 2 TO GROUND

Sample and Difference Circuit (Output Follows Input in Hold Mode and Resets to V_B in Sample Mode)



*THIS RESISTOR PROTECTS INPUT FROM SURGE CURRENTS, BUT INCREASES SAMPLE TIME. IT CAN BE ELIMINATED IF INPUT IS OTHERWISE PROTECTED.

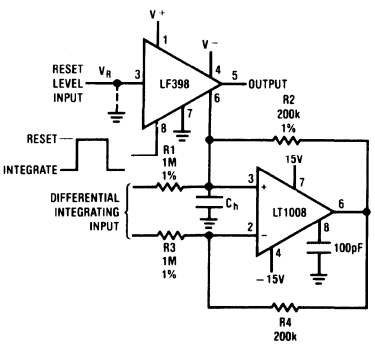
Ramp Generator with Variable Reset Level



*SELECT FOR RAMP RATE $\frac{\Delta V}{\Delta T} = \frac{1.2V}{(R2)C_h)}$

$R \geq 10k$

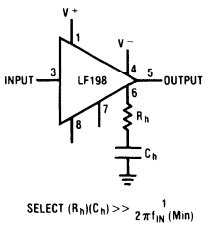
Integrator with Programmable Reset Level



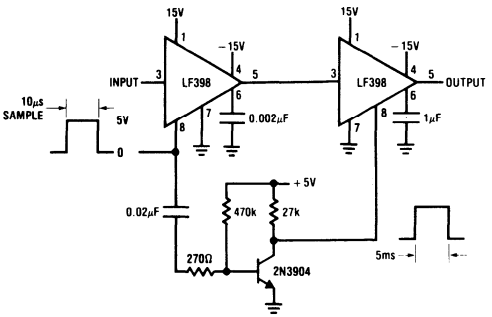
$V_{OUT}\,(HOLD\ MODE) = \left[\frac{1}{(R1)C_h}\int_0^t V_{IN}dt\right] + \left[V_R\right]$

TYPICAL APPLICATIONS

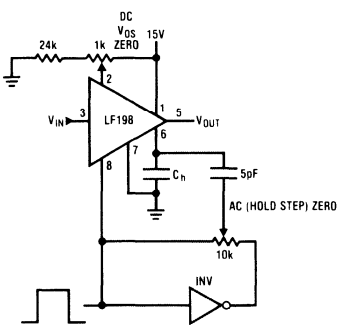
Output Holds at Average of Sampled Input



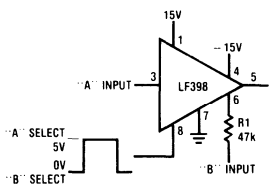
Fast Acquisition, Low Droop Sample and Hold



DC and AC Zeroing



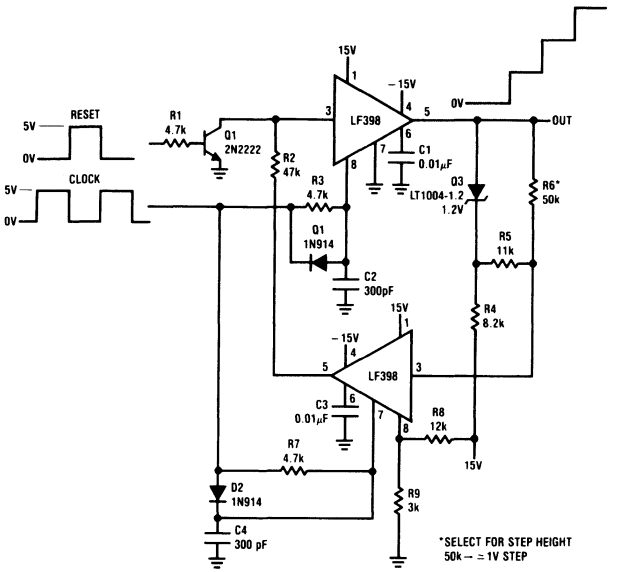
2-Channel Switch



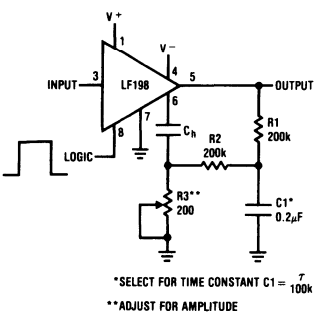
	A	B
Gain	1 ± 0.02%	1 ± 0.2%
Z_{IN}	$10^{10}\Omega$	47kΩ
BW	≃ 1MHz	≈ 400kHz
Crosstalk @1kHz	−90dB	−90dB
Offset	≤ 6mV	≤ 75mV

TYPICAL APPLICATIONS

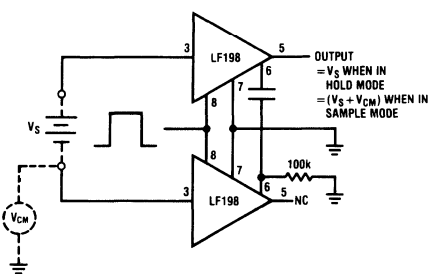
Staircase Generator



Capacitor Hysteresis Compensation

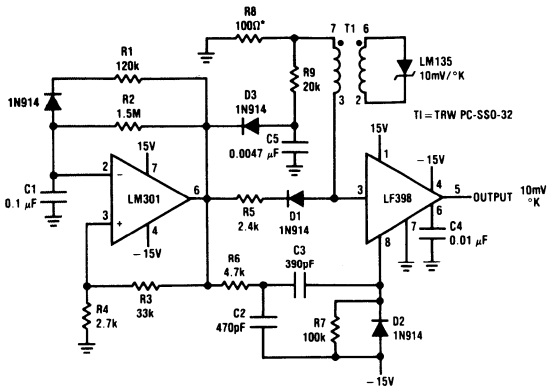


Differential Hold



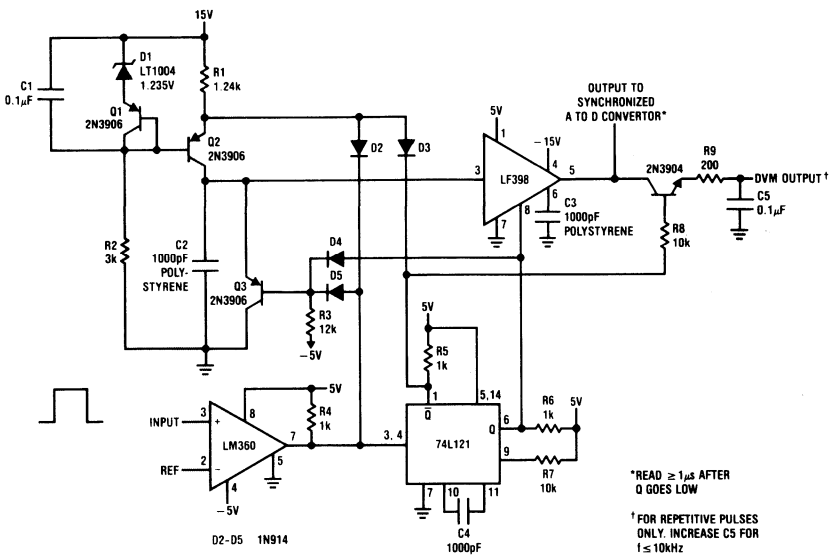
TYPICAL APPLICATIONS

Isolated Temperature Sensor



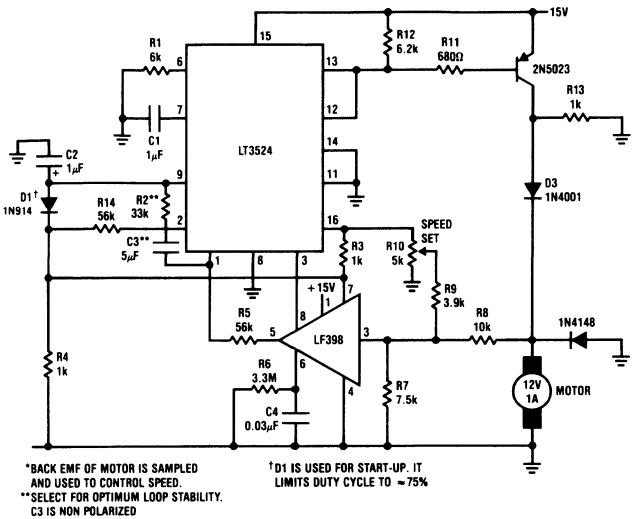
*COMPENSATES FOR TRANSFORMER RESISTANCE. SELECT FOR FLAT OUTPUT FROM LF198 WHILE IN SAMPLE MODE.

Pulse Width to Voltage Converter



TYPICAL APPLICATIONS

Motor Speed Controller Needs No Tachometer*



*BACK EMF OF MOTOR IS SAMPLED AND USED TO CONTROL SPEED.
**SELECT FOR OPTIMUM LOOP STABILITY. C3 IS NON POLARIZED

†D1 IS USED FOR START-UP. IT LIMITS DUTY CYCLE TO ≈75%

DEFINITION OF TERMS

Hold Step: The voltage step at the output of the amplifier when switching from sample mode to hold mode with a constant analog input voltage and a logic swing of 5V.

Acquisition Time: The time required to acquire, within a defined error, a new analog input voltage with an output change of 10V. Acquisition time includes output settling time and includes the time required for all internal nodes to settle so that the output is at the proper value when switched to the hold mode.

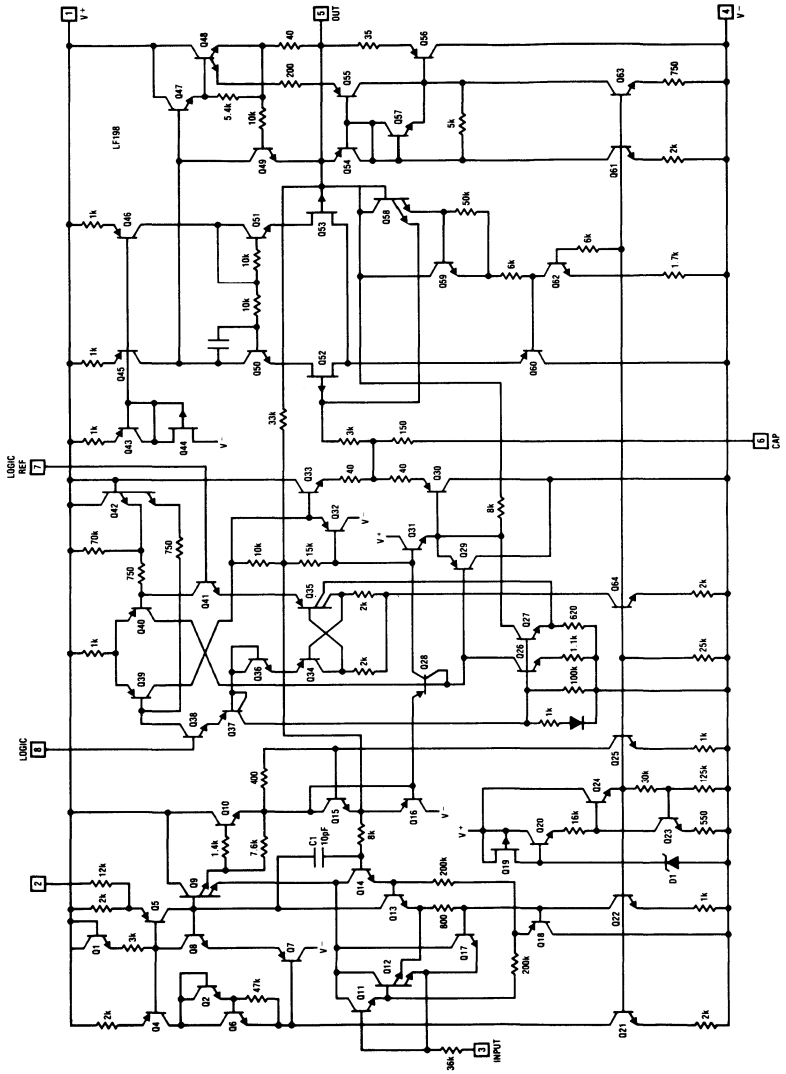
Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold Settling Time: The time required for the output to settle within 1mV of final value after a hold command is initiated.

Dynamic Sampling Error: The error introduced into the held output voltage due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

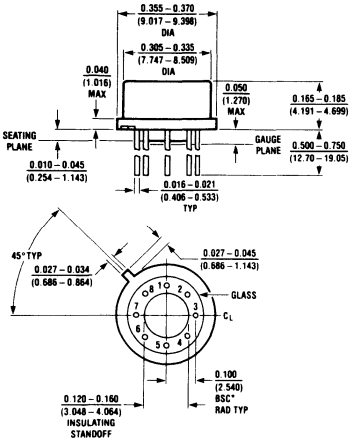
Aperture Time: The delay required between "Hold" command and an input analog transition, so that the transition does not affect the held output.

SCHEMATIC DIAGRAM



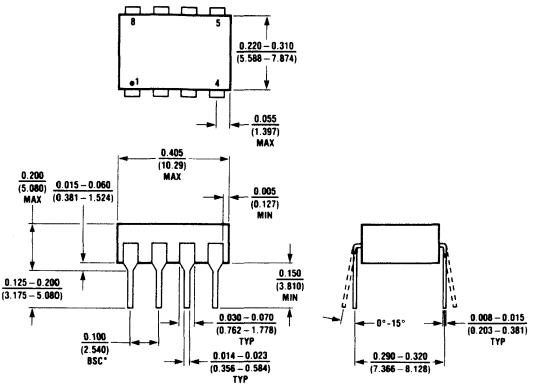
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

L Package
Metal Can



	$T_j$max	θ_{ja}	θ_{jc}
LF198/LF198A	150°C	150°C/W	45°C/W
LF398/LF398A	100°C	150°C/W	45°C/W

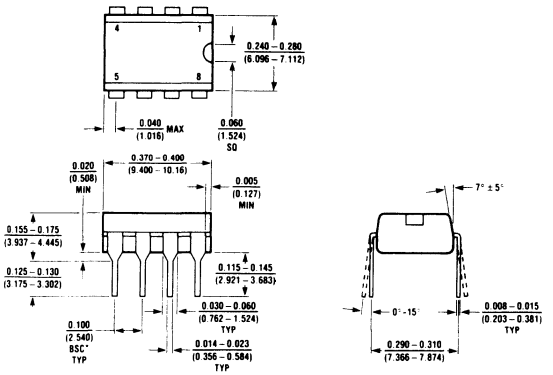
JG Package
8 Lead Hermetic DIP



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

	$T_j$max	θ_{ja}
LF398	100°C	100°C/W

P Package
8 Lead Plastic



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

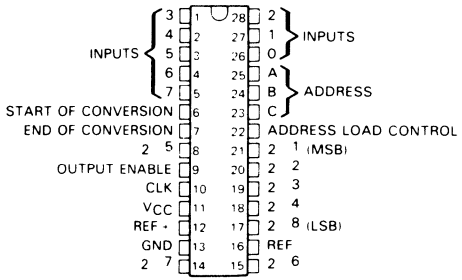
	$T_j$max	θ_{ja}
LF398/LF398A	100°C	130°C/W

TL0808, TL0809
LOW-POWER CMOS ANALOG-TO-DIGITAL CONVERTERS WITH 8-CHANNEL MULTIPLEXERS

DECEMBER, 1984

- **Total Unadjusted Error...± 1/2 LSB Typ for TL0808 and ± 1 LSB Typ for TL0809 Over Temperature Range**
- **Ideal for Battery Operated, Portable Instrumentation Applications**
- **Resolution of 8 Bits**
- **100 μs Conversion Time**
- **Ratiometric Conversion**
- **Guaranteed Monotonicity**
- **No Missing Codes**
- **Easy Interface with Microprocessors**
- **Latched 3-State Outputs**
- **Latched Address Inputs**
- **Single 3-Volt Supply**
- **Extremely Low Power Consumption...0.3 mW Typ**
- **Improved Direct Replacement for ADC0808 and ADC0809**

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



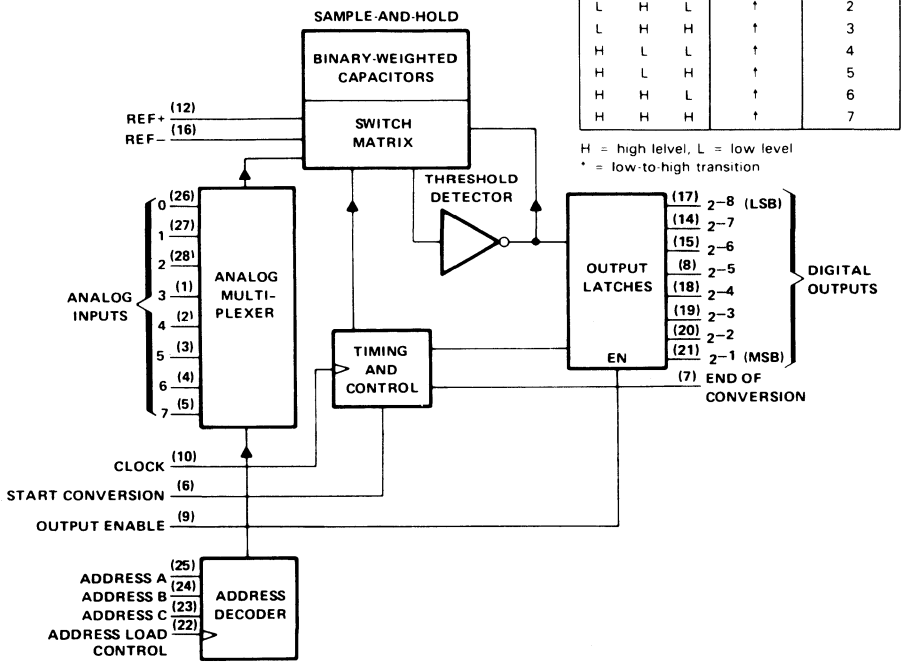
description

The TL0808 and TL0809 are monolithic CMOS devices with an 8-channel multiplexer, an 8-bit analog-to-digital (A/D) converter, and microprocessor-compatible control logic. The 8-channel multiplexer can be controlled by a microprocessor through a 3-bit address decoder with address load to select any one of eight single-ended analog switches connected directly to the comparator. The 8-bit A/D converter uses the successive-approximation conversion technique featuring a high-impedance threshold detector, a switched-capacitor array, a sample-and-hold, and a successive-approximation register (SAR).

The comparison and converting methods used eliminate the possibility of missing codes, nonmonotonicity, and the need for zero or full-scale adjustment. Also featured are latched 3-state outputs from the SAR and latched inputs to the multiplexer address decoder. The single 3-volt supply and extremely low power requirements make the TL0808 and TL0809 especially useful for a wide variety of applications including portable battery and LCD applications. Ratiometric conversion is made possible by access to the reference voltage input terminals.

The TL0808 and TL0809 are characterized for operation from -40°C to 85°C.

functional block diagram (positive logic)

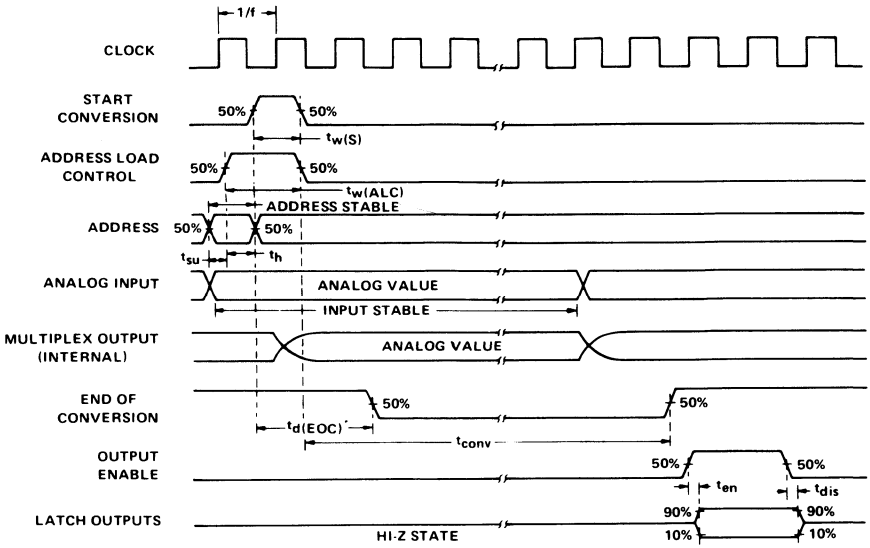


MULTIPLEXER FUNCTION TABLE

INPUTS				SELECTED
ADDRESS			ADDRESS	ANALOG
C	B	A	STROBE	CHANNEL
L	L	L	↑	0
L	L	H	↑	1
L	H	L	↑	2
L	H	H	↑	3
H	L	L	↑	4
H	L	H	↑	5
H	H	L	↑	6
H	H	H	↑	7

H = high lelvel, L = low level
↑ = low-to-high transition

operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 6.5 V
Input voltage range: control inputs ..... −0.3 to 15 V
all other inputs ..... −0.3 V to V_{CC} + 0.3 V
Operating free-air temperature range ..... −40°C to 85°C

NOTE: 1. All voltage values are with respect to the network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage V_{CC}	2.75	3	5.5	V
Positive reference voltage, V_{ref+} (see Notes 2, 3, and 4)	2.75	V_{CC}	V_{CC}+0.1	V
Negative reference voltage, V_{ref-} (see Notes 2, 3, and 4)		0	−0.1	V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 4)		3		V
High-level input voltage, control inputs, V_{IH}	0.7 V_{CC}			V
Low-level input voltage, control inputs, V_{IL}			0.3 V_{CC}	V
Start pulse duration, $t_{w(S)}$	200			ns
Address load control pulse width, $t_{w(ALC)}$	200			ns
Address setup time, t_{su}	50			ns
Address hold time, t_h	50			ns
Clock frequency, f_{clock}	10	640	1280	kHz
Operating free-air temperature, T_A (see Note 4)	−40		85	°C

NOTES: 2. The accuracy of the conversion will depend on the stability of the reference voltages applied.
3. Analog voltages greater than or equal to V_{ref+} convert to all highs, and all voltages less than V_{ref-} convert to all lows.
4. For proper operation of the TL0808 and TL0809 at free-air temperatures below 0°C, V_{CC} and (V_{ref+} - V_{ref-}) should not be less than 3 volts.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 3 V to 5.25 V (unless otherwise noted)

total device

	PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_O = −360 μA	V_{CC} −0.4			V
V_{OL}	Low-level output voltage	Data outputs	I_O = 1.6 mA			0.4	V
		End of conversion	I_O = 1.2 mA			0.4	
I_{OZ}	Off-state (high-impedance-state) output current		V_O = 5 V			1	μA
			V_O = 0			−1	
I_I	Control input current at maximum input voltage		V_I = 15 V			1	μA
I_{IL}	Low-level control input current		V_I = 0			−1	μA
I_{CC}	Supply Current		f_{clock} = 640 kHz		10	50	μA
C_i	Input capacitance, control inputs		T_A = 25°C		10	15	pF
C_c	Output capacitance, data outputs		T_A = 25°C		10	15	pF
	Resistance from pin 12 to pin 16			1	1000		kΩ

analog multiplexer

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{on}	Channel on-state current (see Note 5)	V_I = 3 V,	f_{clock} = 640 kHz			2	μA
		V_I = 0 V,	f_{clock} = 640 kHz			−2	
I_{off}	Channel off-state current	V_{CC} = 3 V, T_A = 25°C	V_I = 3 V		10	200	nA
			V_I = 0		−10	−200	
		V_{CC} = 3 V	V_I = 3 V			1	μA
			V_I = 0			−1	

†Typical values are at V_{CC} = 3 V and T_A = 25°C.

NOTE 5: Channel on-state current is primarily due to the bias current into or out of the threshold detector, and it varies directly with clock frequency.

operating characteristics, T_A = 25°C, V_{CC} = 3 V, V_{REF+} = 3 V, V_{REF-} = 0 V, f_{clock} = 640 kHz (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	TL0808			TL0809			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
k_{SVS}	Supply voltage sensitivity	V_{CC} = V_{ref+} = 3 V to 5.25 V, T_A = −40°C to 85°C, See Note 6		±0.05			±0.05		%/V
	Linearity error (see Note 7)			±0.5			±1		LSB
	Zero error (see Note 8)			±0.5			±1		LSB
	Total unadjusted error (see Note 9)	T_A = 25°C		±0.5			±0.5		LSB
		T_A = −40°C to 85°C		±0.5	±1		±1	±1.25	
		T_A = 0°C to 70°C			±0.75			±1	
t_{en}	Output enable time	C_L = 50 pF, R_L = 10 kΩ		80	250		80	250	ns
t_{dis}	Output disable time	C_L = 10 pF, R_L = 10 kΩ		105	250		105	250	ns
t_{conv}	Conversion time	See Note 10	90	100	116	90	110	116	μs
$t_{d(EOC)}$	Delay time, end of conversion output	See Notes 10 and 11	0		14.5	0		14.5	μs

†Typical values for all except supply voltage sensitivity are at V_{CC} = 3 V, and all are at T_A = 25°C.

NOTES: 6. Supply voltage sensitivity relates to the ability of an analog-to-digital converter to maintain accuracy as the supply voltage varies. The supply and V_{ref+} are varied together and the change in accuracy is measured with respect to full-scale.
7. Linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic.
8. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale voltage.
9. Total unadjusted error is the maximum sum of linearity error, zero error, and full-scale error.
10. Refer to the operating sequence diagram.
11. For clock frequencies other than 640 kHz, $t_{d(EOC)}$ maximum is 8 clock periods plus 2 μs.

PRINCIPLES OF OPERATION

The TL0808 and TL0809 each consists of an analog singal multiplexer, and 8-bit successive-approximation converter, and related control and output circuitry.

multiplexer

The analog multiplexer selects 1 of 8 single-ended input channels as determined by the address decoder. Address load control loads the address code into the decoder on a low-to-high transition. The output latch is reset by the positive-going edge of the start pulse. Sampling also starts with the positive-going edge of the start pulse and last for 32 clock periods. The conversion process may be interrupted by a new start pulse before the end of 64 clock periods. The previous data will be lost if a new start-of-conversion occurs before the 64th clock pulse. Continuous conversion may be accomplished by connecting the End-of-Conversion output to the start input. If used in this mode an external pulse should be applied after power up to assure start up.

converter

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (Figure 1). With each successive step of the capacitor-sampling process, the initial charge is redistributed among the capacitors. The conversion process uses successive approximation, but it relies on charge redistribution rather than a successive-approximation register (and reference DAC) to count and weight the bits from MSB to LSB.

In the first phase of the conversion process, the analog input is sampled by closing switch S_C and all S_T switches, and by simultaneously charging all the capacitors to the input voltage. In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all 8 bits are identified, and then the charge-convert sequence is repeated.

In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 128). Node 128 is switched to the reference voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF −. If the voltage at the summing node is greater than the trip-point of the threshold detector (approximately one-half the V_{CC} voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to REF−. If the voltage at the summing node is less than the trip point of the threshold detector, this 128-weight capacitor remains connected to REF+ through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, the 32-weight capacitor, and so forth down the line, until all bits are counted.

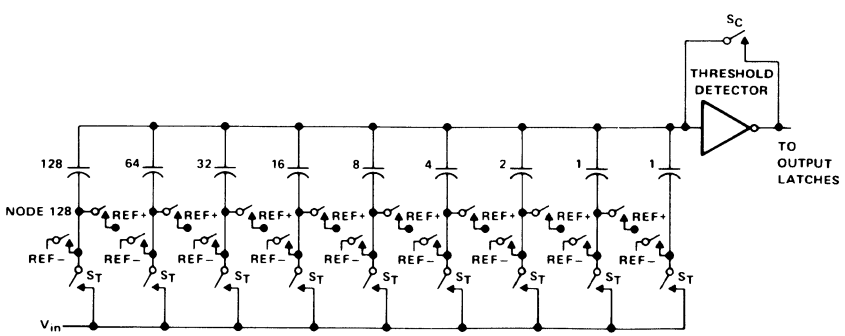


FIGURE 1. SIMPLIFIED MODEL OF THE SUCCESSIVE-APPROXIMATION SYSTEM

TYPES TL182, TL185, TL188, TL191 BI-MOS SWITCHES

D2234, JUNE 1976 – REVISED OCTOBER 1983

- Functionally Interchangeble with Siliconix DG182, DG185, DG188, and DG191 with Same Terminal Assignments
- Monolithic Construction
- Adjustable Reference Voltage
- JFET Inputs
- Uniform On-State Resistance for Minimum Signal Distortion
- ±10-V Analog Voltage Range
- TTL, MOS, and CMOS Logic Control Compatibility

description

The TL182, TL185, TL188, and TL191 are monolithic high-speed analog switches using BI-MOS technology. They comprise JFET-input buffers, level translators, and output JFET switches. The TL182 switches are SPST; the TL185 switches are SPDT. The TL188 is a pair of complementary SPST switches as is each half of the TL191.

A high level at a control input of the TL182 turns the associated switch off. A high level at a control input of the TL185 turns the associated switch on. For the TL188, a high level at the control input turns the associated switches S1 on and S2 off.

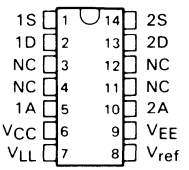
The threshold of the input buffer is determined by the voltage applied to the reference input (V_{ref}). The input threshold is related to the reference input by the equation $V_{th} = V_{ref} + 1.4$ V. Thus, for TTL compatibility, the V_{ref} input is connected to ground. The JFET input makes the device compatible with bipolar, MOS and CMOS logic families. Threshold compatibility may, again, be determined by $V_{th} = V_{ref} + 1.4$ V.

The output switches are junction field-effect transistors featuring low on-state resistance and high off-state resistance. The monolithic structure ensures uniform matching.

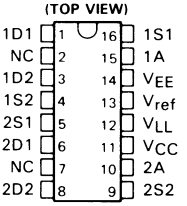
BI-MOS technology is a major breakthrough in linear integrated circuit processing. BI-MOS can have ion-implanted JFETs, p-channel MOS-FETs, plus the usual bipolar components all on the same chip. BI-MOS allows circuit designs that previously have been available only as expensive hybrids to be monolithic.

Devices with an "M" suffix are characterized for operation over the full military temperature range of −55°C to 125°C, those with an "I" suffix are characterized for operation from −25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

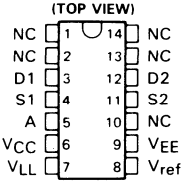
TL182
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



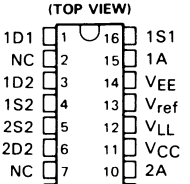
TL185
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



TL188
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



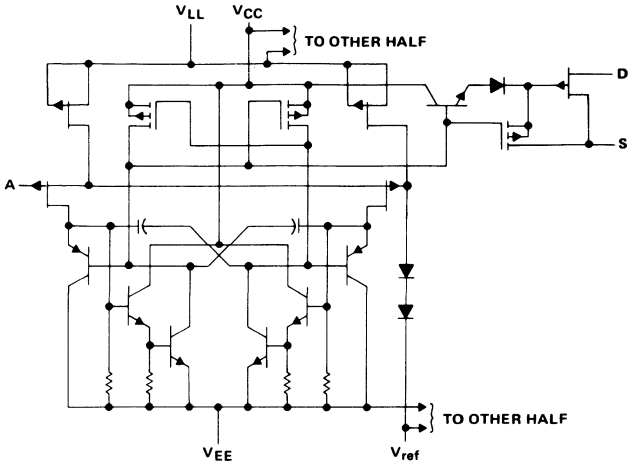
TL191
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

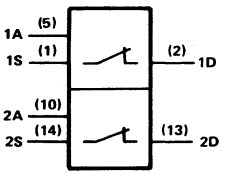


NC – No internal connection

TL182 TWIN SPST SWITCH

schematic (each channel)



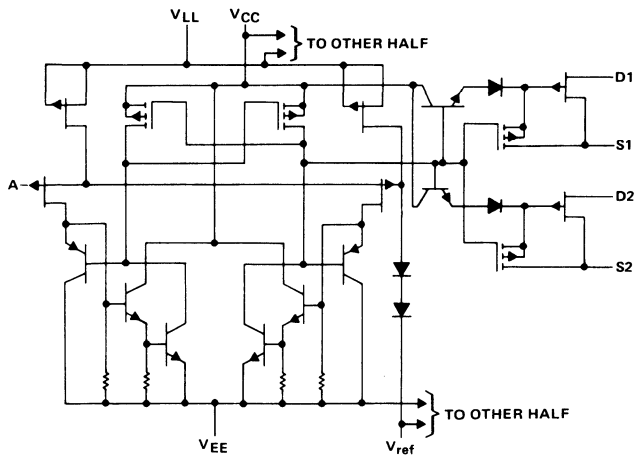


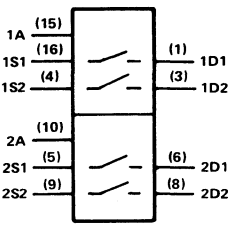
FUNCTION TABLE
(EACH HALF)

INPUT A	SWITCH S
L	ON (CLOSED)
H	OFF (OPEN)

TL185 TWIN DPST SWITCH

schematic (each channel)





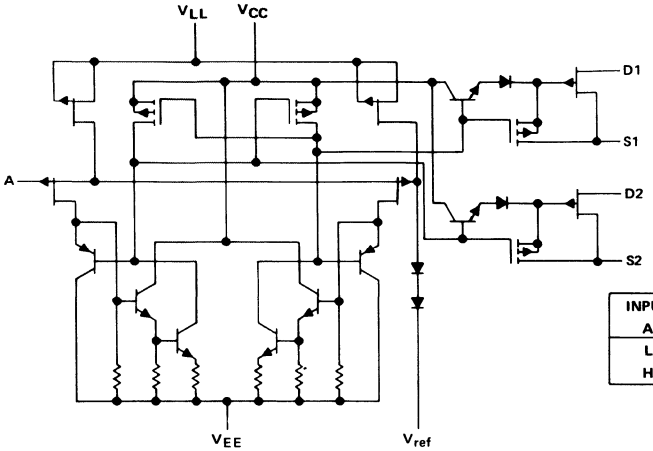
FUNCTION TABLE
(EACH HALF)

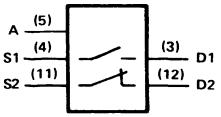
INPUT A	SWITCHES SW1 AND SW2
L	OFF (OPEN)
H	ON (CLOSED)

1283

TL188 DUAL COMPLEMENTARY SPST SWITCH

schematic



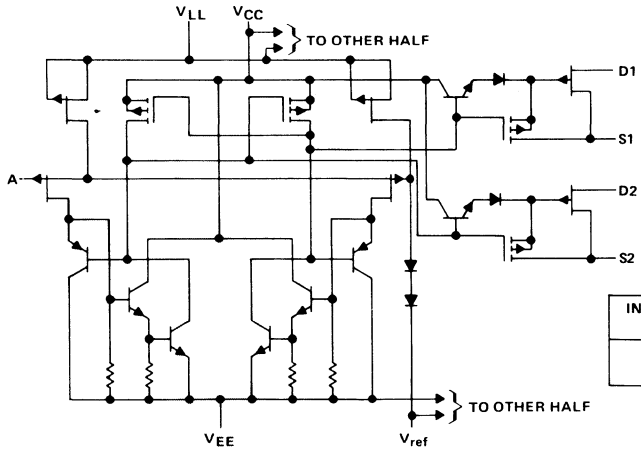


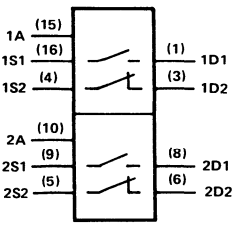
FUNCTION TABLE

INPUT	SWITCHES	
A	SW1	SW2
L	OFF (OPEN)	ON (CLOSED)
H	ON (CLOSED)	OFF (OPEN)

TL191 TWIN DUAL COMPLEMENTARY SPST SWITCH

schematic (each channel)



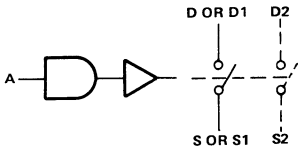


FUNCTION TABLE

INPUT	SWITCHES	
A	SW1	SW2
L	OFF (OPEN)	ON (CLOSED)
H	ON (CLOSED)	OFF (OPEN)

1283

functional block diagram



See the preceding two pages for operation of the switches.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Positive supply to negative supply voltage, $V_{CC} - V_{EE}$ . . . . . 36 V
Positive supply voltage to either drain, $V_{CC} - V_D$ . . . . . 33 V
Drain to negative supply voltage, $V_D - V_{EE}$ . . . . . 33 V
Drain to source voltage, $V_D - V_S$ . . . . . ±22 V
Logic supply to negative supply voltage, $V_{LL} - V_{EE}$ . . . . . 36 V
Logic supply to logic input voltage, $V_{LL} - V_I$ . . . . . 33 V
Logic supply to reference voltage, $V_{LL} - V_{ref}$ . . . . . 33 V
Logic input to reference voltage, $V_I - V_{ref}$ . . . . . 33 V
Reference to negative supply voltage, $V_{ref} - V_{EE}$ . . . . . 27 V
Reference to logic input voltage, $V_{ref} - V_I$ . . . . . 2 V
Current (any terminal) . . . . . 30 mA
Continuous dissipation at (or below) 25°C free-air temperature (see Note 1):
TL182MJ, TL185MJ, TL188MJ, TL191MJ . . . . . 1375 mW
TL182IJ, TL182CJ, TL185IJ, TL185CJ, TL188IJ, TL188CJ, TL191IJ, TL191CJ . . . . . 1025 mW
N package . . . . . 875 mW
Operating free-air temperature range: TL182M, TL185M, TL188M, TL191M . . . . −55°C to 125°C
TL182I, TL185I, TL188I, TL191I . . . . . −25°C to 85°C
TL182C, TL185C, TL188C, TL191C . . . . . 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: For operation above 25°C free-air temperature, see Dissipation Derating Curves, Section 2. In the J package, "M" suffix chips are alloy mounted, "I" and "C" suffix chips are glass mounted.

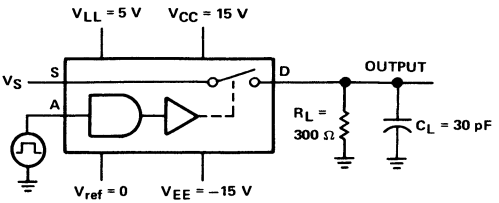
electrical characteristics, V_{CC} = 15 V, V_{EE} = −15 V, V_{LL} = 5 V, V_{ref} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TL1_M MIN	TL1_M MAX	TL1_I MIN	TL1_I MAX	TL1_C MIN	TL1_C MAX	UNIT
V_{IH}	High-level control input voltage			T_A = MIN TO MAX	$V_{ref}+2$		$V_{ref}-2$		$V_{ref}+2$		V
V_{IL}	Low-level control input voltage			T_A = MIN to MAX		$V_{ref}+0.8$		$V_{ref}+0.8$		$V_{ref}+0.8$	V
I_{IH}	High-level control input current	V_I = 5 V		T_A = 25°C		10		10		20	μA
				T_A = MAX		20		20		20	
I_{IL}	Low-level control input current	V_I = 0		T_A = MIN to MAX		−250		−250		−250	μA
$I_{D(off)}$	Off-state drain current	V_D = 10 V, V_S = −10 V, V_{IH} = 2 V, V_{IL} = 0.8 V		T_A = 25°C				5		5	nA
				T_A = MAX		100		100		100	
$I_{S(off)}$	Off-state source current	V_D = −10 V, V_S = 10 V, V_{IH} = 2 V, V_{IL} = 0.8 V		T_A = 25°C				5		5	nA
				T_A = MAX		100		100		100	
$I_{D(on)}+I_{S(on)}$	On-state channel leakage current	V_D = −10 V, V_S = −10 V, V_{IH} = 2 V, V_{IL} = 0.8 V		T_A = 25°C				−10		−10	nA
				T_A = MAX		−200		−200		−200	
$r_{DS(on)}$	Drain-to-source on-state resistance	V_D = −10 V, I_S = 1 mA, V_{IH} = 2 V, V_{IL} = 0.8 V	TL182, TL188	T_A = MIN to 25°C		75		100		100	Ω
				T_A = MAX		100		150		150	
			TL185, TL191	T_A = MIN to 25°C		125		150		150	
				T_A = MAX		250		300		300	
I_{CC}	Supply current from V_{CC}	Both control inputs at 0 V		T_A = 25°C		1.5		1.5		1.5	mA
I_{EE}	Supply current from V_{EE}					−5		−5		−5	
I_{LL}	Supply current from V_{LL}					4.5		4.5		4.5	
I_{ref}	Reference current					−2		−2		−2	
I_{CC}	Supply current from V_{CC}	Both control inputs at 5 V		T_A = 25°C		1.5		1.5		1.5	mA
I_{EE}	Supply current from V_{EE}					−5		−5		−5	
I_{LL}	Supply current from V_{LL}					4.5		4.5		4.5	
I_{ref}	Reference current					−2		−2		−2	

switching characteristics, V_{CC} = 10 V, V_{EE} = −20 V, V_{LL} = 5 V, V_{ref} = 0 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TL1_M TYP	TL1_I TYP	TL1_C TYP	UNIT
t_{on}	Turn-on time	R_L = 300 Ω, C_L = 30 pF, Figure 1	175	175	175	ns
t_{off}	Turn-off time		350	350	350	

PARAMETER MEASUREMENT INFORMATION

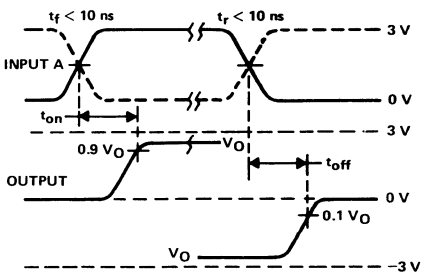


C_L includes probe and jig capacitance.

V_S = 3 V for t_{on} and −3 V for t_{off}.

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

TEST CIRCUIT



NOTE: A. The solid waveform applies for TL185 and SW1 of TL185 and TL191; the dashed waveform applies for TL182 and SW2 of TL185 and TL191.
B. V_O is the steady-state output with the switch on. Feed through via the gate capacitance may result in spikes (not shown) at the leading and trailing edges of the output waveform.

FIGURE 1–VOLTAGE WAVEFORMS

TYPES TL500C THRU TL503C ANALOG-TO-DIGITAL-CONVERTER BUILDING BLOCKS

D2477, DECEMBER 1979 – REVISED OCTOBER 1983

TL500C/TL501C ANALOG PROCESSORS

- True Differential Inputs
- Automatic Zero
- Automatic Polarity
- High Input Impedance . . . 10^9 Ohms Typically

TL500C CAPABILITIES

- Resolution . . . 14 Bits (with TL502C)
- Linearity Error . . . 0.001%
- 4 1/2-Digit Readout Accuracy with External Precision Reference

TL501C CAPABILITIES

- Resolution . . . 10-13 Bits (with TL502C)
- Linearity Error . . . 0.01%
- 3 1/2-Digit Readout Accuracy

TL502C/TL503C DIGITAL PROCESSORS

- Fast Display Scan Rates
- Internal Oscillator May Be Driven or Free-Running
- Interdigit Blanking
- Over-Range Blanking
- Display Test
- 4 1/2-Digit Display Circuitry
- High-Sink-Current Digit Driver for Large Displays

TL502C CAPABILITIES

- Compatible with Popular Seven-Segment Common-Anode Displays
- High-Sink-Current Segment Driver For Large Displays

TL503C CAPABILITIES

- Multiplexed BCD Outputs
- High-Sink-Current BCD Outputs

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

The TL500C and TL501C analog processors and TL502C and TL503C digital processors provide the basic functions for a dual-slope-integrating analog-to-digital converter.

The TL500C and TL501C contain the necessary analog switches and decoding circuits, reference voltage generator, buffer, integrator, and comparator. These devices may be controlled by the TL502C, TL503C, by discrete logic, or by a software routine in a microprocessor.

The TL502C and TL503C each includes oscillator, counter, control logic, and digit enable circuits. The TL502C provides multiplexed outputs for seven-segment displays, while the TL503C has multiplexed BCD outputs.

When used in complementary fashion, these devices form a system that features automatic zero-offset compensation, true differential inputs, high input impedance, and capability for 4 1/2-digit accuracy. Applications include the conversion of analog data from high-impedance sensors of pressure, temperature, light, moisture, and position. Analog-to-digital-logic conversion provides display and control signals for weight scales, industrial controllers, thermometers, light-level indicators, and many other applications.

principles of operation

The basic principle of dual-slope-integrating converters is relatively simple. A capacitor, C_X, is charged through the integrator from V_{CT} for a fixed period of time at a rate determined by the value of the unknown voltage input. Then the capacitor is discharged at a fixed rate (determined by the reference voltage) back to V_{CT} where the discharge time is measured precisely. The relationship of the charge and discharge values are shown below (see Figure 1).

$$V_{CX} = V_{CT} - \frac{V_I\, t_1}{R_X\, C_X} \qquad \text{Charge} \qquad (1)$$

$$V_{CT} = V_{CX} - \frac{V_{ref}\, t_2}{R_X\, C_X} \qquad \text{Discharge} \qquad (2)$$

Combining equations 1 and 2 results in:

$$\frac{V_I}{V_{ref}} = -\frac{t_2}{t_1} \qquad (3)$$

where:

V_{CT} = Comparator (offset) threshold voltage

V_{CX} = Voltage change across C_X during t_1 and during t_2 (equal in magnitude)

V_I = Average value of input voltage during t_1

t_1 = Time period over which unknown voltage is integrated

t_2 = Unknown time period over which a known reference voltage is integrated.

Equation (3) illustrates the major advantages of a dual-slop converter:

a. Accuracy is not dependent on absolute values of t_1 and t_2, but is dependent on their ratios. Long-term clock frequency variations will not affect the accuracy.
b. Offset values, V_{CT}, are not important.

The BCD counter in the digital processor (see Figure 2) and the control logic divide each measurement cycle into three phases. The BCD counter changes at a rate equal to one-half the oscillator frequency.

auto-zero phase

The cycle begins at the end of the integrate-reference phase when the digital processor applies low levels to inputs A and B of the analog processor. If the trigger input is at a high level, a free-running condition exists and continuous conversions are made. However, if the trigger input is low, the digital processor stops the counter at 20,000, entering a hold mode. In this mode, the processor samples the trigger input every 4000 oscillator pulses until a high level is detected. When this occurs, the counter is started again and is carried to completion at 30,000. The reference voltage is stored on reference capacitor C_{ref}, comparator offset voltage is stored on integration capacitor C_X, and the sum of the buffer and integrator offset voltages is stored on zero capacitor C_Z. During the auto-zero phase, the comparator output is characterized by an oscillation (limit cycle) of indeterminate waveform and frequency that is filtered and d-c shifted by the level shifter.

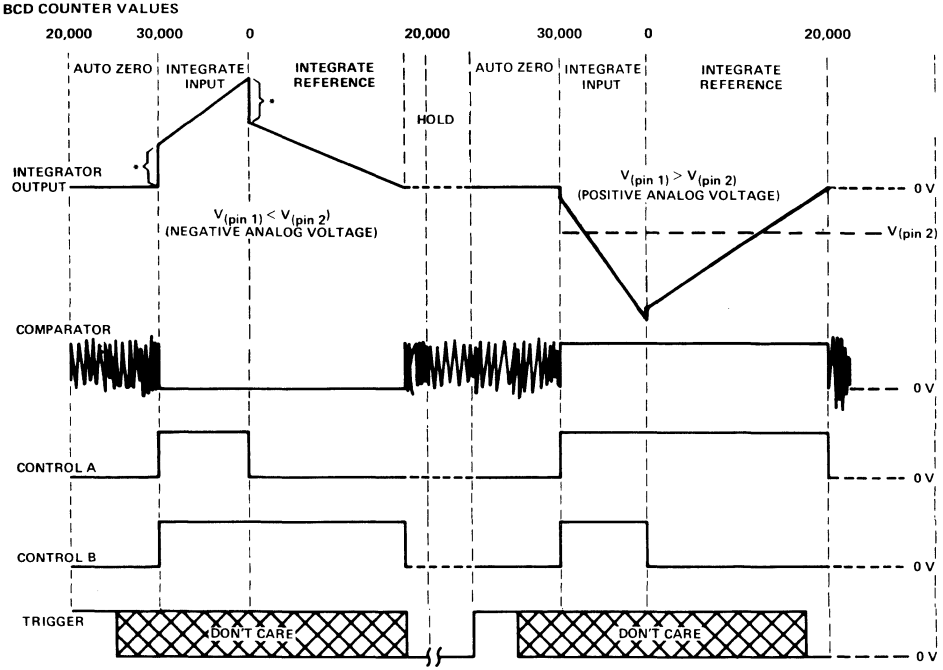
integrate-input phase

The auto-zero phase is completed at a BCD count of 30,000, and high levels are applied to both control inputs to initiate the integrate-input phase. The integrator charges C_X for a fixed time of 10,000 BCD counts at a rate determined by the input voltage. Note that during this phase, the analog inputs see only the high impedance of the noninverting operational amplifier input. Therefore, the integrator responds only to the difference between the analog input terminals, thus providing true differential inputs.

integrate-reference phase

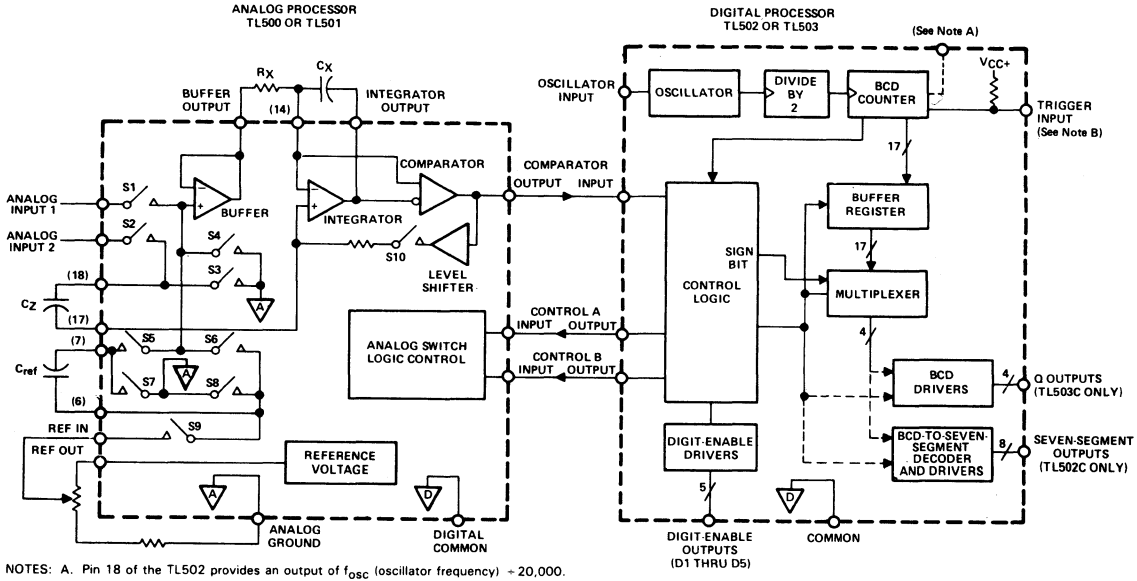
At a BCD count of 39,999 + 1 = 40,000 or 0, the integrate-input phase is terminated and the integrate-reference phase is begun by sampling the comparator output. If the comparator output is low corresponding to a negative average analog input voltage, the digital processor applies a low and a high to inputs A and B, respectively, to apply the reference voltage stored on C_{ref} to the buffer. If the comparator output is high corresponding to a positive input, inputs A and B are made high and low, respectively, and the negative of the stored reference voltage is applied to the buffer. In either case, the processor automatically selects the proper logic state to cause the integrator to ramp back toward zero at a rate proportional to the reference voltage. The time required to return to zero is measured by the counter in the digital processor. The phase is terminated when the integrator output crosses zero and the counter contents are transferred to the register, or when the BCD counter reaches 20,000 and the over-range indication is activated. When activated, the over-range indication blands all but the most significant digit and sign.

Seventeen parallel bits (4-1/2 digits) of information are strobed into the buffer register at the end of the integration phase. Information for each digit is multiplexed out to the BCD outputs (TL503C) or the seven-segment drivers (TL502C) at a rate equal to the oscillator frequency divided by 400.



*This step is the voltage at pin 2 with respect to analog ground.

FIGURE 1–VOLTAGE WAVEFORMS AND TIMING DIAGRAM



NOTES: A. Pin 18 of the TL502 provides an output of f_{osc} (oscillator frequency) ÷ 20,000.
B. The trigger input assumes a high level if not externally connected.

FIGURE 2– BLOCK DIAGRAM OF BASIC ANALOG-TO-DIGITAL CONVERTER USING TL500C OR TL501C AND TL502C OR TL503C

MODE	ANALOG INPUT	COMPARATOR	CONTROLS A AND B	ANALOG SWITCHES CLOSED
Auto Zero	X	Oscillation	L L	S3, S4, S7, S9, S10
Hold†				
Integrate Input	Positive	H	H H	S1, S2
	Negative	L		
Integrate Reference	X	H‡	H L	S3, S6, S7
		L‡	L H	S3, S5, S8

H ≡ High, L ≡ Low, X ≡ Irrelevant

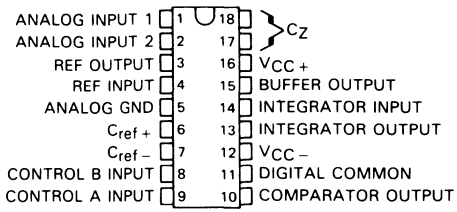
† If the trigger input is low at the beginning of the auto-zero cycle, the system will enter the hold mode. A high level (or open circuit) will signal the digital processor to continue or resume normal operation.

‡ This is the state of the comparator output as determined by the polarity of the analog input during the integrate input phase.

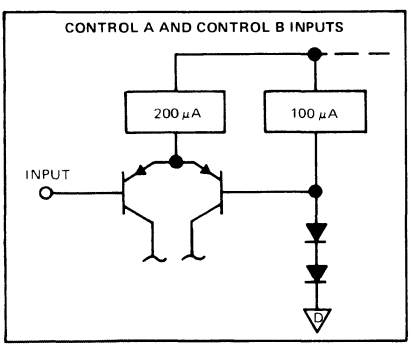
description of analog processors

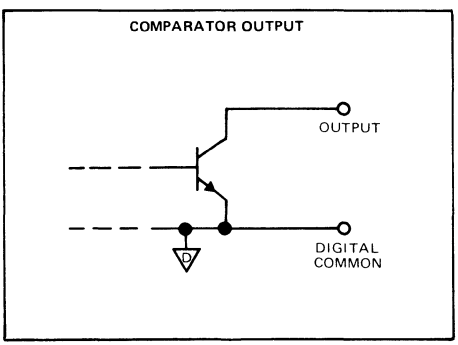
The TL500C and TL501C analog processors are designed to automatically compensate for internal zero offsets, integrate a differential voltage at the analog inputs, integrate a voltage at the reference input in the opposite direction, and provide an indication of zero-voltage crossing. The external control mechanism may be a microcomputer and software routine, discrete logic, or a TL502C or TL503C controller. The TL500C and TL501C are designed primarily for simple, cost-effective, dual-slope analog-to-digital converters. Both devices feature true differential analog inputs, high input impedance, and an internal reference-voltage source. The TL500C provides 4-1/2-digit readout accuracy when used with a precision external reference voltage. The TL501C provides 100-ppm linearity error and 3-1/2-digit accuracy capability. These devices are manufactured using TI's advanced technology to produce JFET, MOSFET, and bipolar devices on the same chip. The TL500C and TL501C are intended for operation over the temperature range of 0°C to 70°C.

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Positive supply voltage, V_{CC+} (see Note 1)	+18 V
Negative supply voltage, V_{CC-}	−18 V
Input voltage, V_I	$\pm V_{CC}$
Comparator output voltage range (see Note 2)	0 V to V_{CC+}
Comparator output sink current (see Note 2)	20 mA
Buffer, reference, or integrator output source current (see Note 2)	10 mA
Total dissipation at (or below) 25°C free-air temperature (see Note 3)	875 mW
Operating free-air temperature range	−0°C to 70°C
Storage temperature range	−65°C to 125°C

NOTES: 1. Voltage values, except differential voltages, are with respect to the analog ground common pin tied together.
2. Buffer, integrator, and comparator outputs are not short-circuit protected.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Positive supply voltage, V_{CC+}		7	12	15	V
Negative supply voltage, V_{CC-}		−9	−12	−15	V
Reference input voltage, $V_{ref(I)}$		0.1		5	V
Analog input voltage, V_I				±5	V
Differential analog input voltage, V_{ID}				10	V
High-level input voltage, V_{IH}	Control inputs	2			V
Low-level input voltage, V_{IL}	Control inputs			0.8	V
Peak positive integrator output voltage, V_{OM+}		+9			V
Peak negative integrator output voltage, V_{OM-}		−5			V
Full scale input voltage				2 V_{ref}	
Autozero and reference capacitors, C_Z and C_{ref}		0.2			μF
Integrator capacitor, C_X		0.2			μF
Integrator resistor, R_X		15		100	kΩ
Integrator time constant, R_XC_X		See Note 4			
Free-air operating temperature, T_A		0		70	°C
Maximum conversion rate with TL502 or TL503			3	12.5	conv/sec

system electrical characteristics at V_{CC} = ±12 V, V_{ref} = 1,000 ± 0.03 mV, T_A = 25°C (unless otherwise noted) (see Figure 3)

PARAMETER	TEST CONDITIONS	TL501C			TL500C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Zero error			50	300		10	30	μV
Linearity error relative to full scale	V_I = −2 V to 2 V		0.005	0.05		0.001	0.005	%FS
Full scale temperature coefficient	T_A = 0°C to 70°C		6			6		ppm/°C
Temperature coefficient of zero error	T_A = 0°C to 70°C		4			1		μV/°C
Rollover error†			200	500		30	100	μV
Equivalent peak-to-peak input noise voltage			20			20		μV
Analog input resistance	Pin 1 or 2		10^9			10^9		Ω
Common-mode rejection ratio	V_{IC} = −1 V to +1 V		86			90		dB
Current into analog input	V_I = ±5 V		50			50		pA
Supply voltage rejection ratio			90			90		dB

† Rollover error is the voltage difference between the conversion results of the full-scale positive 2 volts and the full-scale negative 2 volts.

NOTE 4. The minimum integrator time constant may be found by use of the following formula:

$$\text{Minimum } R_XC_X = \frac{V_{ID}\ (\text{full scale})\ t_1}{|V_{OM-}| - V_I(\text{pin 2})}$$

where

V_{ID} = voltage at pin with respect to pin 2

V_I(pin 2) = voltage at pin 2 with respect to analog ground

t_1 = input integration time seconds

electrical characteristics at V_{CC} = ±12 V, V_{ref} = 1 V, T_A = 25°C (see Figure 3)

integrator and buffer operational amplifiers

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IO}	Input offset voltage			15		mV
I_{IB}	Input bias current			50		pA
V_{OM+}	Positive output voltage swing		9	11		V
V_{OM-}	Negative output voltage swing		−5	−7		V
A_{VD}	Voltage amplification			110		dB
B_1	Unity-gain bandwidth			3		MHZ
CMRR	Common mode rejection	V_{IC} = −1 V to +1 V		100		dB
SR	Output slew rate			5		V/μs

comparator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IO}	Input offset voltage			15		mV
I_{IB}	Input bias current			50		pA
A_{VD}	Voltage amplification			100		dB
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA		200	400	mV
I_{OH}	High-level output current	V_{OH} = 3 V		5	20	nA

voltage reference output

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{ref(0)}$	Reference voltage		1.12	1.22	1.32	V
α_{Vref}	Reference-voltage temperature coefficient	T_A = 0°C to 70°C		80		ppm/°C
r_o	Reference output resistance			3		Ω

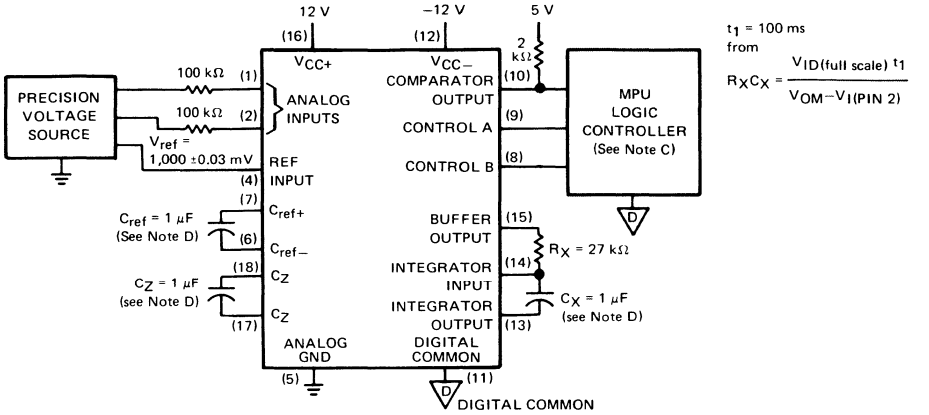
logic control section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	High-level input current	V_{IH} = 2 V		1	10	μA
I_{IL}	Low-level input current	V_{IL} = 0.8 V		−40	−300	μA

total device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC+}	Positive supply current			15	20	mA
I_{CC-}	Negative supply current			12	18	mA

PARAMETER MEASUREMENT INFORMATION



NOTES: C. Tests are started approximately 5 seconds after power-on.

D. Capacitors used are TRW's X363UW poly propylene or eqivalent for C_X, C_{ref}, and C_Z; however for C_{ref} and C_Z, film-dielectric capacitors may be substituted.

FIGURE 3–TEST CIRCUIT CONFIGURATION

external-component selection guide

The autozero capacitor C_Z and reference capacitor C_{ref} should be within the recommended range of operating conditions and should have low leakage characteristics. Most film-dielectric capacitors and some tantalum capacitors provide acceptable results. Ceramic and aluminum capacitors are not recommended because of their relatively high leakage characteristics.

The integrator capacitor C_X should also be within the recommended range and must have good voltage linearity and low dielectric absorbtion. A polypropylene-dielectric capacitor similar to TRW's X363UW is recommended for 4-1/2-digit accuracy. For 3-1/2-digit applications, polyster, polycarbonate, and other film dielectrics are usually suitable. Ceramic and electrolylic capacitors are not recommended.

Stray coupling from the comparator output to any analog pin (in order of importance 17, 18, 14, 7, 6, 13, 1, 2, 15) must be minimized to avoid oscillations. In addition, all power supply pins should be bypassed at the package, for example, by a 0.01-μF ceramic capacitor.

Analog and digital common are internally isolated and may be a different potentials. Digital common can be within 4 volts of positive or negative supply with the logic decode still functioning properly.

The time constant R_XC_X should be kept as near the minimum value as possible and is given by the formula:

$$\text{Minimum } R_XC_X = \frac{V_{ID}\ (\text{full scale})\ t_1}{|V_{OM-}|-V_{I}(\text{pin 2})}$$

where:

V_{ID}(full scale) = Voltage on pin 1 with respect to pin 2

t_1 = Input integration time in seconds

$V_{I(pin\ 2)}$ = Voltage on pin 2 with respect to analog ground

description of digital processors

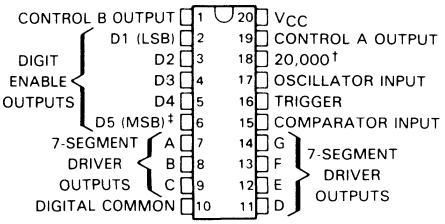
The TL502C and TL503C are control logic devices designed to complement the TL500C and TL501C analog processors. They feature interdigit blanking, over-range blanking, an internal oscillator, and a fast display scan rate. The internal-oscillator input is a Schmitt trigger circuit that can be driven by an external clock pulse or provide its own time base with the addition of a capacitor. The typical oscillator frequency is 120 kHz with a 470-picofarad capacitor connected between the oscillator input and ground.

The TL502C provides seven-segment-display output drivers capable of sinking 100 milliamperes and compatible with popular common-anode displays. The TL503C has four BCD output drivers capable of 100-milliampere sink currents. The code (see next page and Figure 4) for each digit is multiplexed to the output drivers in phase with a pulse on the appropriate digit-enable line at a digit rate equal to f_{osc} divided by 200. Each digit-enable output is capable of sinking 20 milliamperes.

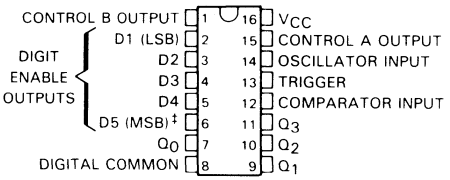
The comparator input of each device, in addition to monitoring the output of the zero-crossing detector in the analog processor, may be used in the display test mode to check for wiring and display faults. A high logic level (2 to 6.5 volts) at the trigger input with the comparator input at or below 6.5 volts starts the integrate-input phase. Voltage levels equal to or greater than 7.9 volts on both the trigger and comparator inputs clear the system and set the BCD counter to 20,000. When normal operation resumes, the conversion cycle is restarted at the auto zero phase.

These devices are manufactured using I^2L and bipolar techniques. The TL502C and TL503C are intended for operation from 0°C to 70°C.

TL502 . . . N DUAL-IN-LINE PACKAGE
(TOP VIEW)



TL503 . . . N DUAL-IN-LINE PACKAGE
(TOP VIEW)



† Pin 18 of TL502 provides an output of f_{osc} (oscillator frequencies) ÷ 20,000.

‡ D5, the most significant bit, is also the sign bit.

TABLE OF SPECIAL FUNCTIONS
V_{CC} = 5 V ±10%

TRIGGER INPUT	COMPARATOR INPUT	FUNCTION
$V_I \leq 0.8$ V	$V_I \leq 6.5$ V	Hold at auto-zero cycle after completion of conversion
2 V $\leq V_I \leq$ 6.5 V	$V_I \leq 6.5$ V	Normal operation (continuous conversion)
$V_I \leq 6.5$ V	$V_I \geq 7.9$ V	Display Test: All BCD outputs high
$V_I \geq 7.9$ V	$V_I \leq 6.5$ V	Internal Test
Both inputs go to $V_I \geq 7.9$ V simultaneously		System clear: Sets BCD counter to 20,000. When normal operation is resumed, cycle begins with Auto Zero.

DIGIT 5 (MOST SIGNIFICANT DIGIT) CHARACTER CODES

CHARACTER	TL502C SEVEN-SEGMENT LINES							TL503C BCD OUTPUT LINES			
	A	B	C	D	E	F	G	Q3	Q2	Q1	Q0
								8	4	2	1
+	H	H	H	H	L	L	L	H	L	H	L
+1	H	L	L	H	L	L	L	H	H	H	L
–	L	H	H	L	H	H	L	H	L	H	H
–1	L	L	L	L	H	H	L	H	H	H	H

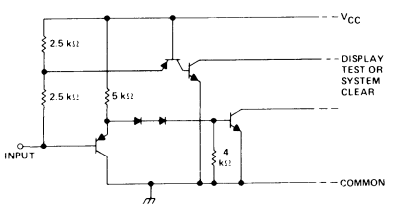
DIGITS 1 THRU 4 NUMERIC CODE (See Figure 4)

NUMBER	TL502C SEVEN-SEGMENT LINES							TL503C BCD OUTPUT LINES			
	A	B	C	D	E	F	G	Q3	Q2	Q1	Q0
								8	4	2	1
0	L	L	L	L	L	L	H	L	L	L	L
1	H	L	L	H	H	H	H	L	L	L	H
2	L	L	H	L	L	H	L	L	L	H	L
3	L	L	L	L	H	H	L	L	L	H	H
4	H	L	L	H	H	L	L	L	H	L	L
5	L	H	L	L	H	L	L	L	H	L	H
6	L	H	L	L	L	L	L	L	H	H	L
7	L	L	L	H	H	H	H	L	H	H	H
8	L	L	L	L	L	L	L	H	L	L	L
9	L	L	L	L	H	L	L	H	L	L	H

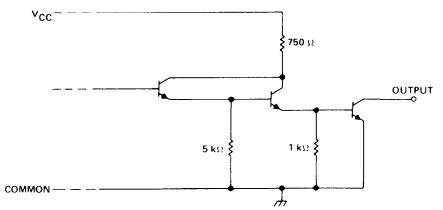
H = high level, L = low level

schematics of inputs and outputs

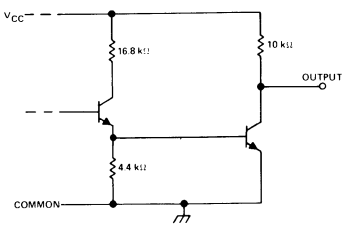
COMPARATOR AND TRIGGER INPUT



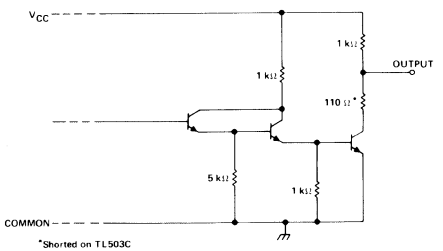
SEGMENT DRIVERS–TL502C
BCD DRIVERS–TL503C



CONTROL A AND B OUTPUTS



DIGIT-ENABLE OUTPUTS



absolute maximum ratings

Supply voltage, V_{CC} (see Note 5)		7	V
Input voltage, V_I	Oscillator	5.5	V
	Comparator or Trigger	9	
Output current	BCD or Segment drivers	120	mA
	Digit-enable outputs	40	
	Pin 18 (TLC502 only)	20	
Total power dissipation at (or below) 30°C free-air temperature (see Note 6)		875	mW
Operating free-air temperature range		0 to 70	°C
Storage temperature range		−65 to 150	°C

NOTES: 5. Voltage values are with respect to the network ground terminal.
6. For operation above 30°C free-air temperature, derate linearly at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	Comparator and trigger inputs	2			V
Low-level input voltage, V_{IL}	Comparator and trigger inputs			0.8	V
Operating free-air temperature		0		70	°C

electrical characteristics at 25°C free-air temperature

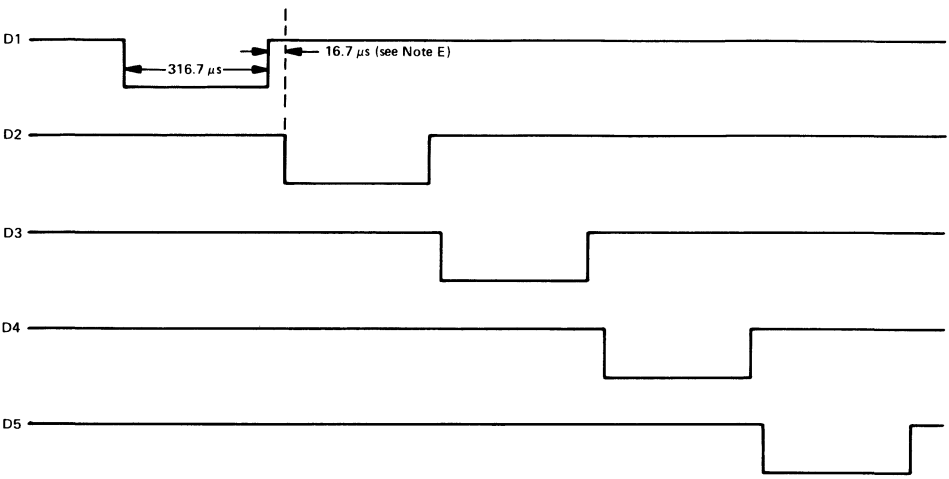
PARAMETER		TERMINAL	TEST CONDITIONS		TL502C			TL503C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IK}	Input clamp voltage	All inputs	V_{CC} = 4.5 V,	I_I = −12 mA		−0.8	−1.5		−0.8	−1.5	V
V_{T+}	Positive-going input threshold voltage	Oscillator	V_{CC} = 5 V			1.5			1.5		V
V_{T-}	Negative-going input threshold voltage	Oscillator	V_{CC} = 5 V			0.9			0.9		V
$V_{T+} - V_{T-}$	Hysteresis	Oscillator	V_{CC} = 5 V		0.4	0.6	0.8	0.4	0.6	0.8	
I_{T+}	Input current at positive-going input threshold voltage	Oscillator	V_{CC} = 5 V		−40	−94	−170	−40	−94	−170	μA
I_{T-}	Input current at negative-going input threshold voltage	Oscillator	V_{CC} = 5 V		40	117	170	40	117	170	μA
V_{OH}	High-level output voltage	Digit enable	V_{CC} = 4.5 V,	I_{OH} = 0	4.15	4.4		4.15	4.4		V
		Pin 18 (TL502C only)			4.25	4.4					
		Control A and B			4.25	4.4		4.25	4.4		
V_{OL}	Low-level output voltage	Digit enable	V_{CC} = 4.5 V	I_{OL} = 20 mA					0.2	0.5	V
		Pin 18 (TL502C only)		I_{OL} = 10 mA		0.15	0.4				
		Control A and B		I_{OL} = 2 mA		0.088	0.4		0.088	0.4	
		Segment drivers		I_{OL} = 100 mA		0.17	0.3				
		BCD drivers		I_{OL} = 100 mA					0.17	0.3	
I_I	Input current	Comparator, Trigger	V_{CC} = 5.5 V,	V_I = 5.5 V		65	100		65	100	μA
		Oscillator					1			1	mA
I_{IH}	High-level input current	Comparator, Trigger	V_{CC} = 5.5 V,	V_I = 2.4 V		−0.6	−1		−0.6	−1	mA
		Oscillator					0.5			0.5	
I_{IL}	Low-level input voltage	Oscillator	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.1	−0.17		−0.1	−0.17	mA
		Comparator, Trigger				−1	−1.6		−1	−1.6	
I_{OH}	High-level output current (Output transistor off)	Digit enable	V_{CC} = 4.5 V	V_O = 0.5 V,	−2.5	−4		−2.5	−4		mA
		Pin 18 (TL502C only)		V_O = 0.5 V	−0.5	−0.9					
		Control A and B		V_O = 0.5 V	−0.25	−0.4		−0.25	−0.4		
		Segment drivers		V_O = 5.5 V			0.25				
		BCD drivers		V_O = 5.5 V						0.25	
I_{OL}	Low-level output current (Output transistor on)	Digit enable	V_{CC} = 4.5 V,	V_O = 3.55 V	18	23					mA
I_{CC}	Supply current	V_{CC}	V_{CC} = 5.5 V			73	110		73	110	mA

special functions† operating characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input current into comparator or trigger inputs	V_{CC} = 5.5 V, V_I = 8.55 V		1.2	1.8	mA
		V_{CC} = 5.5 V, V_I = 6.25 V			0.5	mA

†The comparator and trigger inputs may be used in the normal mode or to perform special functions. See the Table of Special Functions.

TYPICAL APPLICATION DATA



NOTE E. The BCD or seven-segment driver outputs are present for a particular digit slightly before the falling edge of that digit enable.

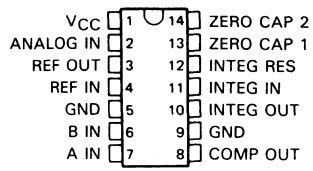
FIGURE 4–TL502C, TL503C DIGIT TIMING WITH 120-kHz CLOCK SIGNAL AT OSCILLATOR INPUT

TYPE TL505C ANALOG-TO-DIGITAL CONVERTER

D2366, OCTOBER 1977—REVISED OCTOBER 1983

- 3-Digit Accuracy (0.1%)
- 10-Bit Resolution
- Automatic Zero
- Internal Reference Voltage
- Single-Supply Operation
- High-Impedance MOS Input
- Designed for use with TMS 1000 Type Microprocessors for Cost-Effective High-Volume Applications
- BI-MOS Technology
- Only 40 mW Typical Power Consumption

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



Caution. This device has limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostic damage to the MOS gates.

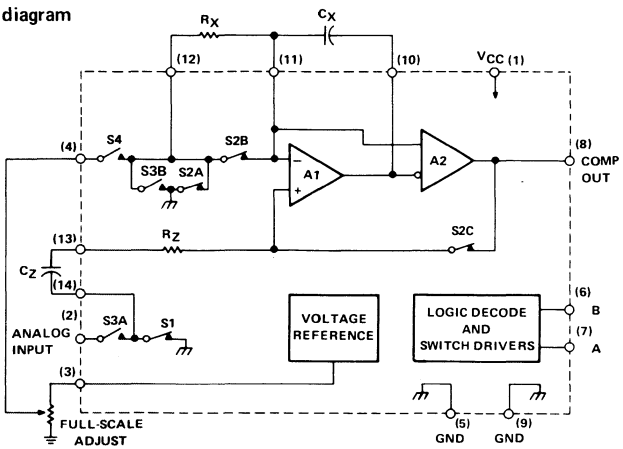
description

The TL505C is an analog-to-digital converter building block designed for use with TMS 1000 type microprocessors. It contains the analog elements (operational amplifier, comparator, voltage reference, analog switches, and switch drivers) necessary for a unipolar automatic-zeroing dual-slope converter. The logic for the dual-slope conversion can be performed by the associated MPU as a software routine or it can be implemented with other components such as the TL502 logic-control device.

The high-impedance MOS inputs permit the use of less expensive, lower value capacitors for the integration and offset capacitors and permit conversion speeds from 20 per second to 0.05 per second.

The TL505C is a product of TI's BI-MOS process, which incorporates bipolar and MOSFET transistors on the same monolithic integrated circuit. The TL505C is characterized for operation from 0°C to 70°C.

functional block diagram



NOTE: Analog and digital GND are internally connected together.

1083

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Input voltage, pins 2, 4, 6, and 7 . . . . . V_{CC}
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 875 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to the two ground terminals connected together.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	7	9	15	V
Analog input voltage, V_I	0		4	V
Reference input voltage, $V_{ref(I)}$	0.5		3	V
High-level input voltage at A or B, V_{IH}	3.6		$V_{CC}+1$	V
Low-level input voltage at A or B, V_{IL}	0.2		1.8	V
Integrator capacitor, C_X	See "component selection"			
Integrator resistor, R_X	0.5		2	MΩ
Integration time, t_1	16.6		500	ms
Operating free-air temperature, T_A	0		70	°C

electrical characteristics, V_{CC} = 9 V, $V_{ref(I)}$ = 1 V, T_A = 25°C, connected as shown in Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage at pin 8	I_{OH} = 0	7.5	8.5		V
I_{OH}	High-level output current at pin 8	V_{OH} = 7.5 V		−100		μA
V_{OL}	Low-level output voltage at pin 8	I_{OL} = 1.6 mA		200	400	mV
V_{OM}	Maximum peak output voltage swing at integrator output	$R_X \geq$ 500 kΩ	$V_{CC}-2$	$V_{CC}-1$		V
$V_{ref(O)}$	Reference output voltage	I_{ref} = −100 μA	1.15	1.22	1.35	V
α_{Vref}	Temperature coefficient of reference output voltage	T_A = 0°C to 70°C		±100		ppm/°C
I_{IH}	High-level input current into A or B	V_I = 9 V		1	10	μA
I_{IL}	Low-level input current into A or B	V_I = 1 V		10	200	μA
I_I	Current into analog input	V_I = 0 to 4 V, A input at 0 V		±10	±200	pA
I_{IB}	Total integrator input bias current			±10		pA
I_{CC}	Supply current	No load		4.5	8	mA

system electrical characteristics, V_{CC} = 9 V, $V_{ref(I)}$ = 1 V, T_A = 25°C, connected as shown in Figure 1 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zero error	V_I = 0		0.1	0.4	mV
Linearity error	V_I = 0 to 4 V		0.02	0.1	%FS
Ratiometric reading	$V_I = V_{ref(I)} \approx$ 1 V,	0.998	1.000	1.002	
Temperature coefficient of ratiometric reading	$V_{ref(I)}$ constant and ≈ 1 V, T_A = 0°C to 70°C		±10		ppm/°C

DEFINITION OF TERMS

Zero Error

The intercept (b) of the analog-to-digital converter system transfer function $y = mx + b$, where y is the digital output, x is the analog input, and m is the slope of the transfer function, which is approximated by the ratiometric reading.

Linearity Error

The maximum magnitude of the deviation from a straight line between the end points of the transfer function.

Ratiometric Reading

The ratio of negative integration time (t_2) to positive integration time (t_1).

PRINCIPLES OF OPERATION

A block diagram of an MPU system utilizing the TL505C is shown in Figure 1. The TL505C operates in a modified positive-integration three-step dual-slope conversion mode. The A/D converter waveforms during the conversion process are illustrated in Figure 2.

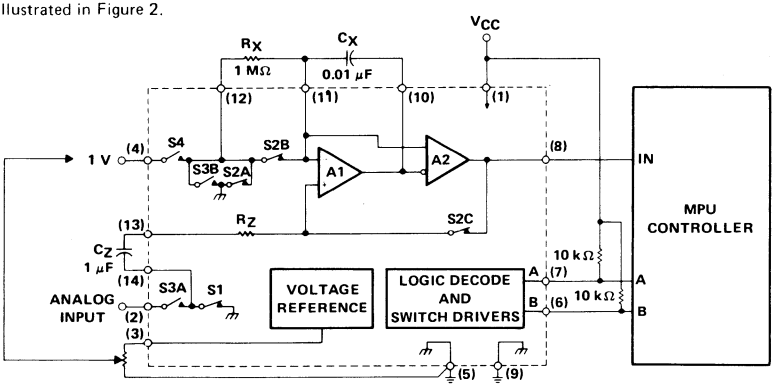
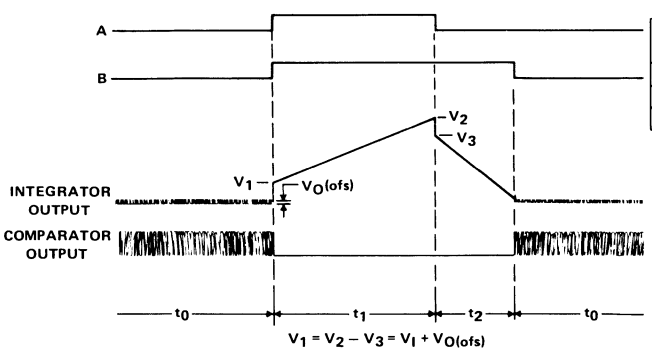


FIGURE 1—FUNCTIONAL BLOCK DIAGRAM OF TL505C INTERFACE WITH A MICROPROCESSOR SYSTEM



FUNCTION TABLE

CONTROLS A	CONTROLS B	ANALOG SWITCHES CLOSED
L	L	S1, S2
H	H	S3
L	H	S1, S4

H = V_{IH}, L = V_{IL}

FIGURE 2—CONVERSION PROCESS TIMING DIAGRAMS

PRINCIPLES OF OPERATION

The first step of the conversion cycle is the auto-zero period t_0 during which the integrator offset is stored in the auto-zero capacitor and the offset of the comparator is stored in the integrator capacitor. To accomplish this, the MPU takes the A and B inputs both low. This is decoded by the switch drivers, which close S1 and S2. The output of the comparator is connected to the input of the integrator through the low-pass filter consisting of R_Z and C_Z. The closed loop of A1 and A2 will seek a null condition where the offsets of the integrator and comparator are stored in C_Z and C_X, respectively. This null condition is characterized by a high-frequency oscillation at the output of the comparator. The purpose of S2B is to shorten the amount of time required to reach the null condition.

At the conclusion of t_0, the MPU takes the A and B inputs both high. This closes S3 and turns all other switches off. The input signal V_I is applied to the noninverting input of A1 through C_Z. V_I is then positively integrated by A1. Since the offset of A1 is stored in C_Z, the change in voltage across C_X will be due to only the input voltage. It should be noted that since the input is integrated in a positive integration during t_1, the output of A1 will be the sum of the input voltage, the integral of the input voltage, and the comparator offset, as shown in Figure 2. The change in voltage across capacitor C_X (V_{CX}) during t_1 is given by

$$\Delta V_{CX(1)} = \frac{V_I\, t_1}{R_1\, C_X} \tag{1}$$

where $R_1 = R_X + R_{S3B}$ and

R_{S3B} is the resistance of switch S3B.

At the end of t_1 the MPU takes the A input low and the B input high. This turns on S1 and S4; all other switches are turned off. In this state the reference is integrated by A1 in a negative sense until the integrator output reaches the comparator threshold. At this point the comparator output goes high. This change in state is sensed by the MPU, which terminates t_2 by again taking the A and B inputs both low. During t_2 the change in voltage across C_X is given by

$$\Delta V_{CX(2)} = \frac{V_{ref}\, t_2}{R_2\, C_X} \tag{2}$$

where $R_2 = R_X + R_{S4} + R_{ref}$ and

R_{ref} is the equivalent resistance of the reference divider.

Since $\Delta V_{CX1} = -\Delta V_{CX2}$, equations (1) and (2) can be combined to give

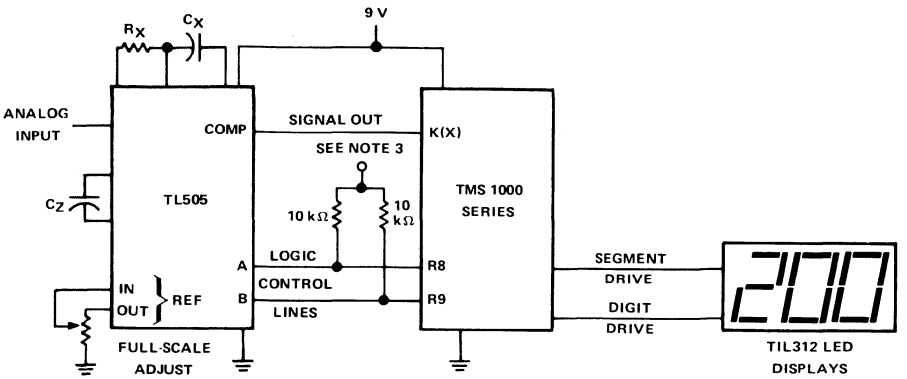
$$V_I = V_{ref} \frac{R_1 \cdot t_2}{R_2 \cdot t_1} \tag{3}$$

This equation is a variation on the ideal dual-slope equation, which is

$$V_I = V_{ref} \frac{t_2}{t_1} \tag{4}$$

Ideally then, the ratio of R_1/R_2 would be exactly equal to one. In a typical TL505C system where $R_X = 1\ M\Omega$, the scaling error introduced by the difference in R_1 and R_2 is so small that it can be neglected, and equation (3) reduces to (4).

TYPICAL APPLICATION DATA



NOTE 3: Connect to either +9 V or 0 V depending on which device in the TMS 1000 series is used and how it is programmed.

FIGURE 5–TL505C IN CONJUNCTION WITH A TMS 1000 SERIES MICROPROCESSOR FOR A 3-DIGIT DIGITAL PANEL METER APPLICATION

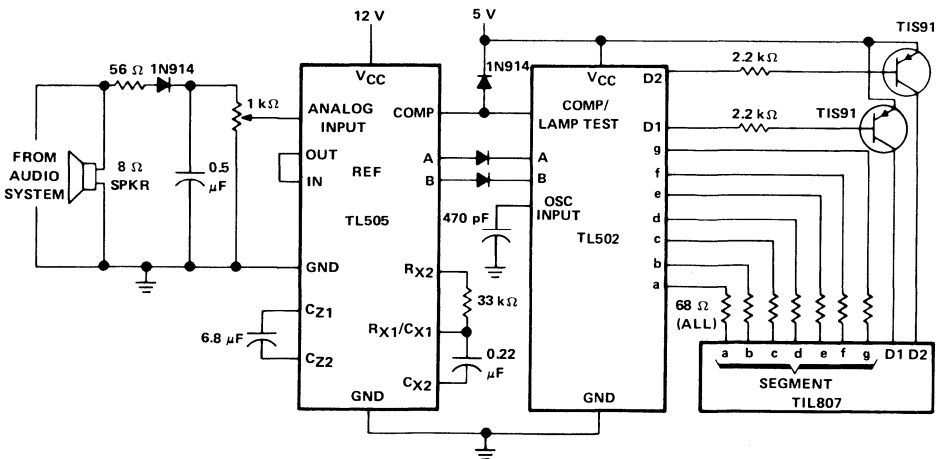


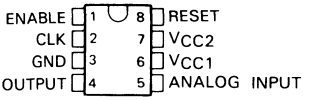
FIGURE 6–AUDIO PEAK POWER METER

TYPES TL507I, TL507C ANALOG-TO-DIGITAL CONVERTER

D2503, OCTOBER 1979–REVISED FEBRUARY 1984

- **Low Cost**
- **7-Bit Resolution**
- **Guaranteed Monotonicity**
- **Ratiometric Conversion**
- **Conversion Speed . . . approximately 1 ms**
- **Single-Supply Operation . . . Either Unregulated 8-V to 18-V (V_{CC2} Input), or Regulated 3.5-V to 6-V (V_{CC1} Input)**
- **I^2L Technology**
- **Power Consumption at 5 V . . . 25 mW Typ**
- **Regulated 5.5-V Output ($\leq$ 1 mA)**

P DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TL507 is a low-cost single-slope analog-to-digital converter designed to convert analog input voltages between 0.25 V_{CC1} and 0.75 V_{CC1} into a pulse-width-modulated output code. It contains a 7-bit synchronous counter, a binary-weighted resistor ladder network, an operational amplifier, two comparators, a buffer amplifier, an internal regulator, and necessary logic circuitry. Integrated-injection logic (I^2L) technology makes it possible to offer this complex circuit at low cost in a small dual-in-line 8-pin package.

FUNCTION TABLE

ANALOG INPUT CONDITION	ENABLE	OUTPUT
X	L†	H
V_I < 200 mV	H	L
V_{ramp} > V_I > 200 mV	H	H
V_I > V_{ramp}	H	L

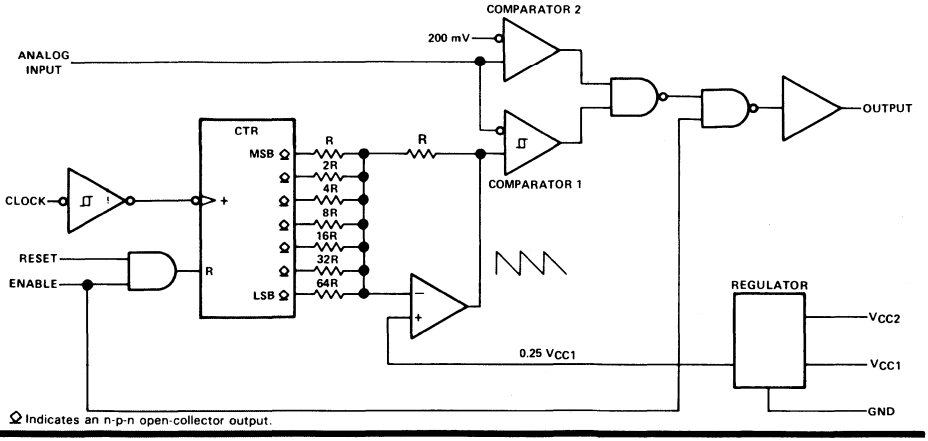
†Low level on enable also inhibits the reset function.
H = high level, L = low level, X = irrelevant

A high level on the reset pin clears the counter to zero, which sets the internal ramp to 0.75 V_{CC}. Internal pull-down resistors keep the reset and enable pins low when not connected.

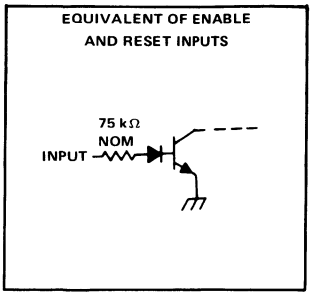
In continuous operation, it is possible to obtain conversion speeds up to 1000 per second. The TL507 requires external signals for clock, reset, and enable. Versatility and simplicity of operation coupled with low cost, makes this converter especially useful for a wide variety of applications.

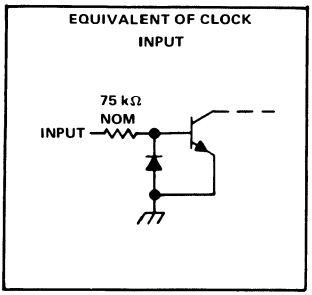
The TL507C is characterized for operation from 0°C to 70°C, and the TL507I is characterized for operation from −40°C to 85°C.

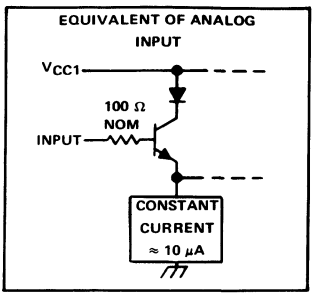
functional block diagram

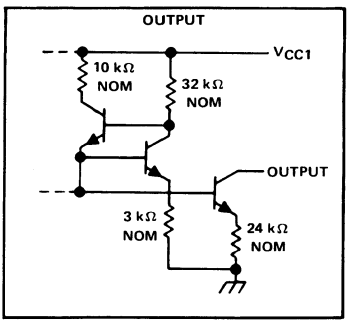


schematics of inputs and outputs









absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 6.5 V
Supply voltage, V_{CC2} . . . . . 20 V
Input voltage at analog input . . . . . 6.5 V
Input voltage at enable, clock, and reset inputs . . . . . ±20 V
On-state output voltage . . . . . 6 V
Off-state output voltage . . . . . 20 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 725 mW
Operating free-air temperature range: TL507I . . . . . −40°C to 85°C
TL507C . . . . . −0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	3.5	5	6	V
Supply voltage, V_{CC2}	8	15	18	V
Input voltage at analog input	0		5.5	V
Input voltage at chip enable, clock, and reset inputs			±18	V
On-state output voltage			5.5	V
Off-state output voltage			18	V
Clock frequency, f_{clock}		125	150	kHz

electrical characteristics over recommended operating free-air temperature range, $V_{CC1} = V_{CC2} = 5$ V (unless otherwise noted)

regulator section

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{CC1}	Supply voltage (output)	V_{CC2} = 10 to 18 V,	I_{CC1} = 0 to −1 mA	5	5.5	6	V
I_{CC1}	Supply current	V_{CC1} = 5 V,	V_{CC2} open		5	8	mA
I_{CC2}	Supply current	V_{CC2} = 15 V,	V_{CC1} open		7	10	mA

inputs

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	Reset and		2			V
V_{IL}	Low-level input voltage	Enable				0.8	V
V_{T+}	Positive-going threshold voltage§	Clock		4.5			V
V_{T-}	Negative-going threshold voltage§	Input				0.4	V
$V_{T+} - V_{T-}$	Hysteresis			2	2.6	4	V
I_{IH}	High-level input current	Reset,	V_I = 2.4 V		17	35	μA
		Enable, and	V_I = 18 V	130	220	320	
I_{IL}	Low-level input current	Clock	V_I = 0			±10	μA
I_I	Analog input current		V_I = 4 V		10	300	nA

output section

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_{OH}	High-level output current	V_{OH} = 18 V		0.1	100	μA
I_{OL}	Low-level output current	V_{OL} = 5.5 V	5	10	15	mA
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA		80	400	mV

operating characteristics over recommended operating free-air temperature range, $V_{CC1} = V_{CC2} = 5.12$ V

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Overall error				±80	mV
Differential nonlinearity	See Figure 1			±1	LSB
Zero error§	Binary count = 0	1.20	1.28	1.36	V
Scale error	Binary count = 127			±80	mV
Full scale input voltage§	Binary count = 127	3.74	3.82	3.9	V
Propagation delay time from reset or enable			2		μs

‡All typical values are at T_A = 25°C.
§These parameters are linear functions of V_{CC1}.

definitions

zero error

The intercept (b) of the analog-to-digital converter-system transfer function y = mx + b, where y is the digital output, x is the analog input, and m is the slope of the transfer function.

overall error

The magnitude of the deviation from a straight line between the endpoints of the transfer function.

differential nonlinearity

Maximum deviation of an analog-value change that is asociated with a 1-bit code change (1 clock pulse) from its theroretical value of 1 LSB.

PARAMETER MEASUREMENT INFORMATION

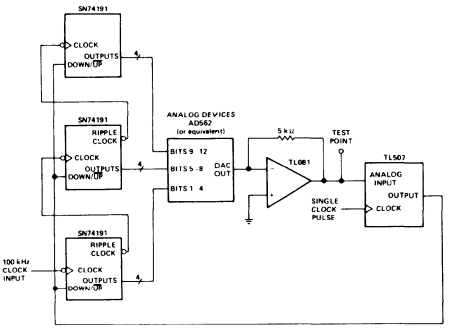


FIGURE 1–MONOTONICITY AND NONLINEARITY TEST CIRCUIT

PRINCIPLES OF OPERATION

The TL507 is a single-slope analog-to-digital converter. All single-slope converters are basically voltage-time or current-to-time converters. A study of the functional block diagram shows the versatility of the TL507.

An external clock signal is applied through a buffer to a negative-edge-triggered synchronous counter. Binary-weighted resistors from the counter are connected to an operational amplifier used as an adder. The operational amplifier generates a signal that ramps from 0.75 • V_{CC1} down to 0.25 • V_{CC1}. Comparator 1 compares the ramp signal to the analog input signal. Comparator 2 functions as a fault defector. With the analog input voltage in the range 0.25 • V_{CC1} to 0.75 • V_{CC1}, the duty cycle of the output signal is determined by the unknown analog input as shown in Figure 2 and the Function Table.

For illustration assume V_{CC1} = 5.12 V,

$$0.25 \cdot V_{CC1} = 1.28 \text{ V}$$

$$1 \text{ binary count} = \frac{(0.75 - 0.25)\, V_{CC1}}{128} = 20 \text{ mV}$$

$$0.75 \cdot V_{CC1} - 1 \text{ count} = 3.82 \text{ V}$$

The output is an open-collector n-p-n transistor capable of withstanding up to 18 volts in the off state. The output is current limited to the 8- to 12-milliampere range; however, care must be taken to ensure that the output does not exceed 5.5 volts in the on state.

The voltage regulator section allows operation from either an unregulated 8- to 18-volt V_{CC2} source or a regulated 3.5- to 6-volt V_{CC1} source. Regardless of which external power source is used, the internal circuitry operates at V_{CC1}. When operating from a V_{CC1} source, V_{CC2} may be connected to V_{CC1} or left open. When operating from a V_{CC2} source, V_{CC1} can be used as a reference voltage output.

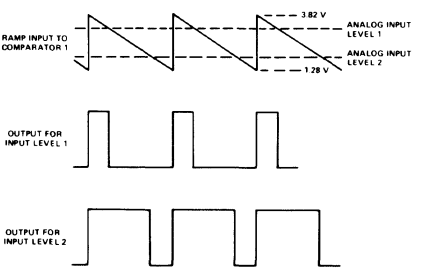


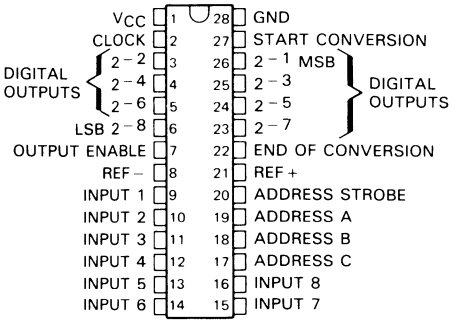
FIGURE 2

TYPES TL520, TL521, TL522 CMOS ANALOG-TO-DIGITAL CONVERTERS WITH 8-CHANNEL MULTIPLEXERS

D2666, SEPTEMBER 1982 – REVISED SEPTEMBER 1983

- **Total Unadjusted Error at 85°C:**
  TL520 . . . ±3/4 LSB MAX
  TL521 . . . ±1 LSB MAX
  TL522 . . . ±1/2 LSB MAX
- **8-Bit Resolution**
- **Built-in 8-Input Analog Multiplexer**
- **Minimum Conversion Time:**
  TL520 . . . 70 μs
  TL521 . . . 100 μs
  TL522 . . . 200 μs
- **Ratiometric Conversion**
- **Guaranteed Monotonicity**
- **No Missing Codes**
- **Easy Interface with Microprocessors**
- **Latched 3-State Outputs**
- **Latched Address Inputs**
- **Single-Supply Operation**
  TL520, TL521 . . . 5 V
  TL522 . . . 3 V
- **Low Power Consumption**
  TL520, TL521 . . . 2.5 mW Typical
  TL522 . . . 0.3 mW Typical

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TL520, TL521, and TL522 are monolithic CMOS devices each with an 8-channel multiplexer, and 8-bit analog-to-digital (A/D) converter, and microprocessor-compatible control logic. The 8-channel multiplexer can be controlled by a microprocessor through a 3-bit address decoder with address load to select any one of eight single-ended analog switches connected directly to a comparator. The 8-bit A/D converter uses a binary-weighted capacitor array to implement the high-speed, successive-approximation conversion technique.

The comparison and conversion methods used eliminate the possibility of missing codes, nonmonotonicity, and the need for zero or full-scale adjustment. Also featured are latched 3-state outputs and latched inputs to the multiplexer address decoder. The single 5 volt supply and low power requirements make the TL520 and TL521 especially useful for a wide variety of applications. The 3-volt and low power requirements make the TL522 especially useful for battery and LCD applications. Ratiometric conversion is made possible by access to the reference voltage input terminals.

The TL520, TL521, and TL522 are characterized for operation from −40°C to 85°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Positive reference input voltage range, V_{REF+} . . . . . V_{REF-} to V_{CC} + 0.3 V
Negative reference input voltage range, V_{REF-} (see Note 1) . . . . . −0.3 V to V_{REF+}
Input voltage range: all other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Continuous total dissipation at 25°C free-air temperature (see Note 2) . . . . . 1250 mW
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

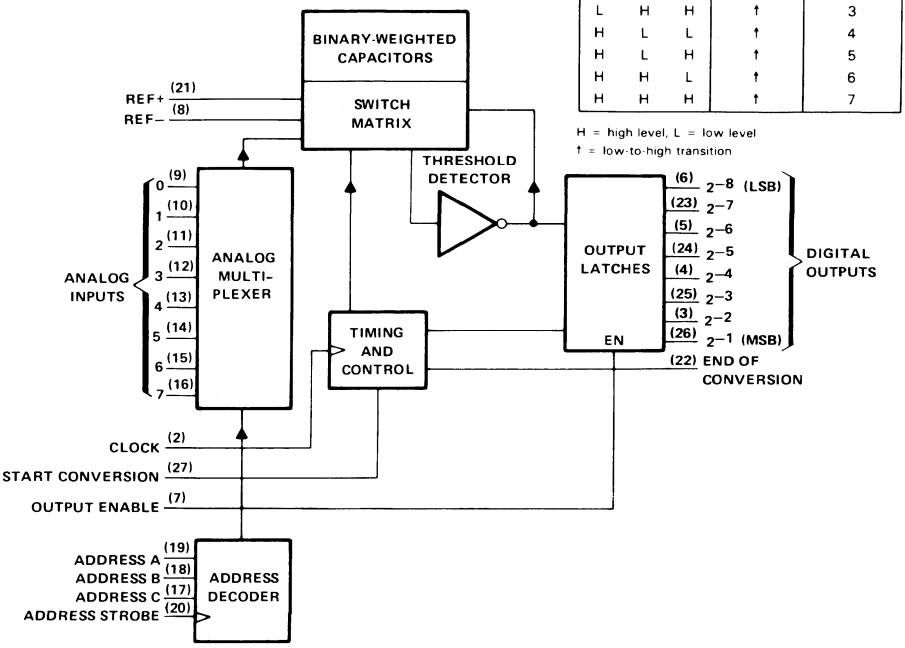
NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

functional block diagram (positive logic)

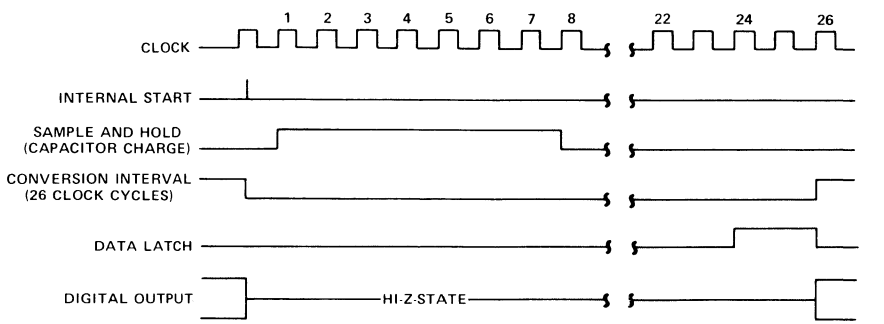
MULTIPLEXER FUNCTION TABLE

INPUTS				SELECTED
ADDRESS			ADDRESS	ANALOG
C	B	A	STROBE	CHANNEL
L	L	L	↑	0
L	L	H	↑	1
L	H	L	↑	2
L	H	H	↑	3
H	L	L	↑	4
H	L	H	↑	5
H	H	L	↑	6
H	H	H	↑	7

H = high level, L = low level
↑ = low-to-high transition



internal timing sequence



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TL520, TL521 recommended operating conditions

		TL520			TL521			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		3	5	5.5	3	5	5.5	V
Positive reference voltage, V_{REF+}		3		V_{CC}	3		V_{CC}	V
Negative reference voltage, V_{REF-}		0		0.3	0		0.3	V
Supply voltage relative to V_{REF+} ($V_{CC} - V_{REF+}$)		0		1	0		1	V
Analog input voltage (see Note 3)		V_{REF-}		V_{REF+}	V_{REF-}		V_{REF+}	V
High-level control input voltage, V_{IH}	$V_{CC} \geq 4.75$ V	$V_{CC} - 1.5$			$V_{CC} - 1.5$			
Low-level control input voltage, V_{IL}	$V_{CC} \geq 4.75$ V			1.5			1.5	V
Clock frequency, f_{clock}	$V_{REF+} = 5$ V		260	370		200	260	kHz
	$V_{REF+} = 3$ V		100			100		
Conversion time, t_{conv}	$V_{CC} = V_{REF+} = 5$ V	70			100			μs
Duration of start pulse, $t_{w(S)}$		100			100			ns
Duration of address strobe pulse, $t_{w(AS)}$		200			200			ns
Address setup time, t_{su}		50			50			ns
Address hold time, t_h		50			50			ns
Input voltage hold time		8			8			clock periods
Operating free-air temperature, T_A		−40		85	−40		85	°C

TL522 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 4)	$T_A = 0°C$ to 85°C	2.75	3	5.5	V
	$T_A = -40°C$ to 0°C	3		5.5	
Positive reference voltage, V_{REF+} (see Notes 3 and 4)		2.75		V_{CC}	V
Negative reference voltage, V_{REF-} (see Note 3)		0		0.3	V
Supply voltage relative to V_{REF+}, $V_{CC} - V_{REF+}$		0		1	V
Analog input voltage (see Note 3)		V_{REF-}		V_{REF+}	V
High-level control input voltage, V_{IH}		$0.7V_{CC}$			V
Low-level control input voltage, V_{IL}				$0.3V_{CC}$	V
Clock frequency, f_{clock}	$V_{REF+} = 5$ V		100	260	kHz
	$V_{REF+} = 2.75$ V (see Note 4)		100	130	
Conversion time, t_{conv} (see Note 5)		200			us
Duration of start pulse, $t_{w(S)}$		600			ns
Duration of address strobe pulse, $t_{w(AS)}$		600			ns
Address setup time, t_{su}		200			ns
Address hold time, t_h		150			ns
Input voltage hold time		8			clock periods
Operating free-air temperature, T_A (see Note 4)		−40		85	°C

NOTES: 3. Analog input voltage greater than V_{REF+} converts as all highs and less than V_{REF-} converts as all lows.
4. For proper operation of TL522 at free-air temperatures below 0°C, V_{CC} and differential reference voltage ($V_{REF+} - V_{REF-}$) must never be less than 3 volts.
5. Conversion time is a function of clock frequency, with 200 μs corresponding to a maximum clock frequency of 130 kHz.

TL520, TL521 electrical characteristics over recommended operating free-air temperature range, V_{CC} = 4.5 V to 5.25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_O = −360 μA		4			V
V_{OL}	Low-level output voltage	I_O = 1.6 mA				0.4	V
I_{OZ}	Off-state (high-impedance state) output current	V_O = 5 V				1	μA
		V_O = 0				−1	
I_{IH}	High-level control input current	$V_I = V_{CC}$ + 0.3 V				1	μA
I_{IL}	Low-level control input current	V_I = 0				−1	μA
$I_{I(op)}$	Peak analog input current (operating) (see Note 6)	$V_{CC} = V_{REF+}$ = 5 V, f_{clock} = 200 kHz,	V_I = 2.5 V, T_A = 25°C		−5	−10	μA
$I_{I(stdby)}$	Analog input current (standby) (see Note 7)	V_{CC} = 5 V,	V_I = 5 V		10	200	nA
		T_A = 25°C	V_I = 0		−10	−200	
		V_{CC} = 5 V,	V_I = 5 V			1	μA
		T_A = 85°C	V_I = 0			−1	
I_{CC}	Supply current (see Note 8)	REF+ and REF− terminals open, f_{clock} = 200 kHz			10	50	μA
$I_{CC} + I_{REF+}$	Supply current plus reference current (see Note 8)	$V_{CC} = V_{REF+}$ = 5 V, f_{clock} = 200 kHz	V_{REF-} = 0,		0.5	1	mA
		$V_{CC} = V_{REF+}$ = 3 V, f_{clock} = 100 kHz	V_{REF-} = 0,		0.1		

†All typical characteristics are at V_{CC} = 5 V and T_A = 25°C (unless otherwise specified)

NOTES: 6. $I_{I(op)}$ is measured on a selected channel and decays exponentially during the first clock pulse.
7. $I_{I(stdby)}$ is measured on a selected channel with the clock input at 0 V.
8. Current increases linearly with frequency of the clock at the rate of approximately 10% per 100 kHz.

TL520, TL521 operating characteristics, T_A = 25°C, $V_{CC} = V_{REF+}$ = 5 V, V_{REF-} = 0, f_{clock} = 370 kHz for TL520 and 260 kHz for TL521 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TL520			TL521			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
k_{SVS}	Supply voltage sensitivity	$V_{CC} = V_{REF+}$ = 4.75 V to 5.25 V		0.05			0.05		%/V
	Linearity error (see Note 9)			±0.25			±0.5		LSB
	Origin error (see Note 9)			±0.25			±0.25		LSB
	Total unadjusted error (see Note 9)	T_A = 25°C		±0.25	±0.5		±0.5		LSB
		T_A = −40°C to 85°C			±0.75			±1	
t_{en}	Output enable time	C_L = 50 pF		100	250		100		ns
t_{dis}	Output disable time	C_L = 10 pF, R_L = 10 kΩ		100	250		100		ns
$t_{d(EOC-L)}$	Delay time, end-of-conversion output		0		100	0		100	ns

‡Typical values for all except supply voltage sensitivity are at V_{CC} = 5 V.

NOTE 9: All errors are measured with reference to an ideal straight-line transfer curve from 9.8 mV to 4.99 V with REF+ = V_{CC}.

TL522 electrical characteristics over recommended operating free-air temperature range, V_{CC} = 3 V to 5.25 V, f_{clock} = 125 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_O = −1 μA		V_{CC} −0.05			V
		V_{CC} = 2.75 V, T_A = 0°C to 85°C	I_O = −0.1 mA,	2.35			
		I_O = −0.36 mA,	V_{CC} = 5 V	V_{CC} −0.4			
V_{OL}	Low-level output voltage	I_O = −1 μA				0.05	V
		V_{CC} = 2.75 V, T_A = 0°C to 85°C	I_O = 0.4 mA,			0.4	
		V_{CC} = 5 V,	I_O = 1.6 mA			0.4	
I_{OZ}	Off-state (high-impedance state) output current	V_{CC} = 5.25 V,	V_O = 5.5 V			1	μA
			V_O = 0			−1	
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 5.5 V			1	μA
I_{IL}	Low-level input current	V_I = 0				−1	μA
$I_{I(op)}$	Peak analog input current (operating) (see Note 6)	V_{CC} = V_{REF+} = 3 V, f_{clock} = 125 kHz,	V_I = 1.5 V, T_A = 25°C		−5	−10	μA
$I_{I(stdby)}$	Analog input current (see Note 7)	V_{CC} = 3 V, T_A = 25°C	V_I = 3 V		10	200	nA
			V_I = 0		−10	−200	
		V_{CC} = 3 V, T_A = 85°C	V_I = 3 V			1	μA
			V_I = 0			−1	
I_{CC}	Supply current from V_{CC1}	REF+ and REF− terminals open			10	50	μA
I_{CC} + I_{REF}	Supply current plus reference current (see Note 8)	V_{CC} = V_{REF+} = 5 V, f_{clock} = 200 kHz	V_{REF-} = 0,		0.5		mA
		V_{CC} = V_{REF+} = 3 V, f_{clock} = 125 kHz	V_{REF-} = 0,		0.1	0.2	
C_i	Input capacitance				10		pF
C_o	Output capacitance				10		pF

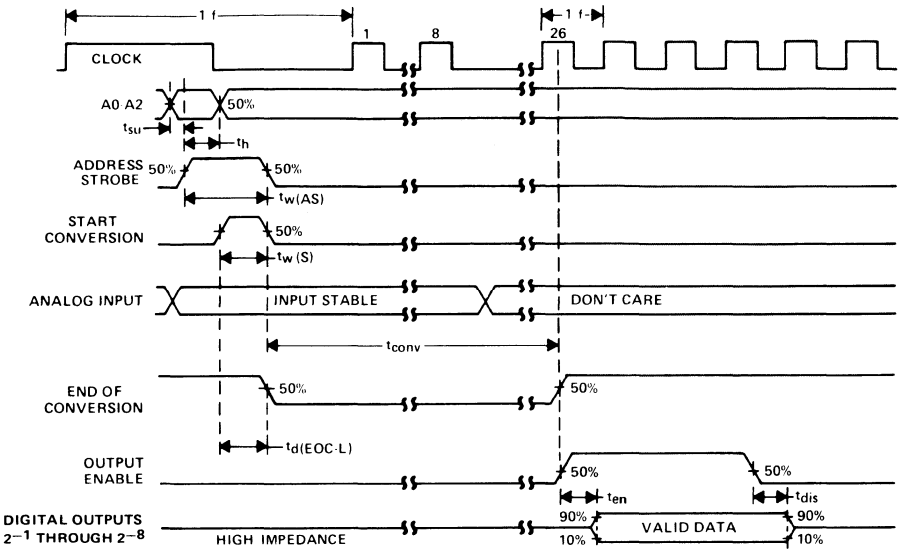
NOTES: 6. $I_{I(op)}$ is measured on a selected channel and decays exponentially during the first clock pulse.
7. $I_{I(stdby)}$ is measured on a selected channel with the clock input at 0 V.
8. Current increases linearly with frequency of the clock at the rate of approximately 10% per 100 kHz.

TL522 operating characteristics, T_A = 25°C, V_{REF+} = 3 V to 5.5 V, V_{REF-} = 0, f_{clock} = 130 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
k_{SVS}	Supply voltage sensitivity			0.05		%/V
	Linearity error (see Note 9)			±0.25		LSB
	Origin error (see Note 9)			±0.25		LSB
	Total unadjusted error (see Note 9)	V_{CC} = 2.75 V, T_A = 0°C to 70°C		±0.25	±0.5	LSB
		T_A = −40°C to 85°C		±0.25	±0.5	
t_{en}	Output enable time	C_L = 50 pF, R_L = 10 kΩ		0.7	1	μs
t_{dis}	Output disable time	C_L = 10 pF, R_L = 10 kΩ		0.6	0.8	μs
$t_{d(EOC-L)}$	Delay time, end-of-conversion output		0		100	ns

†All typical values are at V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)
NOTE 9: All errors are measured with reference to an ideal straight-line transfer curve from 9.8 mV to 4.99 V with REF+ = V_{CC}.

timing diagram



PRINCIPLES OF OPERATION

timing diagram

The analog multiplexer selects 1 of 8 single-ended input channels as determined by the input address code. The address strobe transfers and latches the address into the decoder on the positive-going edge of the signal. The output latch is reset by the postivie-going edge of the start pulse. Sampling also starts with the positive-going edge of the start pulse and lasts for 8 clock periods. The conversion process may be interrupted by a new start pulse before the end of 24 clock periods. The previous data will be lost if a new start of conversio occurs before the 24th clock pulse. Continuous conversion may be accomplished by connecting the end-of-pconversion output to the start input. If used in this mode an external pulse should be applied after power up to assure start up.

converter

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (Figure 1). In the first phase of the conversion process, the analog input is sampled by closing switch S_C and all S_T switches, and by simultaneously charging all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all 8 bits are identified, and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 128). Node 128 of this capacitor is switched to the reference voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF – . If the voltage at the summing node is greater than the trip-point of the threshold detector (approximately one-half the reference voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to REF – . If the voltage at the summing node is less than the trip point of the threshold detector, this 128-weight capacitor remains connected to REF + through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, the 32-weight capacitor, and so forth down the line, until all bits are counted.

With each step of the capacitor-sampling process, the initial charge is redistributed among the capacitors. The conversion process is succcessive approximation, but relies on charge shifting rather than a successive-approximation register (and reference D/A) to count and weigh the bits from MSB to LSB.

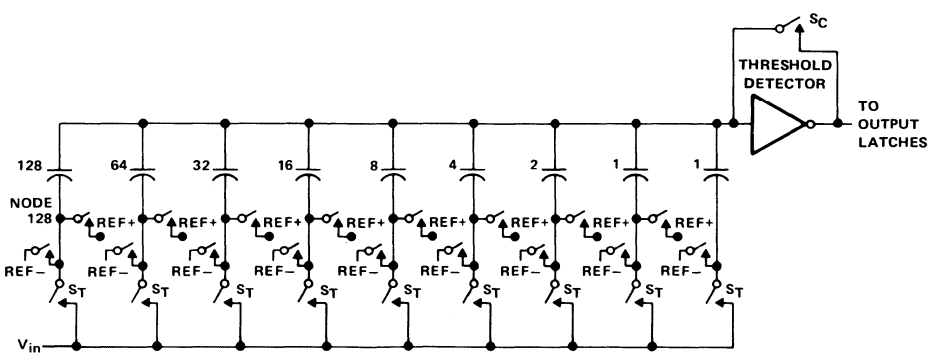


FIGURE 1–SIMPLIFIED MODEL OF THE SUCCESSIVE-APPROXIMATION SYSTEM

TYPICAL APPLICATION INFORMATION

The TL520, TL521, and TL522 are CMOS devices using charge redistribution to achieve A/D conversion. In typical applications as a ratiometric conversion system for a microprocessor, REF− will be connected to ground and REF+ will be connected to V_{CC}. The output will then be a simple proportional ratio between the analog input voltage and V_{CC} (Figure 3). The general relationship is

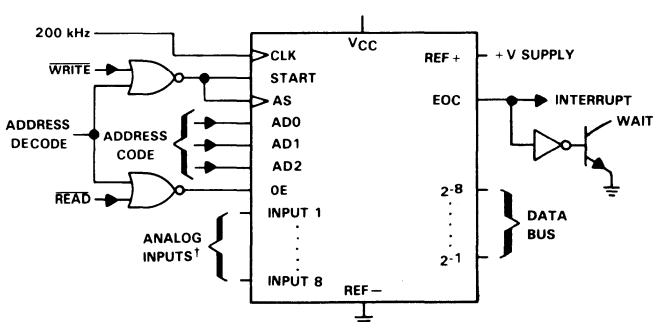
$$\frac{D_{out}}{2^8} = \frac{V_{in}}{V_{REF+} - V_{REF-}}$$

where D_{out} = decimal value of binary output word
V_{in} = analog input voltage
V_{REF+} = positive reference voltage = V_{CC}
V_{REF-} = negative reference voltage = V_{GND}

Latchup may overheat and destroy the device and may occur by either of two kinds of circumstances: out of range reference voltages or by incorrect power-up sequence. V_{REF+} should not be more positive than V_{CC} by more than 300 millivolts or V_{REF-} should not be more negative than GND by more than 300 millivolts. Apply V_{CC} before either of the reference voltages. The advantage of the compressed reference potential is that the full 8-bit resolution applies to be compressed voltage range (Figure 4). However, the cautions mentioned above must be observed. Operation at voltages down to V_{CC} = 3 volts is possible but limits the frequency to 100 kilohertz maximum and thus conversion time to 260 microseconds minimum. Interface for the common microprocessors is shown in Figure 2.

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	READ	WRITE	INTERRUPT (COMMENT)
TMS7000	RD	WR	EINT
TMS9900	MEMEN	WE	INTREQ
8080	MEMR	MEMW	INTR (Thru RST Circuit)
8085	RD	WR	INTR (Thru RST Circuit)
Z-80	RD	WR	INT (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA + 2 R/W	VMA + 2 R/W	IRQA or IRQB (Thru PIA)



† The full-scale value of the analog input voltage can be shifted between 3 volts and 6.5 volts by varying V_{REF-} and V_{CC}, but only 5 volts guarantees TTL compatibility.

FIGURE 2 — TYPICAL MICROPROCESSOR APPLICATION

TYPICAL APPLICATION INFORMATION

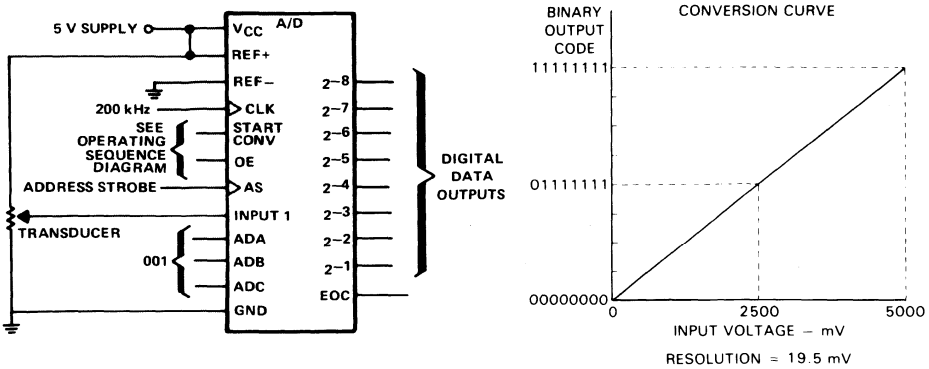


FIGURE 3 – RATIOMETRIC SYSTEM

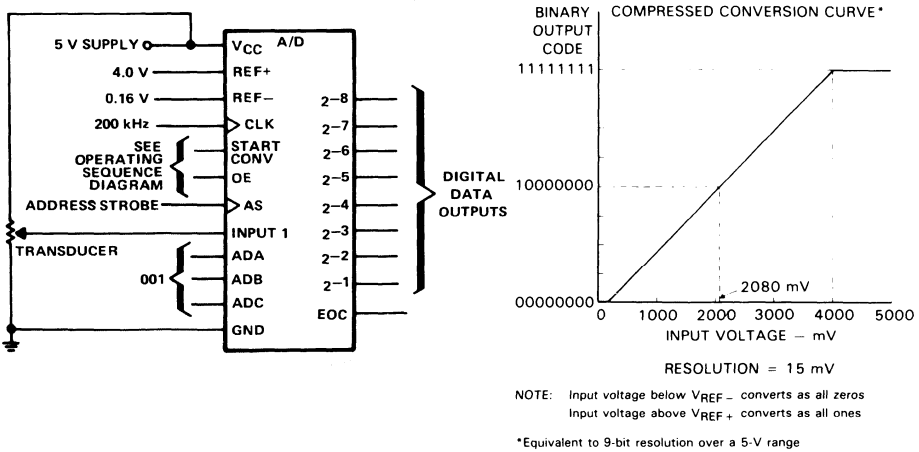


FIGURE 4–COMPRESSED RATIOMETRIC SYSTEM

TYPES TL601, TL604, TL607, TL610 P-MOS ANALOG SWITCHES

D2401, JUNE 1976 – REVISED OCTOBER 1983

- **Switches ±10 V analogue signals**
- **TTL/DTL logic capability**
- **5 to 30 V supply ranges**
- **Low (100 Ω) on-state resistance**
- **High (10^{11} Ω) off-state resistance**
- **8 pin functions**

description

The TL601, TL604, TL607, and TL610 are a family of monolithic P-MOS analog switches that provide fast switching speeds with high r_{off}/r_{on} ratio and no offset voltage. The p-channel enhancement-type MOS switches will accept analog signals up to ±10 volts and are controlled by TTL-compatible logic inputs. The monolithic structure is made possible by BI-MOS technology, which combines p-channel MOS with standard bipolar transistors.

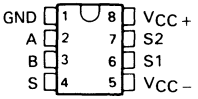
These switches are particularly suited for use in military, industrial, and commercial applications such as data acquisition, multiplexers, A/D and D/A converters, MODEMS, sample-and-hold systems, signal multiplexing, integrators, programmable operational amplifiers, programmable voltage regulators, crosspoint switching networks, logic interface, and many other analog systems.

The TL601 is an SPDT switch with two logic control inputs. The TL604 is a dual complementary SPST switch with a single control input. The TL607 is an SPDT switch with one logic control input and one enable input. The TL610 is an SPST switch with three logic control inputs. The TL610 features a higher r_{off}/r_{on} ratio than the other members of the family.

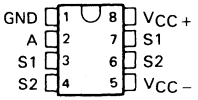
The TL601M, TL604M, TL607M, and TL610M are characterized for operation over the full military temperature range of −55°C to 125°C, the TL601I, TL604I, TL607I, and TL610I are characterized for operation from −25°C to 85°C, and the TL601C, TL604C, TL607C, and TL610C are characterized for operation from 0°C to 70°C.

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

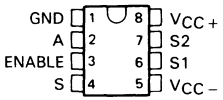
TL601



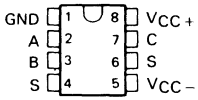
TL604



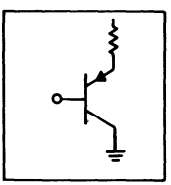
TL607



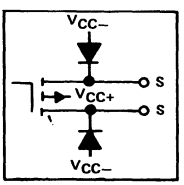
TL610



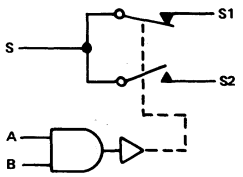
TYPICAL OF ALL INPUTS



TYPICAL OF ALL SWITCHES



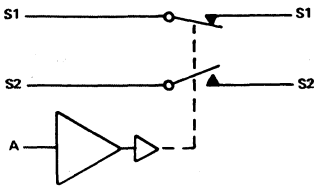
TL601



FUNCTION TABLE

LOGIC INPUTS		ANALOG SWITCH	
A	B	S1	S2
L	X	OFF (OPEN)	ON (CLOSED)
X	L	OFF (OPEN)	ON (CLOSED)
H	H	ON (CLOSED)	OFF (OPEN)

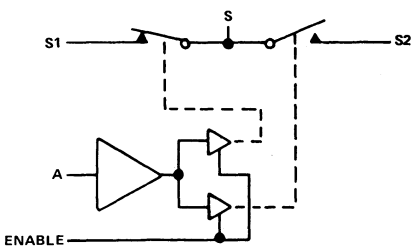
TL604



FUNCTION TABLE

LOGIC INPUT	ANALOG SWITCH	
A	S1	S2
H	ON (CLOSED)	OFF (OPEN)
L	OFF (OPEN)	ON (CLOSED)

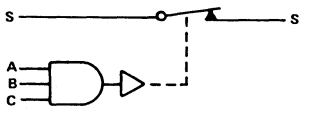
TL607



FUNCTION TABLE

INPUTS		ANALOG SWITCH	
A	ENABLE	S1	S2
X	L	OFF (OPEN)	OFF (OPEN)
L	H	OFF (OPEN)	ON (CLOSED)
H	H	ON (CLOSED)	OFF (OPEN)

TL610



FUNCTION TABLE

INPUTS			ANALOG SWITCH
A	B	C	S
L	X	X	OFF (OPEN)
X	L	X	OFF (OPEN)
X	X	L	OFF (OPEN)
H	H	H	ON (CLOSED)

H = high logic level
L = low logic level
X = irrelevant

Switch positions shown are for all inputs high.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 30 V
Supply voltage, V_{CC-} . . . . . −30 V
V_{CC+} to V_{CC-} supply voltage differential . . . . . 35 V
Control input voltage . . . . . V_{CC+}
Switch off-state voltage . . . . . 30 V
Switch on-state current . . . . . 10 mA
Operating free-air temperature range: TL601M, TL604M, TL607M, TL610M . . . . . −55°C to 125°C
TL601I, TL604I, TL607I, TL610I . . . . . −25°C to 85°C
TL601C, TL604C, TL607C, TL610C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: P package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	TL601M, TL604M TL607M, TL610M			TL601I, TL604I TL607I, TL610I			TL601C, TL604C TL607C, TL610C			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+} (see Figure 1)	5	10	25	5	10	25	5	10	25	V
Supply voltage, V_{CC-} (see Figure 1)	−5	−20	−25	−5	−20	−25	−5	−20	−25	V
V_{CC+} to V_{CC-} supply voltage differential (see Figure 1)	15		30	15		30	15		30	V
Control input voltage	0		5.5	0		5.5	0		5.5	V
Voltage at any analog switch (S) terminal	$V_{CC-}+8$		V_{CC+}	$V_{CC-}+8$		V_{CC+}	$V_{CC-}+8$		V_{CC+}	V
Switch on-state current			10			10			10	mA
Operating free-air temperature, T_A	−55		125	−25		85	0		70	°C

Figure 1 shows power supply boundary conditions for proper operation of the TL601 Series. The range of operation for supply V_{CC+} from +5 V to +25 V is shown on the vertical axis. The range of V_{CC-} from −5 volts to −25 volts is shown on the horizontal axis. A recommended 30-volt maximum voltage differential from V_{CC+} to V_{CC-} governs the maximum V_{CC+} for a chosen V_{CC-} (or vice versa). A minimum recommended difference of 15 volts from V_{CC+} to V_{CC-} and the boundaries shown in Figure 1 allow the designer to select the proper combinations of the two supplies.

The designer-selected V_{CC+} for a chosen V_{CC-} supply values limit the maximum input voltage that can be applied to either switch terminal; that is, the input voltage should be between V_{CC-} +8 V and V_{CC+} to keep the on-state resistance within specified limits.

RECOMMENDED COMBINATIONS
OF SUPPLY VOLTAGES

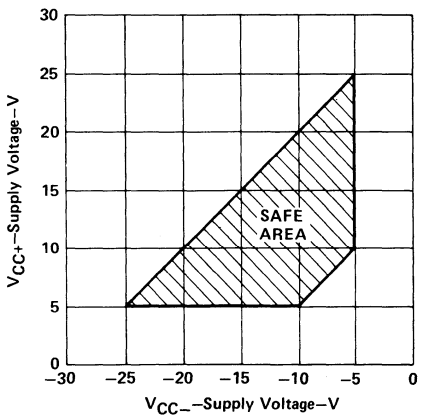


FIGURE 1

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 10 V, V_{CC-} = −20 V, analog switch test current = 1 mA (unless otherwise noted)

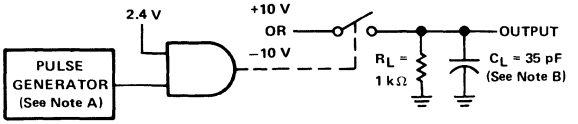
PARAMETER		TEST CONDITIONS†			TL6__M TL6__I MIN	TL6__M TL6__I TYP‡	TL6__M TL6__I MAX	TL6__C MIN	TL6__C TYP‡	TL6__C MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage		Enable input of TL607M				0.6				V
			All other inputs				0.8			0.8	
I_{IH}	High-level input current	V_I = 5.5 V				0.5	10		0.5	10	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−50	−250		−50	−250	μA
I_{off}	Switch off-state current	$V_{I(sw)}$ = −10 V, See Note 2		T_A = 25°C		−400			−500		pA
				T_A = MAX		−50	−100		−10	−20	nA
r_{on}	Switch on-state resistance	$V_{I(sw)}$ = 10 V, $I_{O(sw)}$ = −1 mA		TL601 TL604 TL607		55	100		75	200	Ω
				TL610		40	80		40	100	
		$V_{I(sw)}$ = −10 V, $I_{O(sw)}$ = −1 mA		TL601 TL604 TL607		220	400		220	600	
				TL610		120	300		120	400	
r_{off}	Switch off-state resistance					1 X 10^{11}			5 X 10^{10}		Ω
C_{on}	Switch on-state input capacitance	$V_{I(sw)}$ = 0 V, f = 1 MHz				16			16		pF
C_{off}	Switch off-state input capacitance	$V_{I(sw)}$ = 0 V, f = 1 MHz				8			8		pF
I_{CC+}	Supply current from V_{CC+}	Logic input(s) at 5.5 V, All switch terminals open		TL601 TL604		5	10		5	10	mA
			Enable input high	TL607		5	10		5	10	
			Enable input low			3	5		3	5	
				TL610		5	10		5	10	
I_{CC-}	Supply current from V_{CC-}	Logic input(s) at 5.5 V, All switch terminals open		TL601 TL604		−1.2	−2.5		−1.2	−2.5	mA
			Enable input high	TL607		−2.5	−5		−2.5	−5	
			Enable input low			−0.05	−0.5		−0.05	−0.5	
				TL610		−1.2	−2.5		−1.2	−2.5	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at T_A = 25°C.
NOTE 2: The other terminal of the switch under test is at V_{CC+} = 10 V.

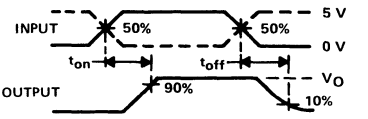
switching characteristics, V_{CC} = 10 V, V_{CC-} = −20 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Switch turn-off time	R_L = 1 kΩ, C_L = 35 pF, See Figure 2		400	500	ns
t_{on}	Switch turn-on time			100	150	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



$V_O = (10\ V)\ \frac{1\ k\Omega}{1\ k\Omega + r_{on}}$

VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics:
Z_{out} = 50Ω, t_r = 15 ns, t_f = 15 ns, t_w = 500 ns.
B. C_L includes probe and jig capacitance.

FIGURE 2

TYPICAL CHARACTERISTICS

SWITCH ON-STATE RESISTANCE
vs
FREE-AIR TEMPERATURE

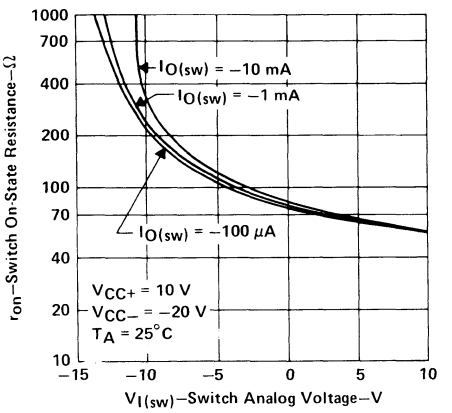


FIGURE 3

SWITCH ON-STATE RESISTANCE
vs
SWITCH ANALOG VOLTAGE

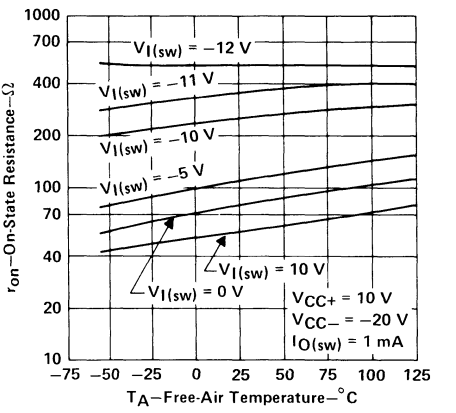


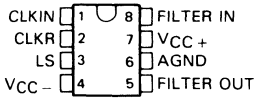
FIGURE 4

TLC04, TLC14
BUTTERWORTH FOURTH-ORDER LOW-PASS SWITCHED-CAPACITOR FILTERS

D2970, NOVEMBER, 1986

- **Low Clock-to-Cutoff-Frequency Ratio Error**
  TLC04 . . . ±0.8%
  TLC14 . . . ±1%
- **Filter Cutoff Frequency Dependent Only on External-Clock Frequency Stability**
- **Minimum Filter Response Deviation Due to External Component Variations Over Time and Temperature**
- **Cutoff Frequency Range from 0.1 Hz to 20 kHz**
- **5-V to 12-V Operation**
- **Self Clocking or TTL-Compatible and CMOS-Compatible Clock Inputs**
- **Designed to be Interchangeable with National MF4-50 and MF4-100**

D OR P PACKAGE
(TOP VIEW)



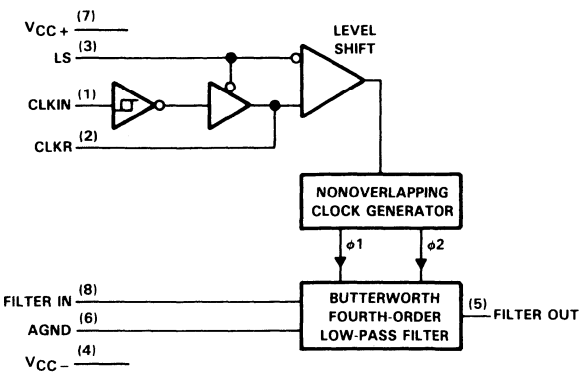
description

The TLC04 and TLC14 are monolithic Butterworth low-pass switched-capacitor filters. Each is designed as a low-cost, easy-to-use device and to provide accurate fourth-order low-pass filter functions in circuit design configurations.

Each filter features cutoff frequency stability that is dependent only on the external-clock frequency stability. The cutoff frequency is clock tunable and has a clock-to-cutoff frequency ratio of 50:1 with less than ±0.8% error for the TLC04 and a clock-to-cutoff frequency ratio of 100:1 with less than ±1% error for the TLC14. The input clock features self-clocking or TTL- or CMOS-compatible options in conjunction with the level shift (LS) pin.

The TLC04 and TLC14 are characterized for operation from 0°C to 70°C.

functional block diagram



pin description

PIN NAME	PIN NO.	I/O	DESCRIPTION
AGND	6	I	Analog Ground — The noninverting input to the operational amplifiers of the Butterworth fourth-order low-pass filter.
CLKIN	1	I	Clock In — The clock input terminal for CMOS-compatible clock or self-clocking options. For either option, the Level Shift (LS) terminal is at V_{CC-}. For self-clocking, a resistor is connected between the CLKIN and CLKR terminal pins and a capacitor is connected from the CLKIN terminal pin to ground.
CLKR	2	I	Clock R — The clock input for a TTL-compatible clock. For a TTL clock, the level shift pin is connected to mid-supply and the CLKIN pin may be left open, but it is recommended that it be connected to either V_{CC+} or V_{CC-}.
FILTER IN	8	I	Filter Input
FILTER OUT	5	O	Butterworth fourth-order low-pass Filter Output
LS	3	I	Level Shift — This terminal accommodates the various input clocking options. For CMOS-compatible clocks or self-clocking, the level-shift terminal is at V_{CC-} and for TTL-compatible clocks, the level-shift terminal is at mid-supply.
V_{CC+}	7	I	Positive supply voltage terminal
V_{CC-}	4	I	Negative supply voltage terminal

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC\pm}$ (see Note 1) . . . . . ±7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to the AGND terminal.

recommended operating conditions

		TLC04		TLC14		UNIT
		MIN	MAX	MIN	MAX	
V_{CC+}	Positive supply voltage	2.5	6	2.5	6	V
V_{CC-}	Negative supply voltage	−2.5	−6	−2.5	−6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
f_{clock}	Clock frequency (see Note 2)	5	1×10^6	10	1×10^6	Hz
f_{co}	Cutoff frequency (see Note 3)	0.1	20×10^3	0.1	10×10^3	Hz
T_A	Operating free-air temperature	0	70	0	70	°C

NOTES: 2. Above 250 kHz, the input clock duty cycle should be at 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.
3. The cutoff frequency is defined as the frequency where the response is 3.01 dB less than the dc gain of the filter.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 2.5 V, V_{CC-} = −2.5 V, f_{clock} ≤ 250 kHz (unless otherwise noted)

filter section

PARAMETER			TEST CONDITIONS	TLC04			TLC14			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OO}	Output voltage offset				−150			−300		mV
V_{OM}	Peak output voltages	V_{OM+}	R_L = 5 kΩ	2	2.3		2	2.3		V
		V_{OM-}		−1	−1.5		−1	−1.5		
I_{OS}	Short-circuit output current	Source	T_A = 25°C, See Note 4		−0.5			−0.5		mA
		Sink			28			28		
I_{CC}	Supply current		f_{clock} = 250 kHz		1.5	2.25		1.5	2.25	mA

NOTE 4: I_{OS} (source current) is measured by forcing the output to its maximum positive voltage and then shorting the output to the negative supply (V_{CC-}) terminal. I_{OS} (sink current) is measured by forcing the output to its maximum negative voltage and then shorting the output to the positive supply (V_{CC+}) terminal.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 2.5 V, V_{CC-} = −2.5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLC04			TLC14			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Clock-to-cutoff-frequency ratio (f_{clock}/f_{co})	f_{clock} ≤ 250 kHz, T_A = 25°C		49.27	50.07	50.87	99	100	101	
Temperature coefficient of clock-to-cutoff frequency ratio	f_{clock} ≤ 250 kHz		−25	0	25	−25	0	25	ppm/°C
Frequency response above and below cutoff frequency (see Note 5)	f_{co} = 5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 6 kHz	−8.11	−7.57	−7.03				dB
		f = 4.5 kHz	−1.7	−1.46	−1.22				
	f_{co} = 2.5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 3 kHz				−7.92	−7.42	−6.92	dB
		f = 2.25 kHz				−1.77	−1.51	−1.25	
Dynamic range (see Note 6)	T_A = 25°C			80			78		dB
Stop-band frequency attentuation at 2 f_{co}	f_{clock} ≤ 250 kHz		24	25		24	25		dB
DC voltage amplification	f_{clock} ≤ 250 kHz, RS ≤ 2 kΩ		−0.15	0	0.15	−0.15	0	0.15	dB
Peak-to-peak clock feedthrough voltage	T_A = 25°C			15			15		mV

† All typical values are at T_A = 25°C.

NOTES: 5. The frequency responses at f are referenced to a dc gain of 0 dB.

6. The dynamic range is referenced to 2.82 V rms (4 V peak) where the wideband noise over a 20-kHz bandwidth is typically 282 μV rms for the TLC04 and 355 μV rms for the TLC14.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, f_{clock} ≤ 250 kHz, (unless otherwise noted)

filter section

PARAMETER		TEST CONDITIONS	TLC04			TLC14			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OO} Output voltage offset				−200			−400		mV
V_{OM} Peak output voltages	V_{OM+}	R_L = 5 kΩ	4	4.5		4	4.5		V
	V_{OM-}		−4	−4.1		−4	−4.1		
I_{OS} Short-circuit output current	Source	T_A = 25°C,		−1.5			−1.5		mA
	Sink	See Note 4		50			50		
I_{CC} Supply current		f_{clock} = 250 kHz		2.5	3.5		2.5	3.5	mA

NOTE 4: I_{OS} (source current) is measured by forcing the output to its maximum positive voltage and then shorting the output to the negative supply (V_{CC-}) terminal. I_{OS} (sink current) is measured by forcing the output to its maximum negative voltage and then shorting the output to the positive supply (V_{CC+}) terminal.

clocking section

PARAMETER		TEST CONDITIONS‡		MIN	TYP†	MAX	UNIT
V_{T+} Positive-going input threshold voltage	CLKIN	V_{CC} = 10 V		6.1	7	8.9	V
		V_{CC} = 5 V		3.1	3.5	4.4	
V_{T-} Negative-going input threshold voltage	CLKIN	V_{CC} = 10 V		1.3	3	3.8	V
		V_{CC} = 5 V		0.6	1.5	1.9	
V_{hys} Hysteresis ($V_{T+} - V_{T-}$)	CLKIN	V_{CC} = 10 V		2.3	4	7.6	V
		V_{CC} = 5 V		1.2	2	3.8	
V_{OH} High-level output voltage	CLKR	V_{CC} = 10 V	I_O = −10 μA	9			V
		V_{CC} = 5 V		4.5			
V_{OL} Low-level output voltage	CLKR	V_{CC} = 10 V	I_O = 10 μA			1	V
		V_{CC} = 5 V				0.5	
Input leakage current	CLKR	V_{CC} = 10 V	Level Shift pin at mid-supply,			2	μA
		V_{CC} = 5 V	T_A = 25°C			2	
Output current	CLKR	V_{CC} = 10 V	CLKR shorted to V_{CC-}	−3	−6		mA
		V_{CC} = 5 V		−0.75	−1.5		
Output current	CLKR	V_{CC} = 10 V	CLKR shorted to V_{CC+}	2.5	5		mA
		V_{CC} = 5 V		0.65	1.3		

† All typical values are at T_A = 25°C.
‡ $V_{CC} = V_{CC+} - V_{CC-}$.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLC04			TLC14			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Clock-to-cutoff-frequency ratio (f_{clock}/f_{co})	f_{clock} ≤ 250 kHz, T_A = 25°C		49.58	49.98	50.38	99	100	101	
Temperature coefficient of clock-to-cutoff frequency ratio	f_{clock} ≤ 250 kHz		−15	0	15	−15	0	15	ppm/°C
Frequency response above and below cutoff frequency (see Note 5)	f_{co} = 5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 6 kHz	−7.84	−7.57	−7.3				dB
		f = 4.5 kHz	−1.56	−1.44	−1.32				
	f_{co} = 2.5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 3 kHz				−7.67	−7.42	−7.17	dB
		f = 2.25 kHz				−1.64	−1.51	−1.38	
Dynamic range (see Note 7)	T_A = 25°C			80			78		dB
Stop-band frequency attentuation at 2 f_{co}	f_{clock} ≤ 250 kHz		24	25		24	25		dB
DC voltage amplification	f_{clock} ≤ 250 kHz, RS ≤ 2 kΩ		−0.15	0	0.15	−0.15	0	0.15	dB
Peak-to-peak clock feedthrough voltage	T_A = 25°C			25			25		mV

† All typical values are at T_A = 25°C.

NOTES: 5. The frequency responses at f are referenced to a dc gain of 0 dB.

7. The dynamic range is referenced to 2.82 V rms (4 V peak) where the wideband noise over a 20-kHz bandwidth is typically 282 μV rms for the TLC04 and 355 μV rms for the TLC14.

TYPICAL APPLICATION DATA

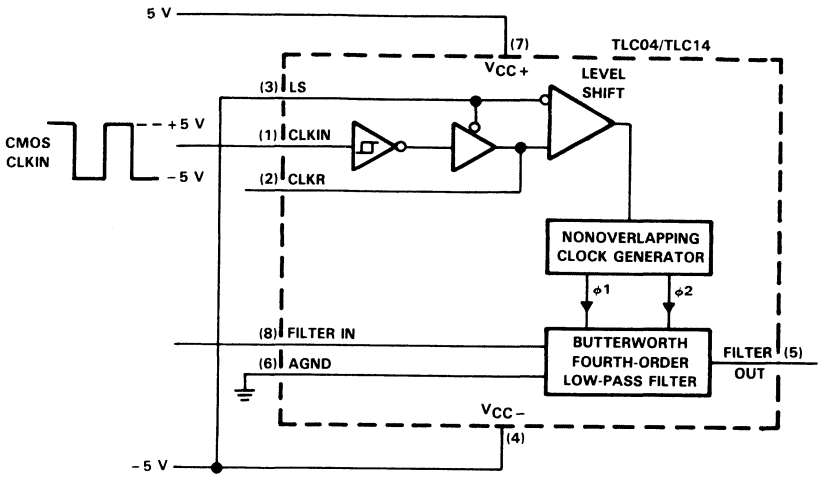


FIGURE 1. CMOS-CLOCK-DRIVEN, DUAL-SUPPLY OPERATION

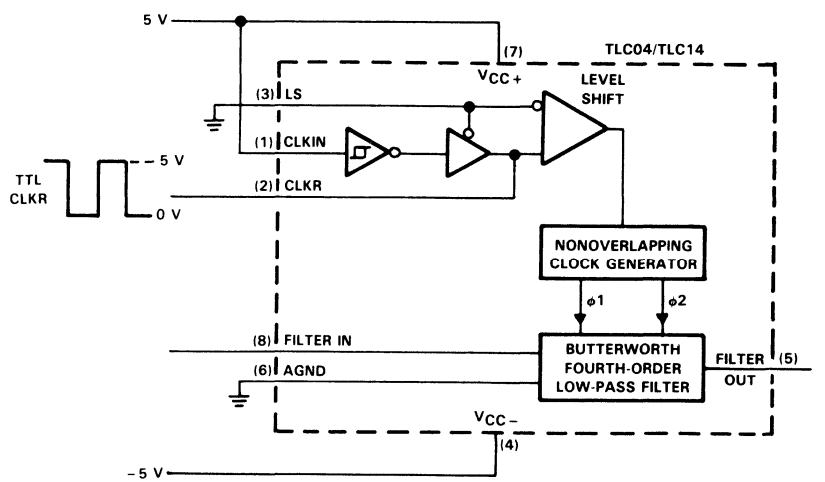
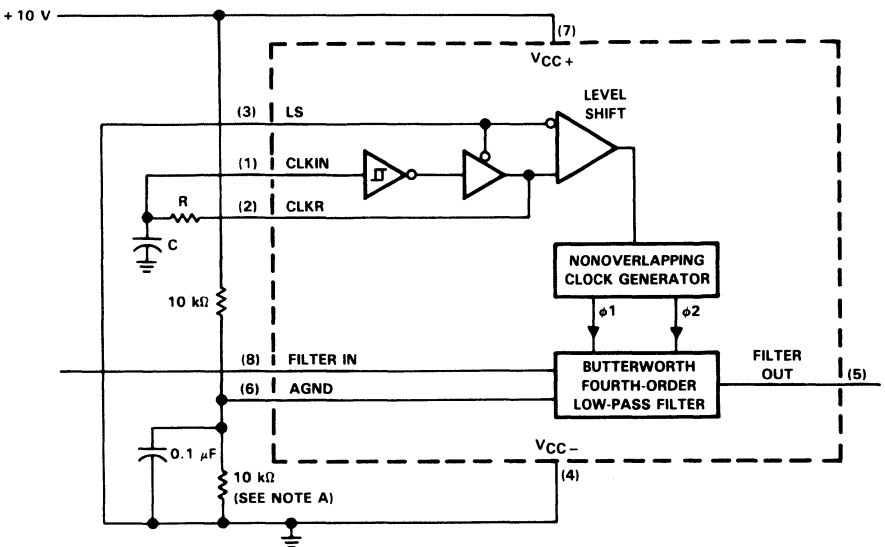


FIGURE 2. TTL-CLOCK-DRIVEN, DUAL-SUPPLY OPERATION

TYPICAL APPLICATION DATA



$$f_{clock} = \frac{1}{RC \times \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

For V_{CC} = 10 V,

$$f_{clock} = \frac{1}{1.69\ RC}$$

NOTE A: The AGND terminal must be biased to mid-supply.

FIGURE 5. SELF-CLOCKING THROUGH SCHMITT TRIGGER OSCILLATOR, SINGLE-SUPPLY OPERATION

TYPICAL APPLICATION DATA

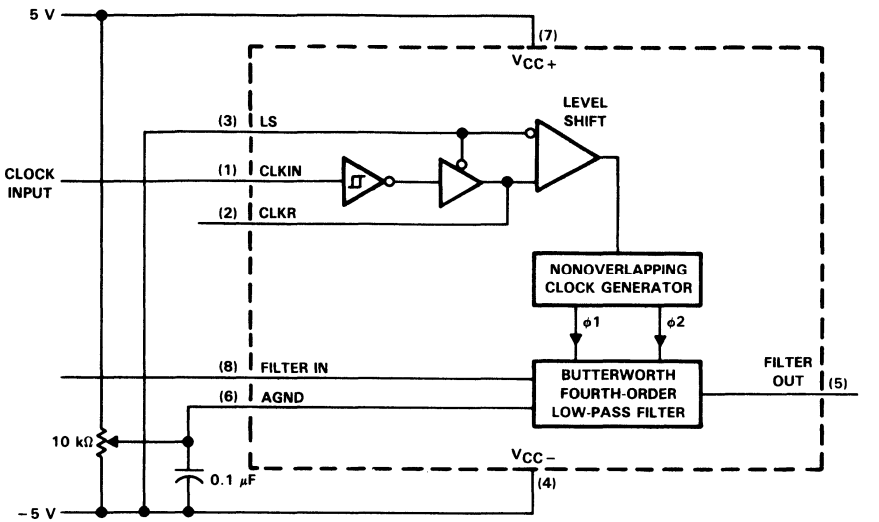
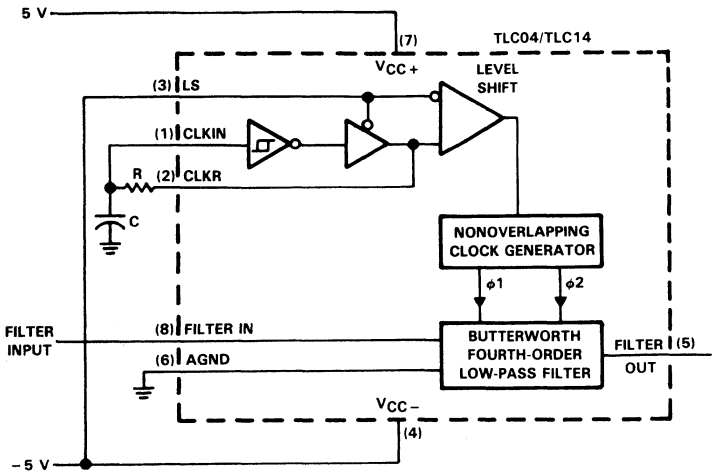


FIGURE 6. DC OFFSET ADJUSTMENT

TYPICAL APPLICATION DATA



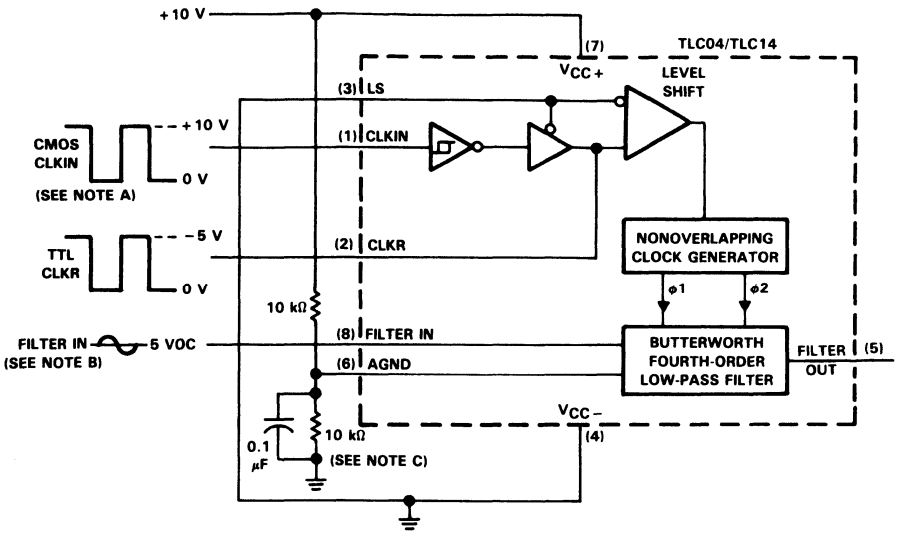
$$f_{clock} = \frac{1}{RC \times \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

For V_{CC} = 10 V,

$$f_{clock} = \frac{1}{1.69\ RC}$$

FIGURE 3. SELF-CLOCKING THROUGH SCHMITT TRIGGER OSCILLATOR, DUAL-SUPPLY OPERATION

TYPICAL APPLICATION DATA



NOTES: A. The external clock used must be of CMOS level because the clock is input to a CMOS Schmitt trigger.
B. The Filter input signal should be dc-biased to mid-supply or ac-coupled to the terminal.
C. The AGND terminal must be biased to mid-supply.

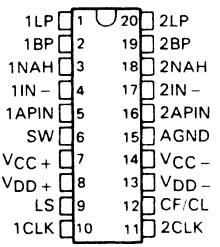
FIGURE 4. EXTERNAL-CLOCK-DRIVEN SINGLE-SUPPLY OPERATION

TLC10, TLC20
UNIVERSAL DUAL SWITCHED-CAPACITOR FILTER

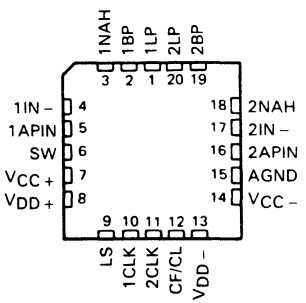
D2952 AUGUST 1986 – REVISED SEPTEMBER 1987

- **Maximum Clock to Center-Frequency Ratio Error**
  - **TLC10 . . . ±0.6%**
  - **TLC20 . . . ±1.5%**
- **Filter Cutoff Frequency Stability Dependent Only on External-Clock Frequency Stability**
- **Minimum Filter Response Deviation Due to External Component Variations over Time and Temperature**
- **Critical-Frequency Times Q Factor Range Up to 200 kHz**
- **Critical-Frequency Operation Up to 30 kHz**
- **Designed to be Interchangeable with:**
  - **National MF10**
  - **Maxim MF10**
  - **Linear Technology LTC1060**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



description

The TLC10 and TLC20 are monolithic general-purpose switched-capacitor CMOS filters each containing two independent active-filter sections. Each device facilitates configuration of Butterworth, Bessel, Cauer, or Chebyshev filter design.

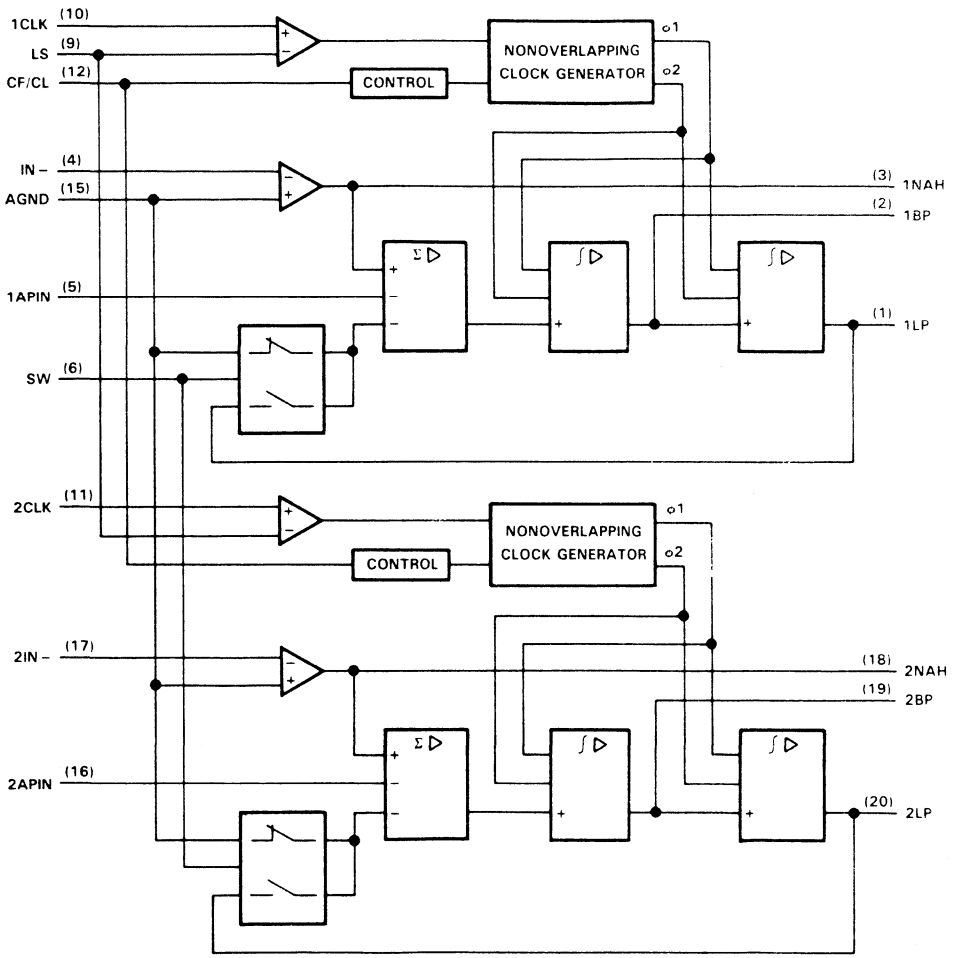
Filter features include cutoff frequency stability that is dependent only on the external clock frequency stability and minimal response deviation over time and temperature. Features also include a critical-frequency times filter quality (Q) factor range of up to 200 kiloHertz.

With external clock and resistors, each filter section can be used independently to produce various second-order functions or both sections can be cascaded to produce fourth-order functions. For functions greater than fourth-order, ICs can be cascaded.

The TLC10 and TLC20 are characterized for operation from 0°C to 70°C.

PIN NAME	PIN NO.	I/O	DESCRIPTION
AGND	15	I	Analog Ground — The noninverting inputs to the input operational amplifiers of both filter sections. This terminal should be at ground for dual supplies or at mid-supply level for single-supply operation.
1APIN 2APIN	5 16	I	All-Pass Inputs — The all-pass input to the summing amplifier of each respective filter section used for all-pass filter applications in configuration modes 1a, 4, 5, and 6. This terminal should be driven from a source having an impedance of less than 1 kilohm. In all other modes, this terminal is grounded. See Typical Application Data.
1BP 2BP	2 19	O	Band-Pass Outputs — The band-pass output of each respective filter section provides the second-order band-pass filter functions.
CF/CL	12	I	Center Frequency/Current Limit — This input terminal provides the option to select the input-clock-to-center-frequency ratio of 50:1 or 100:1 or to limit the current of the IC. For a 50:1 ratio, the CF/CL terminal is set to V_{DD+}. For a 100:1 ratio, the CF/CL terminal is set to ground for dual supplies or to mid-supply level for single-supply operation. For current limiting, the CF/CL terminal is set to V_{DD-}. This aborts filtering and limits the IC current to 0.5 milliamperes.
1CLK 2CLK	10 11	I	Clock Inputs — The clock input to the two-phase nonoverlapping generator of each respective filter section is used to generate the center frequency of the complex pole pair second-order function. Both clocks should be of the same level (TTL or CMOS) and have duty cycles close to 50%, especially when clock frequencies (f_{clock}) greater than 200 kiloHertz are used. At this duty cycle, the operational amplifiers have the maximum time to settle while processing analog samples.
1IN− 2IN−	4 17	I	Inverting Inputs — The inverting input side of the input operational amplifier whose output drives the summing amplifier of each respective filter section.
1LP 2LP	1 20	O	Low-Pass Outputs — The low-pass outputs of the second-order filters.
LS	9	I	Level Shift — This terminal accommodates various input clock levels of bipolar (CMOS) or unipolar (TTL or other clocks) to function with single or dual supplies. For CMOS (±5-volt) clocks, V_{DD-} or ground is applied to the LS terminal. For TTL and other clocks, ground is applied to the LS terminal.
1NAH 2NAH	3	O	Notch, All-Pass, or High-Pass Outputs — The output of each respective filter section can be used to provide either a second-order notch, all-pass, or high-pass output filter function, depending on circuit configuration.
SW	6	I	Switch Input — This input terminal is used to control internal switches to connect either the AGND input or the LP output to one of the inputs of the summing amplifier. The terminal controls both independent filter sections and places them in the same configuration simultaneously. If V_{CC-} is applied to the SW terminal, the AGND input terminal will be connected to one of the inputs of each summing amplifier. If V_{CC+} is applied to the SW terminal, the LP output will be connected to one of the inputs of the summing amplifier.
V_{CC+}	8		Analog positive supply voltage terminal
V_{CC-}	14		Analog negative supply voltage terminal
V_{DD+}	7		Digital positive supply voltage terminal
V_{DD-}	13		Digital negative supply voltage terminal

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Analog supply voltage, $V_{CC\pm}$ (see Note 1) . . . . . ±7 V
Digital supply voltage, $V_{DD\pm}$ . . . . . ±7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: FN or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to the AGND terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Analog supply voltage, $V_{CC\pm}$, (see Note 2)	±4	±5	±6	V
Digital supply voltage, $V_{DD\pm}$, (see Note 2)	±4	±5	±6	V
Clock frequency, f_{clock}, (see Note 3)	0.008		1.0	MHz
Operating free-air temperature, T_A	0		70	°C

NOTES: 2. A common supply voltage source should be used for the analog and digital supply voltages. Although each has separate terminals, they are connected together internally at the substrate. $V_{CC}+$ and $V_{DD}+$ can be connected together at the device terminals or at the supply voltage source. The same is true for $V_{CC}-$ and $V_{DD}-$.
3. Both input clocks should be of the same level type (TTL or CMOS), and their duty cycles should be at 50% above 200 kHz to allow the operational amplifiers the maximum time to settle while processing analog samples.

electrical characteristics at $V_{CC\pm}$ = ±5 V, $V_{DD\pm}$ + = ±5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V_{OPP}	Maximum peak-to-peak output voltage swing		R_L = 3.5 kΩ at all outputs	±4	±4.1		±3.8	±3.9		V
I_{OS}	Short-circuit output current, Pins 3 and 18	Source	See Note 4		2			2		mA
		Sink			50			50		
I_{CC}	Supply current				8	10		8	10	mA

NOTE 4: The short-circuit output current for pins 1, 2, 19, and 20 will be typically the same as pins 3 and 18.

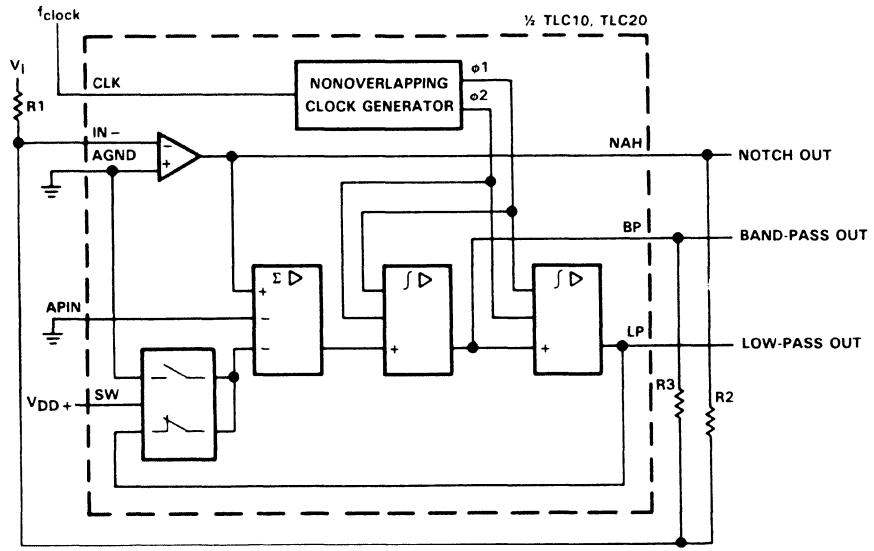
operating characteristics at $V_{CC\pm}$ = ±5 V, $V_{DD\pm}$ = ±5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TLC10			TLC20			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Critical-frequency range	$f_o \times Q \leq 200$ kHz			20	30		20	30		kHz
Maximum clock frequency, f_{clock}	See Note 3			1.0	1.5		1.0	1.5		MHz
Clock to center-frequency ratio	$f_o \leq 5$ kHz, Mode 1,	R3/R2 = 10, See Figure 1	Pin 12 at 5 V	49.64	49.94	50.24	49.24	49.94	50.64	
			Pin 12 at 0 V	98.75	99.35	99.95	97.86	99.35	100.84	
Temperature coefficient of center frequency	$f_o \leq 5$ kHz, Mode 1,	R3/R2 = 20, See Figure 1	Pin 12 at 5 V		±10			±10		ppm/°C
			Pin 12 at 0 V		±100			±100		
Filter Q (quality factor) deviation from 20	$f_o \leq 5$ kHz, Mode 1,	R3/R2 = 20, See Figure 1	Pin 12 at 5 V		±2%	±4%		±2%	±6%	
			Pin 12 at 0 V		±2%	±3%		±2%	±6%	
Temperature coefficient of measured filter Q	$f_o \leq 5$ kHz, Mode 1	R3/R2 = 20,			±500			±500		ppm/°C
Low-pass output deviation from unity gain	R1 = R2 = 10 kΩ Mode 1,	See Figure 1				±2%			±2%	
Crosstalk attenuation					60			60		dB
Clock feedthrough voltage					10			10		mV
Operational amplifier gain-bandwidth product					2.5			2.5		MHz
Operational amplifier slew rate					7			7		V/μs

TYPICAL APPLICATION DATA

modes of operation

The TLC10 and TLC20 are switched-capacitor (sampled-data) filters that closely approximate continuous filters. Each filter section is designed to approximate the response of a second-order variable filter. When the sampling frequency is much larger than the frequency band of interest, the sampled-data filter is a good approximation to its continuous time equivalent. In the case of the TLC10 and TLC20, the ratio is about 50:1 or 100:1. To fully describe their transfer function, a time domain approach would be appropriate. Since this may appear cumbersome, the following application examples are based on the well known frequency domain. It should be noted that in order to obtain the actual filter response, the filter's response must be examined in the z-domain.

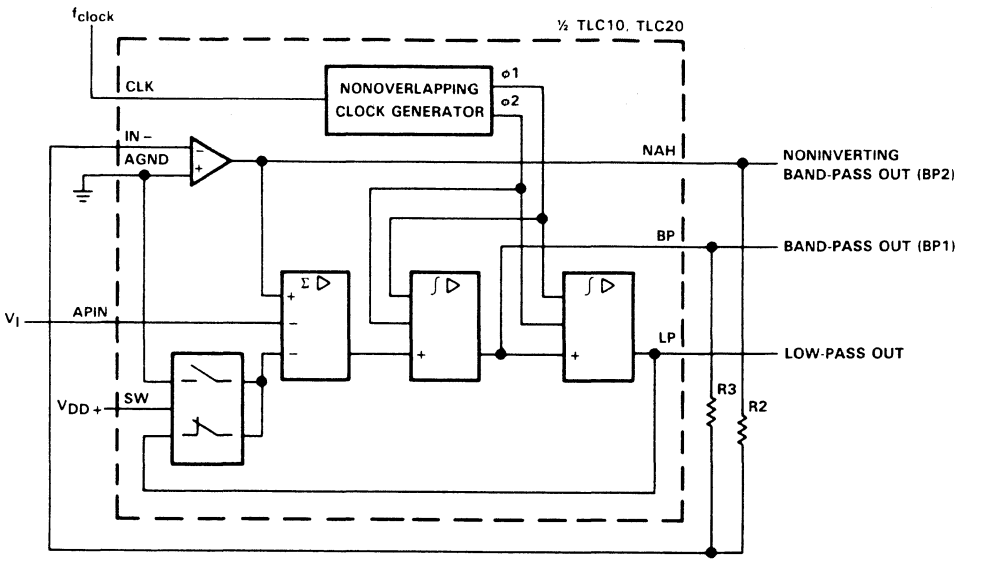


$f_o = f_{clock}/100$ or $f_{clock}/50$
$f_{notch} = f_o$
$H_{OLP} = -R2/R1$ (as $f \rightarrow 0$)
$H_{OBP} = -R3/R1$ (at $f = f_o$)
H_{ON} = notch gain { as f approaches 0 $-R2/R1$; as f approaches 0.5 f_{clock}
$Q = f_o/BW = R3/R2$

Circuit dynamics:
The following expressions determine the swing at each output as a function of the desired Q of the second-order function.
$H_{OLP} = H_{OBP}/Q$ or $H_{OLP} \times Q = H_{ON} \times Q$
H_{OLP} (peak) = $Q \times H_{OLP}$ (for high Qs)

FIGURE 1. MODE 1 FOR NOTCH, BAND-PASS, AND LOW-PASS OUTPUTS: $f_{notch} = f_o$

TYPICAL APPLICATION DATA

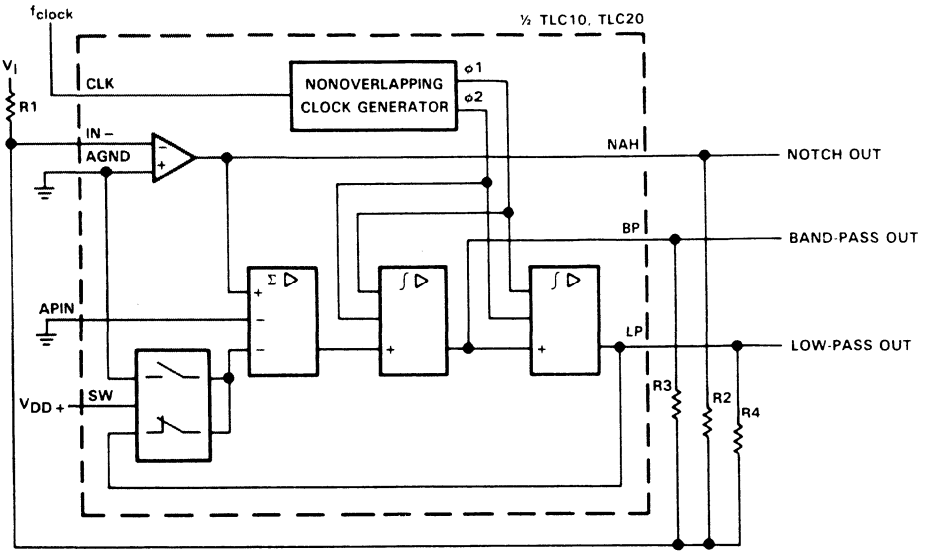


$f_o = f_{clock}/100$ or $f_{clock}/50$
$Q = R3/R2$
$H_{OLP} = -1\,H_{OLP}$ (peak) $= Q \times H_{OLP}$ (for high Qs)
$H_{OBP1} = -R3/R2$
$H_{OBP2} = 1$ (noninverting)

Circuit dynamics:
$H_{OBP1} = Q$

FIGURE 2. MODE 1a FOR NONINVERTING BAND-PASS AND LOW-PASS OUTPUTS

TYPICAL APPLICATION DATA



$f_o = f_{notch} \times \sqrt{R2/R4 + 1}$

$f_{notch} = f_{clock}/100$ or $f_{clock}/50$

$Q = \dfrac{\sqrt{R2/R4 + 1}}{R2/R3}$

H_{OLP} (as f approaches 0) $= \dfrac{-R2/R1}{R2/R4 + 1}$

H_{OBP} (at $f = f_o$) $= -R3/R1$

H_{ON1} (as f approaches 0) $= \dfrac{-R2/R1}{R2/R4 + 1}$

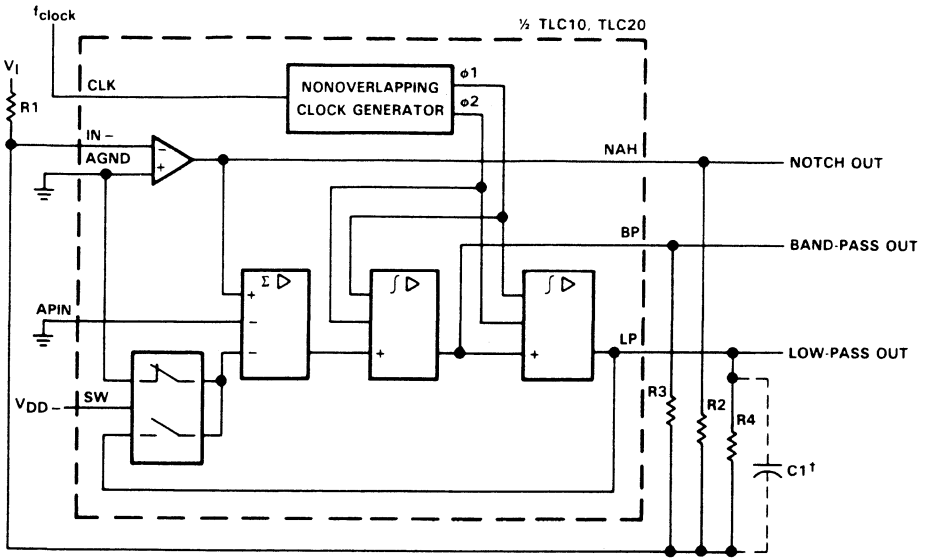
H_{ON2} (as f approaches 0.5 f_{clock}) $= -R2/R1$

Circuit dynamics:

$H_{OBP} = Q\sqrt{H_{OLP} \cdot H_{ON2}} = Q\sqrt{H_{ON1} \cdot H_{ON2}}$

FIGURE 3. MODE 2 FOR NOTCH 2, BAND-PASS, AND LOW-PASS OUTPUTS: $f_{notch} < f_o$

TYPICAL APPLICATION DATA



$f_o = (f_{clock}/100 \text{ or } f_{clock}/50)\sqrt{R2/R4}$

$Q = \sqrt{R2/R4} \times R3/R2$

H_{OHP} (as f approaches 0.5 f_{clock}) = $-R2/R1$

H_{OLP} (as f approaches 0) = $-R4/R1$

H_{OBP} (at $f = f_o$) = $-R3/R1$

Circuit dynamics:

$R2/R4 = H_{OHP}/H_{OLP}$: $H_{OBP} = \sqrt{H_{OHP} \times H_{OLP}} \times Q$

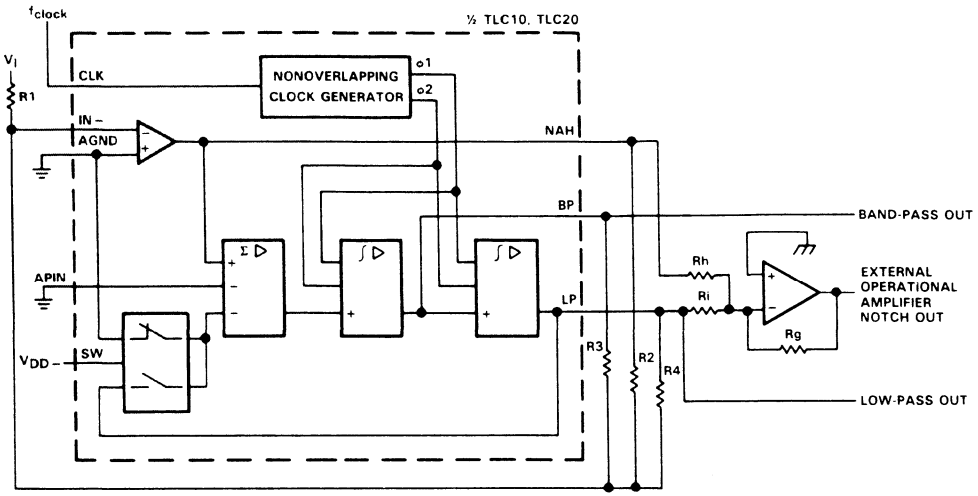
H_{OLP} (peak) = $Q \cdot H_{OLP}$ (for high Qs)

H_{OHP} (peak) = $Q \cdot H_{OHP}$ (for high Qs)

†In this mode, the feedback loop is closed around the input summing amplifier; the finite GBW product of this operational amplifier will cause a slight Q enhancement. If this is a problem, connect a low-value capacitor (10 pF to 100 pF) across R4 to provide some phase lead.

FIGURE 4. MODE 3 FOR HIGH-PASS, BAND-PASS, AND LOW-PASS OUTPUTS

TYPICAL APPLICATION DATA



$f_o = (f_{clock}/100 \text{ or } f_{clock}/50)\sqrt{R2/R4}$

$Q = \sqrt{R2/R4} \times R3/R2$

$H_{OHP} = -R2/R1$

$H_{OBP} = -R3/R1$

$H_{OLP} = -R4/R1$

$f_{notch} = (f_{clock}/100 \text{ or } f_{clock}/50)\sqrt{Rh/Ri}$

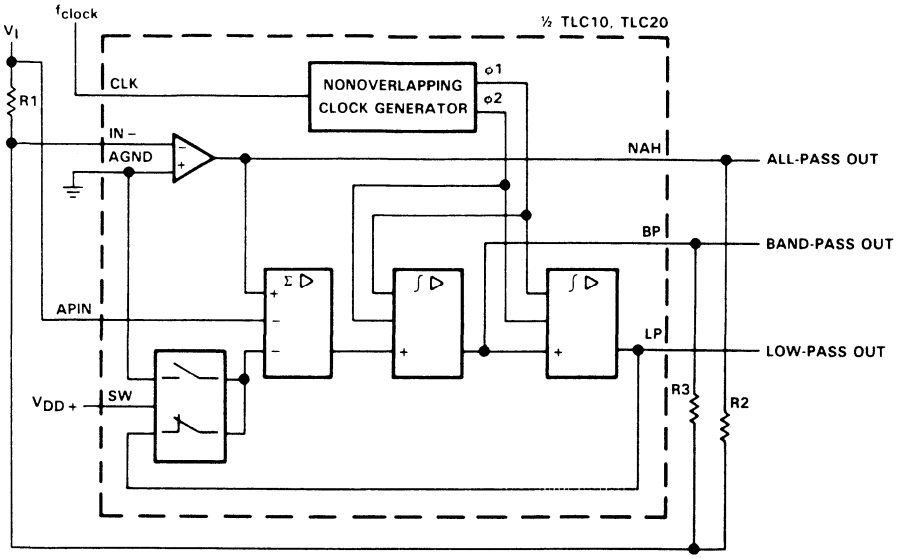
H_{ON} (at $f = f_o$) = . $Q\,(Rg/Ri \times H_{OLP} - Rg/Rh \times HOHP)$

H_{ON1} (as f approaches 0) = $Rg/Ri \times H_{OLP}$

H_{ON2} (as f approaches 0.5 f_{clock}) = $-Rg\,Rh \times H_{OHP}$

FIGURE 5. MODE 3a FOR HIGH-PASS, BAND-PASS, LOW-PASS, AND NOTCH OUTPUTS WITH EXTERNAL OPERATIONAL AMPLIFIER

TYPICAL APPLICATION DATA



$f_o = f_{clock}/100$ or $f_{clock}/50$

$f_z = f_o$ †

$Q = f_o/BW = R3/R2$

$Q_z = R3/R1$

H_{OAP} (at $0 \le f \le 0.5\ f_{clock}$) $= -R2/R1 = -1$
(for AP output R1 = R2)

H_{OLP} (as f approaches 0) $= -(R2/R1 + 1) = -2$

H_{OBP} (at $f = f_o$) $= -R3/R2\ (R2/R1 + 1) = -2\ (R3/R2)$

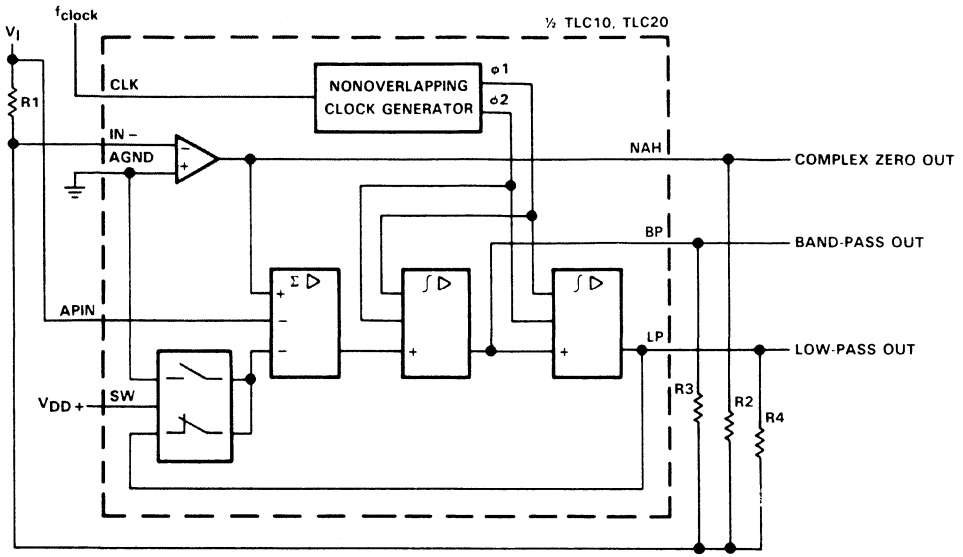
Circuit dynamics:

$H_{OBP} = H_{OLP} \cdot Q = (H_{OAP} + 1)\ Q$

† Due to the sampled-data nature of the filter, a slight mismatch of f_z and f_o occurs causing a 0.4-dB peaking around f_o of the all-pass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

FIGURE 6. MODE 4 FOR ALL-PASS, BAND-PASS, AND LOW-PASS OUTPUTS

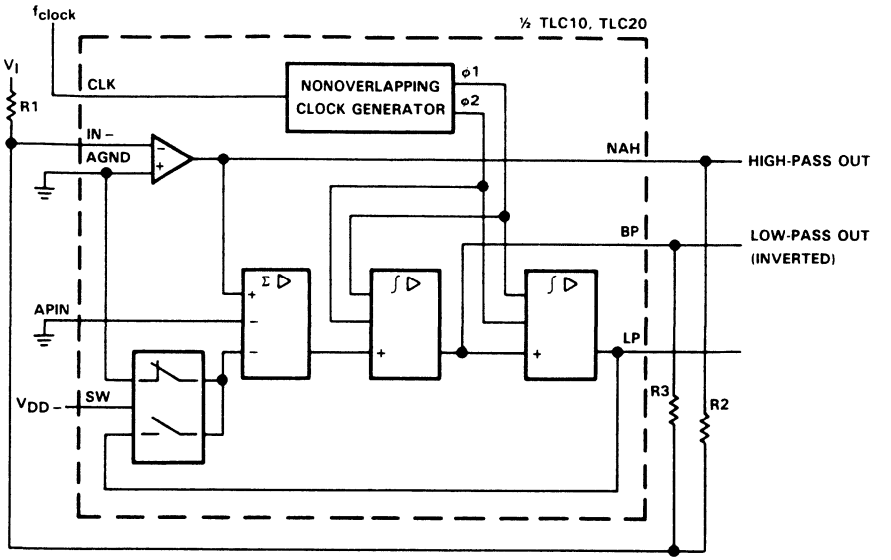
TYPICAL APPLICATION DATA



$f_o = \sqrt{R2/R4 + 1} \times (f_{clock}/100 \text{ or } f_{clock}/50)$
$f_z = \sqrt{1 - R1/R4} \times (f_{clock}/100 \text{ or } f_{clock}/50)$
$Q = \sqrt{R2/R4 + 1} \times R3/R2$
$Q_z = \sqrt{1 - R1/R4} \times R3/R1$
H_{OZ1} (as f approaches 0) = R2 (R4 – R1)/R1 (R2 + R4)
H_{OZ2} (as f approaches 0.5 f_{clock}) = R2/R1
$H_{OBP} = (R2/R1 + 1) \times R3/R2$
$H_{OLP} = (R2 + R1)/(R2 + R4) \times R4/R1$

FIGURE 7. MODE 5 FOR NUMERATOR COMPLEX ZEROS, BAND-PASS, AND LOW-PASS OUTPUTS

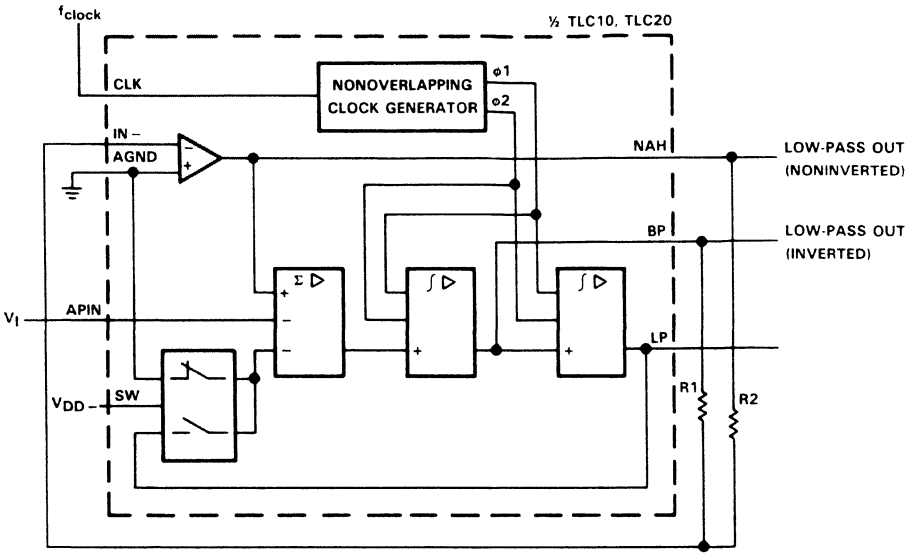
TYPICAL APPLICATION DATA



f_c = R2/R3 (f_{clock}/100 or f_{clock}/50)
H_{OLP} = – R3/R1
H_{OHP} = – R2/R1

FIGURE 8. MODE 6 FOR SINGLE-POLE HIGH-PASS AND LOW-PASS OUTPUT

TYPICAL APPLICATION DATA



f_c = R2/R3 • (f_{clock}/100 or f_{clock}/50)
H_{OLP1} = 1 (noninverting)
H_{OLP2} = –R3/R2

FIGURE 9. MODE 6a FOR SINGLE-POLE LOW-PASS OUTPUT (INVERTED AND NONINVERTED)

TYPICAL APPLICATION DATA

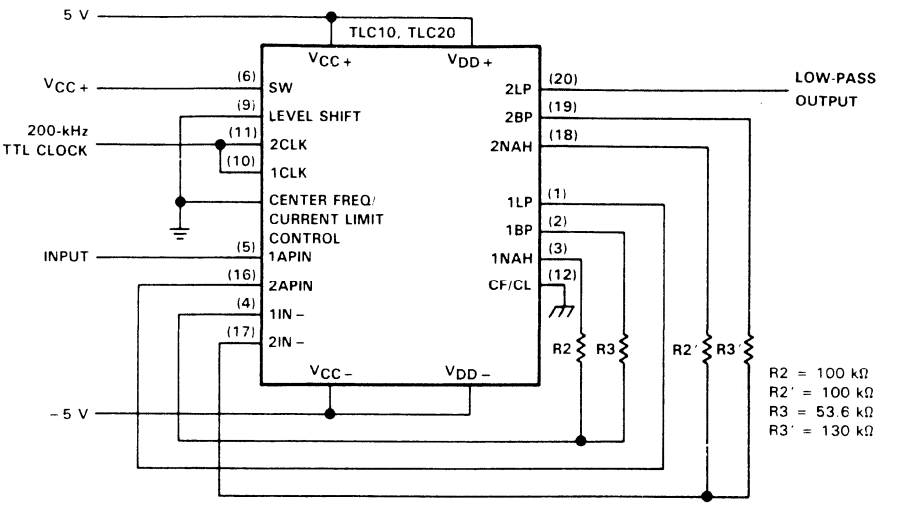
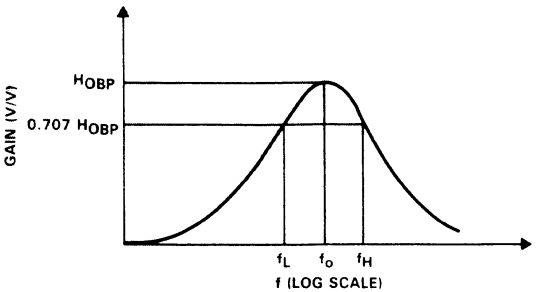


FIGURE 10. FOURTH-ORDER 2-kHz LOW-PASS BUTTERWORTH FILTER

filter terminology

f_C	The cutoff frequency of the low-pass or high-pass filter output
f_{clock}	The input clock frequency to the device
f_{notch}	The notch frequency of the notch output
f_O	The center frequency of the complex pole pair second-order function
f_Z	The center frequency of the complex zero pair
H_{OBP}	The band-pass output voltage gain (V/V) at the band-pass center frequency
H_{OHP}	The high-pass output voltage gain (V/V) as the frequency approaches 0.5 f_{clock}
H_{OLP}	The low-pass output voltage gain (V/V) as the frequency approaches 0
H_{ON}	The notch output voltage gain (V/V) at the notch frequency
H_{ON1}	The low-side notch output voltage gain as the frequency approaches 0
H_{ON2}	The high-side notch output voltage gain as the frequency approaches 0.5 f_{clock}
H_{OZ1}	Gain at complex zero output (as f → 0 Hz)
H_{OZ2}	Gain at complex zero output (as f approaches 0.5 f_{clock})
Q	The quality factor of the complex pole pair second-order function. Q is the ratio of f_O to the 3-dB bandwidth of the band-pass output. The value of Q also affects the possible peaking of the low-pass and high-pass outputs.
Q_Z	The quality factor of the complex zero pair, if such a complex pair exists. This parameter is used when an all-pass filter output is desired.

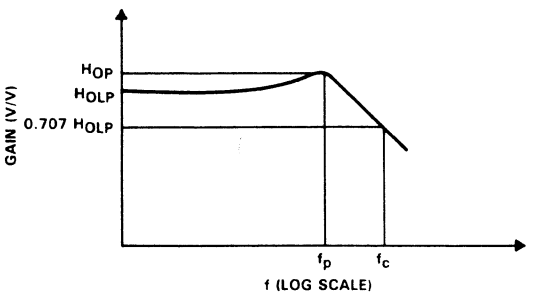


$$Q = \frac{f_o}{f_H - f_L} \; ; \; f_o = \sqrt{f_L f_H}$$

$$f_L = f_o \left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

$$f_H = f_o \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

FIGURE 11. BAND-PASS OUTPUT

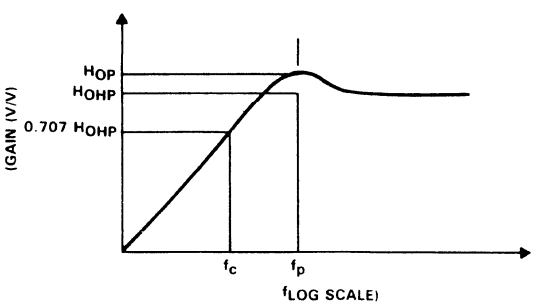


$$f_c = f_o \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_p = f_o \sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 12. LOW-PASS OUTPUT



$$f_c = f_o \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 - 1}} \right]^{-1}$$

$$f_p = f_o \times \left[\sqrt{1 - \frac{1}{2Q^2}} \right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

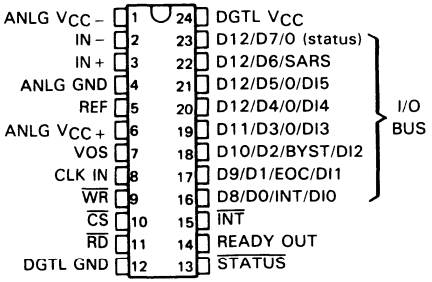
FIGURE 13. HIGH-PASS OUTPUT

TLC1205A, TLC1205B, TLC1225A, TLC1225B
SELF-CALIBRATING 12-BIT-PLUS-SIGN UNIPOLAR OR BIPOLAR ANALOG-TO-DIGITAL CONVERTERS

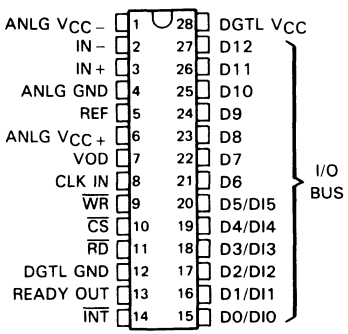
D2982, FEBRUARY 1987

- **ADVANCED LinCMOS™ Technology**
- **Self-Calibration Eliminates Expensive Trimming at Factory and Offset Adjustment in the Field**
- **12-Bit Plus Sign Unipolar or Bit Bipolar**
- **± ½ and ± 1 LSB Linearity Error in Unipolar Configuration**
- **10 μs Conversion Time (Mode 2) (clock = 2.6 MHz)**
  20 μs Conversion Time (Mode 1) (clock = 2.6 MHz)
- **Compatible with All Microprocessors**
- **True Differential Analog Voltage Inputs**
- **0 to 5 V Analog Voltage Range with Single 5-V Supply (Unipolar Configuration)**
- **−5 V to 5 V Analog Voltage Range with ±5-V Supplies (Bipolar Configuration)**
- **Low Power . . . 25 mW Maximum**
- **Replaces National Semiconductor ADC1205 and ADC1225 in Mode 1 Operation**

TLC1205
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



TLC1225
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



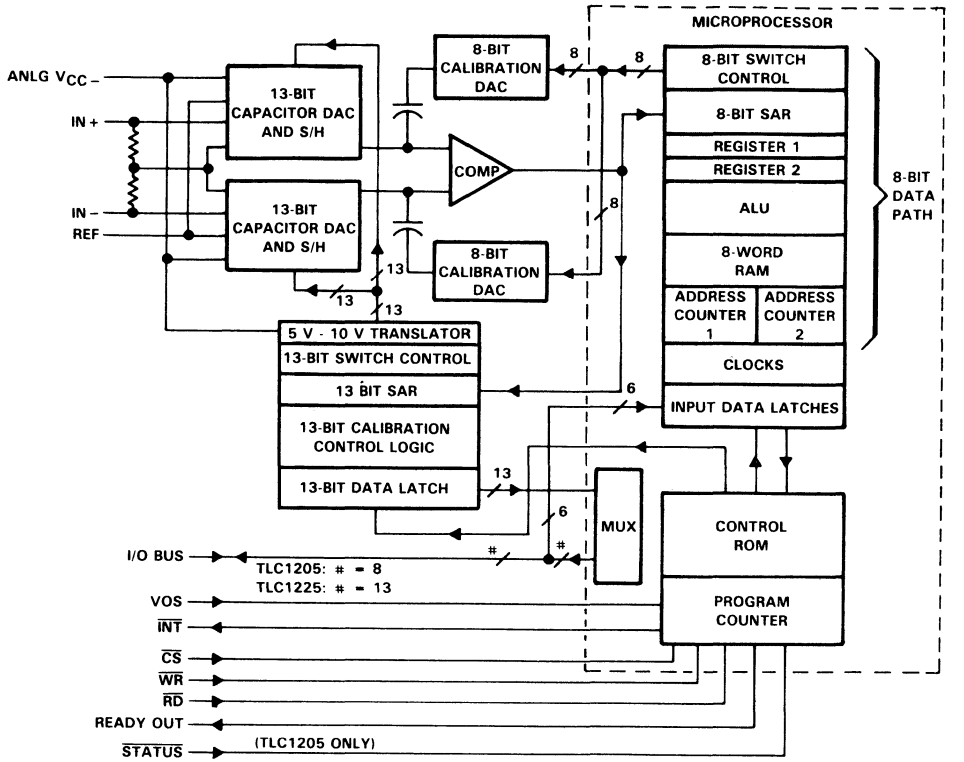
description

The TLC1205 and TLC1225 converters are manufactured with Texas Instruments highly efficient ADVANCED LinCMOS™ technology. Either of the TLC1205 or TLC1225 CMOS analog-to digital converters can be operated as a unipolar or bipolar converter. A unipolar input (0 to 5 V) can be accommodated with a single 5-volt supply, while a bipolar input (−5 V to 5 V) requires the addition of a 5-volt negative supply. Conversion is performed via the successive-approximation method. The 24-pin TLC1205 outputs the converted data in two 8-bit bytes, while the TLC1225 outputs the converted data in a parallel word and interfaces directly to a 16-bit data bus. Negative numbers are given in the 2's complement data format. All digital signals are fully TTL and CMOS compatible.

These converters utilize a self-calibration technique by which seven of the internal capacitors in the capacitive ladder of the A/D conversion circuitry can be automatically or manually calibrated. If the converters are operated in Mode 1, one of the seven internal capacitors is calibrated during the first part of the conversion sequence. For example, one capacitor is calibrated during the first conversion. The next capacitor is calibrated during the second conversion. If the converters are operated in Mode 2, the internal capacitors are calibrated during a nonconversion, capacitor-calibrate cycle in which all seven of the internal capacitors are calibrated at the same time. A Mode 2 conversion requires only 10 μs (2.6 MHz clock) after the nonconversion, capacitor-calibrating cycle has been completed. The calibration or conversion cycle may be initiated at any time by issuing the proper address to the data bus. The self-calibrating techniques eliminate the need for expensive trimming of thin-film resistors at the factory and provide excellent performance at low cost.

ADVANCED LinCMOS™ is a trademark of Texas Instruments Incorporated

functional block diagram



In Mode 1, these converters are replacements for National Semiconductor ADC1205 and ADC1225 integrated circuits. The Mode 1 conversion time for guaranteed accuracy is 51 clock cycles. In the Mode 2 operation, these devices are no longer true replacements. However, the Mode 2 conversion time for guaranteed accuracy is only 26 clock cycles.

The TLC1205AM, TLC1205BM, TLC1225AM, and TLC1225BM are characterized for operation over the full military temperature range of −55°C to 125°C. The TLC1205AI, TLC1205BI, TLC1225AI, and TLC1225BI are characterized for operation from −40°C to 85°C.

operation description

calibration of comparator offset

The following actions are performed to calibrate the comparator offset:

1. The IN+ and IN− inputs are internally shorted together in order that the comparator input is zero. A course comparator offset calibration is performed by storing the offset voltages of the interconnecting comparator stages on the coupling capacitors, which connect the interconnecting stages. Refer to Figure 1. The storage of offset voltages is accomplished by closing all switches and then opening switches A and A′, then switches B and B′, and then C and C′. This process continues until all interconnecting stages of the comparator are calibrated. After this action, some of the comparator offset still remains uncalibrated.

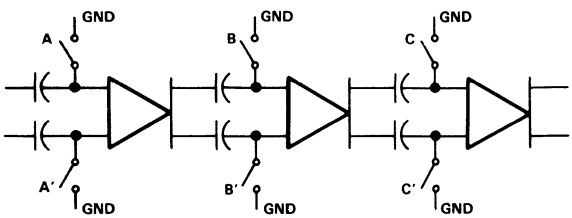


FIGURE 1

2. An A/D conversion is done on the remaining offset with the 8-bit calibration DACs and 8-bit SAR and the result is stored in the RAM.

capacitor calibration of the ADC's Capacitive Ladder

The following actions are performed to calibrate capacitors in the 13-bit DAC's, which comprise the ADC's capacitive ladder:

1. The IN+ and IN− inputs are internally disconnected from the 13-bit capacitive DACs.
2. The most-significant-bit (MSB) capacitor is tied to REF, while the rest of the ladder capacitors are tied to GND. The A/D conversion result for the remaining comparator offset, obtained in step 2 above, is retrieved from the RAM and is input to the 8-bit DACs.
3. Step 1 of the Calibration of Comparator Offset sequence is performed. The 8-bit DAC input is returned to zero and the remaining comparator offset is then subtracted. Thus, the comparator offset is completely corrected.
4. Now the MSB capacitor is tied to GND, while the rest of the ladder capacitors, C_X , are tied to REF. An MSB capacitor voltage error (see Figure 2) on the comparator output will occur if the MSB capacitor does not equal the sum of the other capacitors in the capacitive ladder. This error voltage is converted to an 8-bit word from which a capacitor error is computed and stored in the RAM.
5. The capacitor voltage error for the next most significant capacitor is calibrated by keeping the MSB capacitor grounded and then performing the above Steps 1 - 4 while using the next most significant capacitor in lieu of the MSB capacitor. The seven most significant capacitors can be calibrated in this manner.

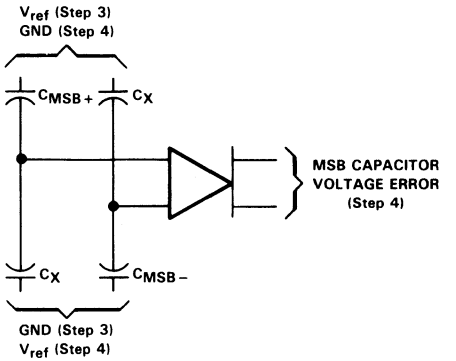


FIGURE 2

analog-to-digital conversion

The following steps are performed in the analog-to-digital conversion process:

1. Step 1 of the Calibration of Comparator Offset Sequence is performed. The A/D conversion result for the remaining comparator offset, which was obtained in Step 2 of the Calibration of Comparator Offset, is retrieved from the RAM and is input to the 8-bit DACs. Thus the comparator offset is completely corrected.
2. IN+ and IN− are sampled onto the 13-bit capacitive ladders.
3. The 13-bit analog-to-digital conversion is performed. As the successive-approximation conversion proceeds successively through the seven most significant capacitors, the error for each of these capacitors is recovered from the RAM and accumulated in a register. This register controls the 8-bit DACs so the total accumulated error for these capacitors is subtracted out during the conversion process.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (ANLG V_{CC+} and DGTL V_{CC}) (see Note 1) . . . . . 15 V
Supply voltage, ANLG V_{CC-} . . . . . −15 V
Control and Clock input voltage range . . . . . −0.3 V to +15 V
Analog input (IN+, IN−) voltage range,
V_{I+} and V_{I-} . . . . . ANLG V_{CC-} −0.3 V to ANLG V_{CC+} + 0.3 V
Reference voltage range, V_{ref} . . . . . −0.3 V to ANLG V_{CC+} + 0.3 V
Mode select voltage range, VOS . . . . . −0.3 V to ANLG V_{CC+} + 0.3 V
Output voltage range . . . . . −0.3 V to DGTL V_{CC} + 0.3 V
Input current (per pin) . . . . . ±5 mA
Input current (per package) . . . . . ±20 mA
Operating free-air temperature range:
TLC1205AM, TLC1205BM, TLC1225AM, TL1225BM . . . . . −55°C to 125°C
TLC1205AI, TLC1205BI, TLC1225AI, TLC1225BI . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: N package . . . . . 260°C

Note 1: All analog voltages are referred to ANLG GND and all digital voltages are referred to DGTL GND.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage	ANLG V_{CC+}	4.5	6	V
	ANLG V_{CC-}	−5.5	ANLG GND	
	DGTL V_{CC}	4.5	6	
High-level input voltage, V_{IH}, all digital inputs except CLK IN (V_{CC} = 4.75 V to 5.25 V)		2		V
Low level input voltage, V_{IL}, all digital inputs except CLK IN (V_{CC} = 4.75 V to 5.25 V)			0.8	V
Analog input voltage, V_{I+}, V_{I-}	Bipolar range	ANLG V_{CC-} − 0.05	ANLG V_{CC+} + 0.05	V
	Unipolar range	ANLG GND − 0.05	ANLG V_{CC+} + 0.05	
Clock input frequency, f_{clock}		0.3	2.6	MHz
Clock duty cycle		40%	60%	
Pulse duration, $\overline{CS}$ and $\overline{WR}$ both low, t_w ($\overline{CS}$•$\overline{WR}$)		350		ns
Setup time before $\overline{WR}$↑ or $\overline{CS}$↑, t_{su}			100	ns
Hold time after $\overline{WR}$↑ or $\overline{CS}$↑, t_h			20	ns
Operating free-air temperature, T_A	TLC1205AM, TLC1225AM TLC1205BM, TLC1225BM	−55	125	°C
	TLC1205AI, TLC1225AI TLC1205BI, TLC1225BI	−40	85	

electrical characteristics over recommended operating free-air temperature range, ANLG V_{CC+} = DGTL V_{CC} = V_{ref} = 5 V, ANLG V_{CC-} = −5 V (for bipolar input range), ANLG V_{CC-} = ANLG GND (for unipolar input range) (unless otherwise noted) (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	DGTL V_{CC} = 4.75 V	I_O = −1.8 mA	2.4		V
			I_O = −50 μA	4.5		
V_{OL}	Low-level output voltage	DGTL V_{CC} = 4.75 V,	I_O = 8 mA		0.4	V
V_{T+}	Clock positive-going threshold voltage			2.7	3.5	V
V_{T-}	Clock negative-going threshold voltage			1.4	2.1	V
V_{hys}	Clock input hysteresis	$V_{T+}min - V_{T-}max$		0.6		V
		$V_{T+}max - V_{T-}min$			2.1	
R_{ref}	Input resistance, REF terminal			1	10	MΩ
I_{IH}	High-level input current	V_I = 5 V			1	μA
I_{IL}	Low-level input current	V_I = 0			−1	μA
I_{OZ}	High-impedance-state output leakage current	V_O = 0			−3	μA
		V_O = 5 V			3	
I_O	Output current	V_O = 0			−6	mA
		V_O = 5 V			8	
DGTL I_{CC}	Supply current from DGTL V_{CC}	f_{clk} = 2.6 MHz,	$\overline{CS}$ high		3	mA
ANLG I_{CC+}	Supply current from ANLG V_{CC+}	f_{clk} = 2.6 MHz,	$\overline{CS}$ high		3	mA
ANLG I_{CC-}	Supply current from ANLG V_{CC-}	f_{clk} = 2.6 MHz,	$\overline{CS}$ high		−3	mA

NOTE 1: Bipolar input range is defined as: V_{I+} = −5.05 V to +5.05 V, V_{I-} = −5.05 V to +5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V. The unipolar input voltage range is defined as: V_{I+} = −0.05 V to 5.05 V, V_{I-} = −0.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V.

operating characteristics over recommended operating free-air temperature range, ANLG V_{CC+} = DGTL V_{CC} = V_{ref} = 5 V, ANLG V_{CC-} = −5 V (for bipolar input range), ANLG V_{CC-} = ANLG GND (for unipolar input range), f_{clock} = 2.6 MHz (unless otherwise noted)(see Note 1)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
Linearity error			Unipolar input range	TLC1205A, TLC1225A		±1	LSB
				TLC1205B, TLC1225B		±0.5	
			Bipolar input range	TLC1205A, TLC1225A		±2	
				TLC1205B, TLC1225B		±1.5	
Zero error						±0.5	LSB
Adjusted positive and negative full-scale error (see Note 2)			Unipolar input range			±1	LSB
Adjusted positive and negative full-scale error (see Note 3)			Bipolar input range			±1	LSB
Temperature coefficient of gain						15	ppm/°C
Temperature coefficient of offset point						1.5	ppm/°C
k_{SVS}	Supply voltage sensitivity	Zero error	ANLG V_{CC+} = 5 V ± 5%, ANLG V_{CC-} = −5 V ± 5%, DGTL V_{CC} = 5 V ± 5%			±0.75	LSB
		Positive and negative full-scale error				±0.75	
		Linearity error				±0.25	
t_c	Conversion time	Mode 1				51	$\frac{1}{f_{clk}}$
		Mode 2				26	
t_a	Access time (delay from falling edge of $\overline{CS}$•$\overline{RD}$ to data output)		C_L = 100 pF			210	ns
t_{dis}	Disable time, output (delay from rising edge of $\overline{RD}$ to high-impedance state		R_L = 10 kΩ,	C_L = 10 pF		260	ns
			R_L = 2 kΩ,	C_L = 100 pF		290	
$t_{d(READY)}$	$\overline{RD}$ or $\overline{WR}$ to READY OUT delay					400	ns
$t_{d(INT)}$	$\overline{RD}$ or $\overline{WR}$ to reset of $\overline{INT}$ delay					400	ns

NOTES: 1. Bipolar input range is defined as: V_{I+} = −5.05 V to +5.05 V, V_{I-} = −5.05 V to +5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V. The unipolar input voltage range is defined as: V_{I+} = −0.05 V to 5.05 V, V_{I-} = −0.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V.
2. See section — Positive and Negative Full-Scale Adjustment, Unipolar Inputs.
3. See section — Positive and Negative Full-Scale Adjustment, Bipolar Inputs.

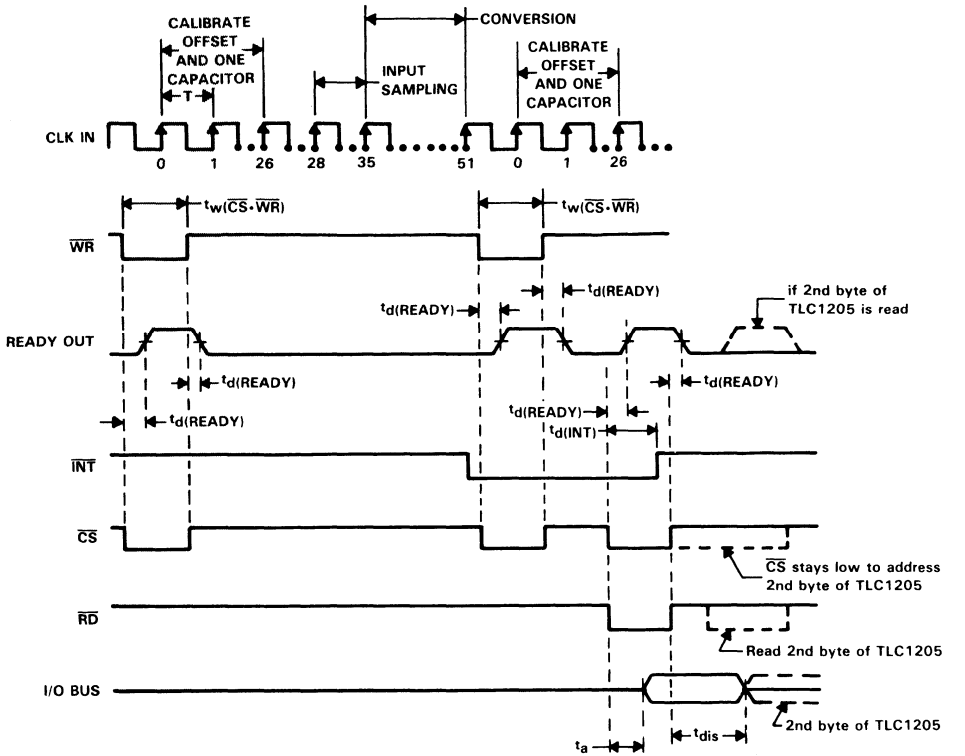


FIGURE 3. MODE 1 TIMING DIAGRAM

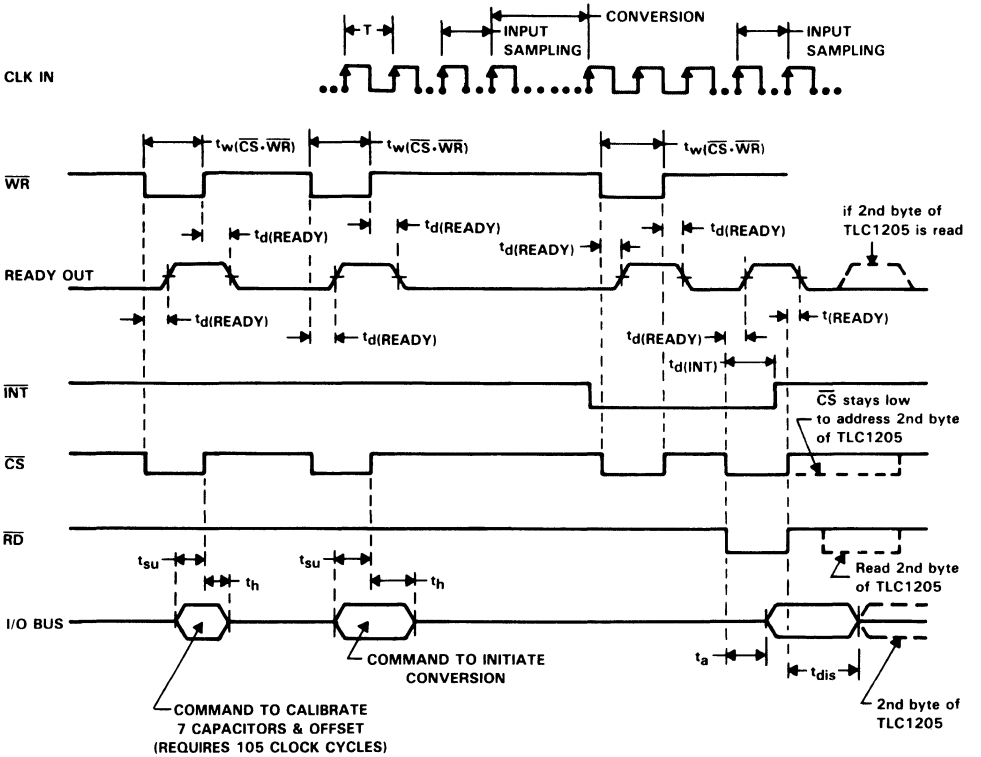


FIGURE 4. MODE 2 TIMING DIAGRAM

PARAMETER MEASUREMENT INFORMATION

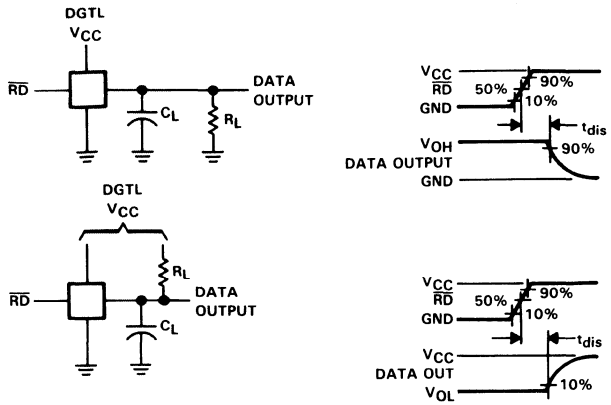


FIGURE 5. LOAD CIRCUITS AND WAVEFORMS

PRINCIPLES OF OPERATION

The following information is categorized into Mode 1 and Mode 2 groupings to allow the designer to concentrate on a particular mode of interest

power-up calibration sequence

Mode 1

When the chip is powered-up, the internal capacitors are automatically calibrated as part of the power-up sequence. This initial calibration sequence requires 105 clock cycles. The chip will not perform an A/D conversion during this calibration sequence.

Mode 2

Power-Up calibration is not automatic and calibration is initiated by writing control words to the six least significant bits of the data bus. If addressed or initiated, conversion can begin after the first clock cycle. However, full A/D conversion accuracy is not guaranteed until after internal capacitor calibration.

conversion start sequence

Mode 1

The conversion sequence is initiated when $\overline{CS}$ and $\overline{WR}$ are both low.

Mode 2

The writing of the conversion command word to the six least significant bits of the data bus, when either $\overline{CS}$ or $\overline{WR}$ goes high, initiates the conversion sequence.

analog sampling sequence

Mode 1

Sampling of the input signal occurs during clock cycles 29 thru 35 of the conversion sequence.

Mode 2

Sampling of the input signal occurs during clock cycles 4 thru 10 of the conversion sequence.

completed A/D conversion

When $\overline{INT}$ goes low, conversion is complete and the A/D result can be read. A new conversion can begin immediately.

Mode 1

The A/D conversion is complete at the end of clock cycle 51 of the conversion sequence.

Mode 2

The A/D conversion is complete at the end of clock cycle 26 of the conversion sequence.

aborting a conversion in process and beginning a new conversion

Mode 1 and Mode 2

If a conversion is initiated while a conversion sequence is in process, the ongoing conversion will be aborted and a new conversion sequence will begin.

Mode 1

If the new conversion is started before the Analog Sampling begins (see Analog Sampling Sequence section and the Mode 1 Timing Diagram), the particular internal capacitor that was being calibrated during the aborted conversion sequence will be calibrated during the new conversion sequence. Otherwise, the next internal capacitor will be calibrated during the new conversion sequence.

reading the conversion result

TLC1205

Upon activating the required control signals to read the conversion result or status information, the appropriate pins are brought out of a high-impedance state and drive the data bus with the proper information. These pins are D12/D7/0 through D8/D0/INT/DI0.

If $\overline{STATUS}$, $\overline{CS}$, and $\overline{RD}$ are all low, status information can be read. The format of the conversion result and status information and the respective pins for output are presented in Table 1.

TABLE 1

BYTES	$\overline{\text{STATUS}}$	$\overline{\text{CS}}$	$\overline{\text{RD}}$	I/O BUS							
				D12/ D7/ 0	D12/ D6/ SARS	D12/ D5/ DI5	D12/ D4/ DI4	D11/ D3/ DI3	D10/ D2/ DI2	D9/ D1/ EOC/ DI1	D8/ D0/ INT/ DI0
MSB	H	L	L	D12	D12	D12	D12	D11	D10	D9	D8
LSB	H	L	↑↓	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	L	L	L	L	SARS	L	L	L	BYST	EOC	INT

The status information is described in Table 2.

TABLE 2

STATUS BIT	BIT DESCRIPTION	TO CLEAR BIT
L	The output has no meaning and is low.	
SARS	A high indicates that conversion is in progress.	
BYST	A low indicates that the next conversion result read will be the most significant conversion byte. A high indicates that the next conversion result read will be the least significant conversion byte. The BYST bit is toggled by reading the conversion result bytes. This bit can be cleared with a "status write" instruction.	By a "status write" or toggled by reading a conversion data byte
EOC	A high indicates that conversion is complete and the conversion data has been transferred to the output latch.	
INT	A high indicates that conversion is complete and the conversion data has been transferred to the output latch and is ready to read.	By reading a conversion data byte, reading the status byte, or a "status write"

With $\overline{\text{STATUS}}$ high, when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ both go low, the most significant byte (MSB) of the conversion result can be read. Then by taking $\overline{\text{RD}}$ high and back low, the least significant byte (LSB) of the conversion result can be read. Subsequently taking $\overline{\text{RD}}$ high and low causes the alternate reading of the MSB and LSB of the conversion result.

The format of the output is extended sign with 2's complement, right justified data. For both unipolar and bipolar cases, the sign bit D12 is low if $V_{I+} - V_{I-}$ is positive and high if $V_{I+} - V_{I-}$ is negative. The format of the conversion result and the respective output pins are presented in Table 2. The format of the conversion result and the respective pins for output are presented in Table 1.

TLC1225

When both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ go low, all 13 bits of conversion data are output to the I/O bus. The format of the output is extended sign with 2's complement, right justified data. Unlike the TLC1205, the TLC1225 does not have internal status information or a $\overline{\text{STATUS}}$ pin. For both unipolar and bipolar cases, the sign bit D12 is low if $V_{I+} - V_{I-}$ is positive and high if $V_{I+} - V_{I-}$ is negative.

general

reset INT

When reading the conversion data, the falling edge of the first low-going combination of $\overline{CS}$ and $\overline{RD}$ will reset $\overline{INT}$. The falling edge of the low-going combination of $\overline{CS}$ and $\overline{WR}$ will also reset $\overline{INT}$.

ready out

For high-speed microprocessors, READY OUT allows the TLC1205 and the TLC1225 to insert a wait state in the microprocessor's read cycle.

status write (TLC1205)

A status write resets the internal logic and status bits and aborts any conversion in process. A status write occurs when $\overline{CS}$, $\overline{WR}$, and $\overline{STATUS}$ are taken low.

reference voltage (V_{ref})

This voltage defines the range for $|V_{I+} - V_{I-}|$. When $|V_{I+} - V_{I-}|$ equals V_{ref}, the highest conversion data value results. When $|V_{I+} - V_{I-}|$ equals 0, the conversion data value is zero. Thus, for a given input, the conversion data changes ratiometrically with changes in V_{ref}.

V_{OS}

This pin is a digital input and is used to select Mode 1 or Mode 2 operation. A logic low selects Mode 1; a logic high selects Mode 2.

In Mode 1, the ICs are true replacements for National Semiconductor's ADC1205 and ADC1225. The ADC1205 and ADC1225 use the VOS pin to adjust zero error. Since the zero error adjustment voltage is below the TLC1205's and TLC1225's maximum acceptable level for a logic low signal, the TLC1205 and TLC1225 ICs are true replacements. Even in Mode 1, the TLC1205's and TLC1225's converted data can be read earlier than the ADC1205's and ADC1225's.

calibration and conversion considerations

Mode 1

Calibration of the seven internal capacitors is an integral part of the A/D conversion. One of the seven internal capacitors is calibrated during the first part of the conversion sequence. For example, one of the capacitors is calibrated during the first conversion. The next capacitor is calibrated during the second conversion. After seven conversions, the pattern for calibrating the internal capacitors repeats. A conversion sequence requires 51 clock cycles.

A conversion is initiated by the low-going combination of $\overline{CS}$ and $\overline{WR}$. The conversion sequence is illustrated in the Mode 1 timing diagram.

Mode 2

Calibration of the internal capacitor and A/D conversion are two separate actions. Each action is independently initiated. Mode 2 conversion is much faster than Mode 1, since Mode 2 conversion is not accompanied by the calibration of internal capacitors. In Mode 2, a calibration command that calibrates all seven internal capacitors is normally issued first. A conversion command then initiates the A/D conversion without calibrating the internal capacitors. Subsequent conversions can be performed by issuing additional conversion commands. The calibration and conversion commands are totally independent from one another and can be initiated in any order. Calibration and conversion commands require 105 and 26 clock cycles, respectively.

The calibrate and conversion commands are initiated by writing control words on the six least significant bits of the data bus. These control words are written into the IC when either $\overline{CS}$ or $\overline{WR}$ goes high. The initiation of these commands is illustrated in the Mode 2 Timing Diagram. The bit patterns for the commands are shown in Table 3.

TABLE 3. MODE 2 CONVERSION COMMANDS

COMMAND	$\overline{CS}$ + $\overline{WR}$	I/O BUS						Required number of clock cycles
		DI5	DI4	DI3	DI2	DI1	DI0	
Conversion	↑	H	L	X	X	X	L	26
Calibrate†	↑	L	X	L	L	L	L	105

†Calibration is lost when clock is stopped.

analog inputs

differential inputs provide common mode rejection

The differential inputs reduce common-mode noise. Common-mode noise is noise common to both IN+ and IN− inputs, such as 60-Hz noise. There is no time interval between the sampling of the IN+ and IN− so these inputs are truly differential. Thus, no conversion errors result from a time interval between the sampling of the IN+ and IN− inputs.

input bypass capacitors

Input bypass capacitors may be used for noise filtering. However, the charge on these bypass capacitors will be depleted during the input sampling sequence when the internal sampling capacitors are charged. Note that the charging of the bypass capacitors through the differential source resistances must keep pace with the charge depletion of the bypass capacitors during the input sampling sequence. Note that higher source resistances reduce the amount of charging current for the bypass capacitors. Also, note that fast, successive conversion will have the greatest charge depletion effect on the bypass capacitors. Therefore, the above phenomenon becomes more significant as source resistances and the conversion rate (i.e., higher clock frequency and conversion initiation rate) increase.

In addition, if the above phenomenon prevents the bypass capacitors from fully charging between conversions, voltage drops across the source resistances will result due to the ongoing bypass capacitor charging currents. The voltage drops will cause a conversion error. Also, the voltage drops increase with higher $|V_{I+} - V_{I-}|$ values, higher source resistances, and lower charge on the bypass capacitors (i.e., faster conversion rate).

For low-source-resistance applications ($R_{source} < 100\,\Omega$), a 0.001-μF bypass capacitor at the inputs will prevent pickup due to the series lead inductance of a long wire. A 100-ohm resistor can be placed between the capacitor and the output of an operational amplifier to isolate the capacitor from the operational amplifier.

input leads

The input leads should be kept as short as possible, since the coupling of noise and digital clock signals to the inputs can cause errors.

power supply considerations

Noise spikes on the V_{CC} lines can cause conversion error. Low-inductance tantalum capacitors ($> 1\,\mu F$) with short leads should be used to bypass ANLG V_{CC} and DGTL V_{CC}. A separate regulator for the TLC1205 or TLC1225 and other analog circuitry will greatly reduce digital noise on the supply line.

positive and negative full-scale adjustment

unipolar inputs

Apply a differential input voltage that is 0.5 LSB below the desired analog full-scale voltage (V_{FS}) and adjust the magnitude of the REF input so that the output code is just changing from 0 1111 1111 1110 to 0 1111 1111 1111. If this transition is desired for a different input voltage, the reference voltage can be adjusted accordingly.

bipolar inputs

First, follow the procedure for the Unipolar case.

Second, apply a differential input voltage so that the digital output code is just changing from 1 0000 0000 0001 to 1 0000 0000 0000. Call this actual differential voltage V_X. The ideal differential voltage for this transition is:

$$-V_{FS} + \frac{V_{FS}}{8192} \quad (1)$$

The difference between the actual and ideal differential voltages is:

$$\text{Delta} = V_X - \left(-V_{FS} + \frac{V_{FS}}{8192}\right) \quad (2)$$

Then apply a differential input voltage of:

$$V_X - \frac{\text{Delta}}{2} \quad (3)$$

and adjust V_{ref} so the digital output code is just changing from 1 0000 0000 0001 to 1 0000 0000 0000. This procedure produces positive and negative full-scale transitions with symmetrical minimum error.

TYPICAL APPLICATIONS

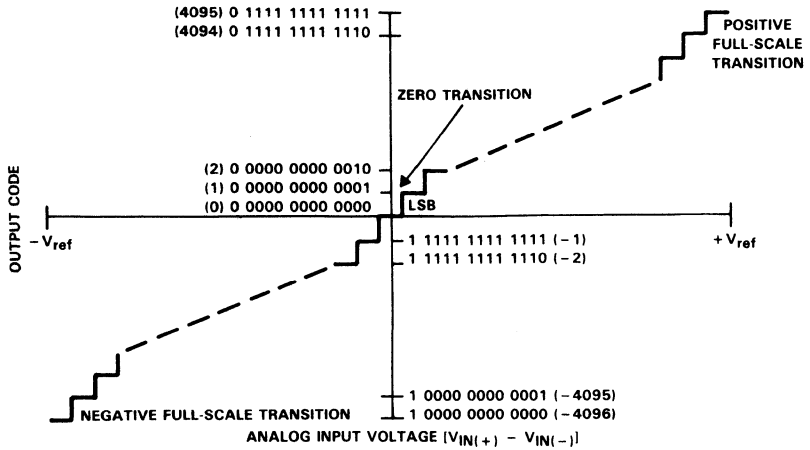
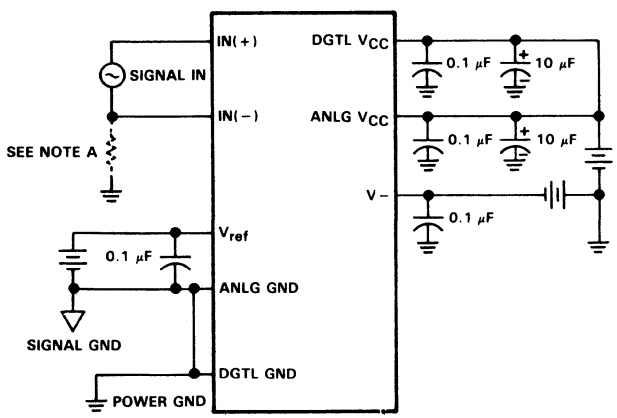


FIGURE 6. TRANSFER CHARACTERISTIC



NOTE: A. The analog input must have some current return path to ANALOG GND.
B. Bypass capacitor leads must be as short as possible.

FIGURE 7. ANALOG CONSIDERATIONS

TYPICAL APPLICATIONS (Continued)

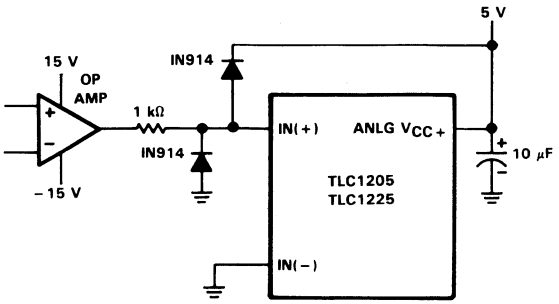
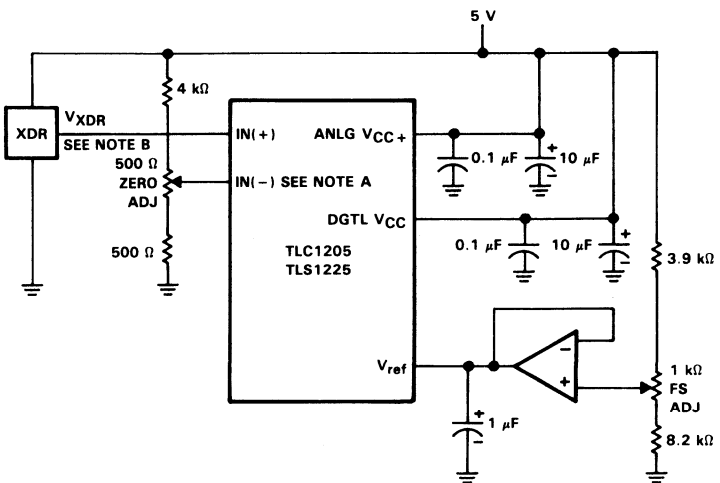


FIGURE 8. INPUT PROTECTION



NOTE: A. $V_{I-} = 0.15 \times$ ANLG V_{CC+}.
B. 15% of ANALOG $V_{CC} \leq V_{XDR} \leq$ 85% of ANALOG V_{CC}.

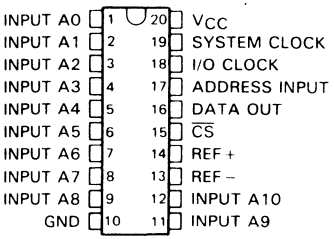
FIGURE 9. OPERATING WITH RATIOMETRIC TRANSDUCERS

D2859, DECEMBER 1985 – REVISED JANUARY 1988

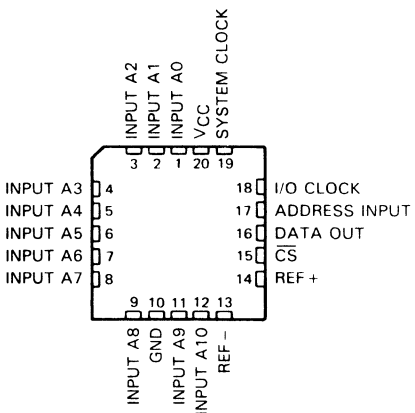
- **LinCMOS™ Technology**
- **10-Bit Resolution A/D Converter**
- **Microprocessor Peripheral or Stand-Alone Operation**
- **On-Chip 12-Channel Analog Multiplexer**
- **Built-In Self-Test Mode**
- **Software-Controllable Sample and Hold**
- **Total Unadjusted Error . . .**
  TLC1540: ±0.5 LSB Max
  TLC1541: ±1.0 LSB Max
- **Pinout and Control Signals Compatible with TLC540 and TLC549 Families of 8-Bit A/D Converters**

TYPICAL PERFORMANCE	
Channel Acquisition Sample Time	5.5 μs
Conversion Time	21 μs
Samples per Second	32×10^3
Power Dissipation	6 mW

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FK OR FN CHIP CARRIER PACKAGE
(TOP VIEW)



description

The TLC1540 and TLC1541 are LinCMOS™ A/D peripherals built around a 10-bit, switched-capacitor, successive-approximation, A/D converter. They are designed for serial interface to a microprocessor or peripheral via a three-state output with up to four control inputs [including independent System Clock, I/O Clock, Chip Select ($\overline{CS}$), and Address Input]. A 2.1-megahertz system clock for the TLC1540 and TLC1541, with a design that includes simultaneous read/write operation, allows high-speed data transfers and sample rates of up to 32,258 samples per second. In addition to the high-speed converter and versatile control logic, there is an on-chip 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal "self-test" voltage, and a sample-and-hold that can operate automatically or under microprocessor control. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The converters incorporated in the TLC1540 and TLC1541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched-capacitor design allows guaranteed low-error conversion (±0.5 LSB for the TLC1540, ±1 LSB for the TLC1541) in 21 microseconds over the full operating temperature range.

The TLC1540 and the TLC1541 are available in FK, FN, J, and N packages. The M-suffix versions are characterized for operation from −55°C to 125°C. The I-suffix versions are characterized for operation from −40°C to 85°C.

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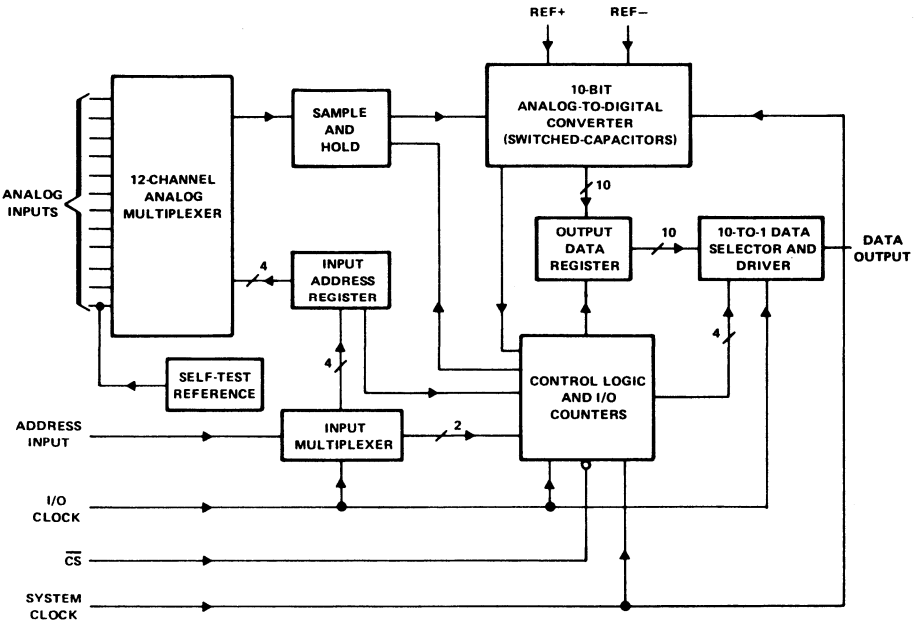
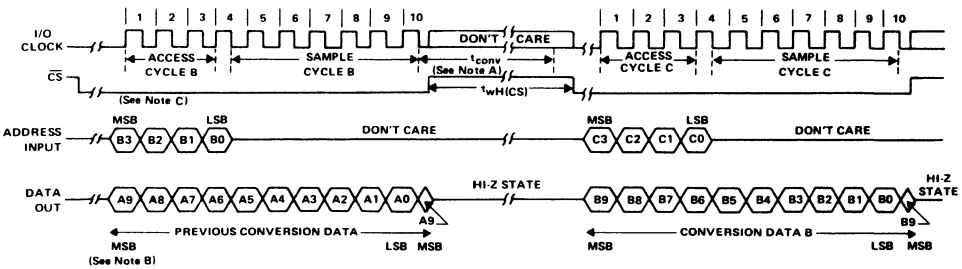
functional block diagram



operating sequence



NOTES: A. The conversion cycle, which requires 44 System Clock periods, is initiated on the 10th falling edge of the I/O Clock↓ after CS↓ goes low for the channel whose address exists in memory at that time. If $\overline{CS}$ is kept low during conversion, the I/O Clock must remain low for at least 44 System Clock cycles to allow conversion to be completed.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining nine bits (A8-A0) will be clocked out on the first nine I/O Clock falling edges.

C. To minimize errors caused by noise at the CS input, the internal circuitry waits for three System Clock cycles (or less) after a chip-select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range (any input)	−0.3 V to V_{CC} + 0.3 V
Output voltage range	−0.3 V to V_{CC} + 0.3 V
Peak input current range (any input)	±10 mA
Peak total input current (all inputs)	±30 mA
Operating free-air temperature range: TLC1540I, TLC1541I	−40°C to 85°C
TLC1540M, TLC1541M	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: N package	260°C

NOTE 1: All voltage values are with respect to digital ground with REF− and GND wired together (unless otherwise noted).

recommended operating conditions

			TLC1540, TLC1541			UNIT
			MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)			2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 2)			−0.1	0	2.5	V
Differential reference voltage, $V_{REF+} - V_{REF-}$ (see Note 2)			1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	V
High-level control input voltage, V_{IH}			2			V
Low-level control input voltage, V_{IL}					0.8	V
Setup time, address bits before I/O CLK↑, $t_{su(A)}$			400			ns
Hold time, address bits after I/O CLK↑, $t_{h(A)}$			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			3			System clock cycles
$\overline{CS}$ high during conversion, $t_{wH(CS)}$			44			System clock cycles
Input/Output clock frequency, $f_{CLK(I/O)}$			0		1.1	MHz
System clock frequency, $f_{CLK(SYS)}$			$f_{CLK(I/O)}$		2.1	MHz
System clock high, $t_{wH(SYS)}$			210			ns
System clock low, $t_{wL(SYS)}$			190			ns
Input/Output clock high, $t_{wH(I/O)}$			404			ns
Input/Output clock low, $t_{wL(I/O)}$			404			ns
Clock transition time (see Note 4)	System	$f_{CLK(SYS)} \le 1048$ kHz			30	ns
		$f_{CLK(SYS)} > 1048$ kHz			20	
	I/O	$f_{CLK(I/O)} \le 525$ kHz			100	ns
		$f_{CLK(I/O)} > 525$ kHz			40	
Operating free-air temperature, T_A		TLC1540M, TLC1541M	−55		125	°C
		TLC1540I, TLC1541I	−40		85	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all "1"s (11111111), while input voltages less than that applied to REF− convert as all "0"s (00000000). For proper operation, REF+ voltage must be at least 1 volt higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 volts.

3. To minimize errors caused by noise at the chip select input, the internal circuitry waits for three System Clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in an address until the minimum chip select setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 microseconds for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 1.1 MHz, $f_{CLK(SYS)}$ = 2.1 MHz

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 16)		V_{CC} = 4.75 V,	I_{OH} = 360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC},	$\overline{CS}$ at V_{CC}			10	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		V_I = V_{CC}			0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0			−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V			0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}			−0.4	−1	
I_{CC} + I_{REF}	Supply and reference current		V_{REF+} = V_{CC},	$\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

operating characteristics over recommended operating free-air temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V, $f_{CLK(I/O)}$ = 1.1 MHz, $f_{CLK(SYS)}$ = 2.1 MHz

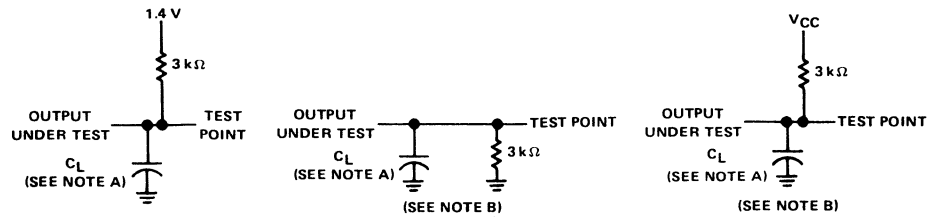
PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
	Linearity error	TLC1540	See Note 5		±0.5	LSB
		TLC1541			±1	
	Zero error	TLC1540	See Notes 2 and 6		±0.5	LSB
		TLC1541			±1	
	Full-scale error	TLC1540	See Notes 2 and 6		±0.5	LSB
		TLC1541			±1	
	Total unadjusted error	TLC1540	See Note 7		±0.5	LSB
		TLC1541			±1	
	Self-test output code		Input A11 address = 1011 (See Note 8)	0111110100 (500)	1000001100 (524)	
t_{conv}	Conversion time		See Operating Sequence		21	μs
	Total access and conversion time		See Operating Sequence		31	μs
t_{acq}	Channel acquisition time (sample cycle)		See Operating Sequence		6	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓			10		ns
t_d	Delay time, I/O clock↓ to data output valid		See Parameter Measurement Information		400	ns
t_{en}	Output enable time				150	ns
t_{dis}	Output disable time				150	ns
$t_{r(bus)}$	Data bus rise time				300	ns
$t_{f(bus)}$	Data bus fall time				300	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 2. Analog input voltages greater than that applied to REF+ convert to all "1"s (11111111), while input voltages less than that applied to REF− convert to all"0"s (00000000). For proper operation, REF+ voltage must be at least 1 volt higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 volts.

5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error comprises linearity, zero, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The A11 analog input signal is internally generated and is used for test purposes.

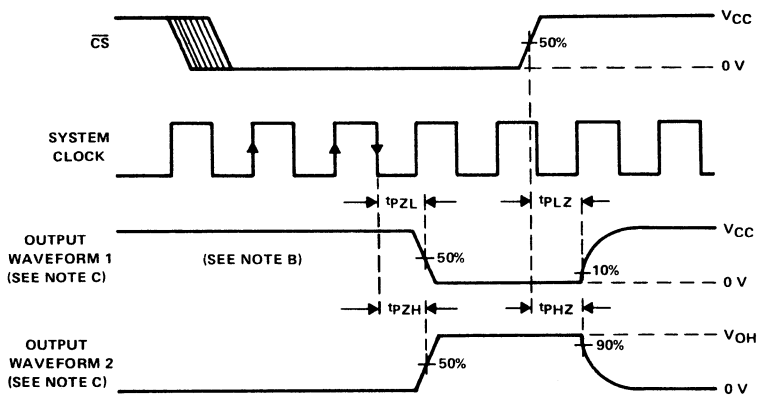
PARAMETER MEASUREMENT INFORMATION



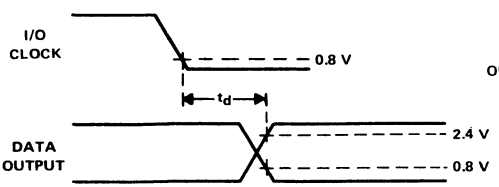
LOAD CIRCUIT FOR t_d, t_r, AND t_f

LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}

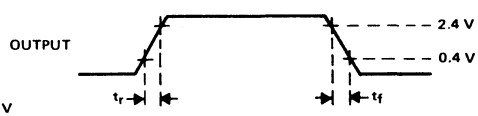
LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME



VOLTAGE WAVEFORM FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

principles of operation

The TLC1540 and TLC1541 are complete data acquisition systems on single chips. Each includes such functions as sample-and-hold, 10-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs; Chip Select ($\overline{CS}$), Address Input, I/O Clock, and System Clock. These control inputs and a TTL-compatible three-state output are intended for serial communications with a microprocessor or microcomputer. The TLC1540 and TLC1541 can complete conversions in a maximum of 21 microseconds, while complete input-conversion-output cycles can be repeated at a maximum of 31 microseconds.

The System and I/O Clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the System Clock input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O Clock. The System Clock will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the Data Output pin is in a three-state condition and the Address Input and I/O Clock pins are disabled. This feature allows each of these pins, with the exception of the $\overline{CS}$ pin, to share a control logic point with their counterpart pins on additional A/D devices when additional TLC1540/1541 devices are used. In this way, the above feature serves to minimize the required control logic pins when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the System Clock after a low $\overline{CS}$ transition, before the low transition is recognized. This technique is used to protect the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result will automatically appear on the Data Out pin.
2. A new positive-logic multiplexer address is shifted in on the first four rising edges of the I/O Clock. The MSB of the address is shifted in first. The negative edges of these four I/O Clock pulses shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample-and-hold begins sampling the newly addressed analog input after the fourth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Five clock cycles are then applied to the I/O pin and the sixth, seventh, eighth, ninth, and tenth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final tenth clock cycle is applied to the I/O Clock pin. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 44 System Clock cycles. After this final I/O Clock cycle, $\overline{CS}$ must go high or the I/O Clock must remain low for at least 44 System Clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O Clock line. If glitches occur on the I/O Clock line, the I/O sequence between the microprocessor/controller and the device will lose synchronization. Also, if $\overline{CS}$ is taken high, it must remain high until the end of the conversion. Otherwise, a valid falling edge of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 44 System Clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

principles of operation (continued)

It is possible to connect the System and I/O Clock pins together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. When $\overline{CS}$ is recognized by the device to be at a low level, the common clock signal is used as an I/O Clock. When $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used to drive the "conversion crunching" circuitry.
2. The device will recognize a $\overline{CS}$ low transition only when the $\overline{CS}$ input changes and subsequently the System Clock pin receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles will not shift in the address because a low $\overline{CS}$ must be recognized before the I/O Clock can shift in an analog channel address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the eighth I/O Clock that has been recognized by the device, so that a $\overline{CS}$ low level will be recognized upon the lowering of the tenth I/O Clock signal that is recognized by the device. Otherwise, additional common clock cycles will be recognized as I/O Clock pulses and will shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample-and-hold begins sampling upon the negative edge of the fourth I/O Clock cycle, the hold function is not initiated until the negative edge of the tenth I/O Clock cycle. Thus, the control circuitry can leave the I/O Clock signal in its high state during the tenth I/O Clock cycle until the moment at which the analog signal must be converted. The TLC1540/TLC1541 will continue sampling the analog input until the tenth falling edge of the I/O Clock. The control circuitry or software will then immediately lower the I/O Clock signal and hold the analog signal at the desired point in time and start conversion.

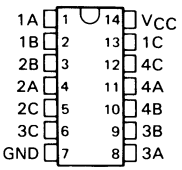
Detailed information on interfacing to most popular microprocessors is readily available from the factory.

TLC4016M, TLC4016I
SILICON-GATE CMOS QUADRUPLE BILATERAL ANALOG SWITCH

D2922, JANUARY 1986

- **High Degree of Linearity**
- **High On-Off Output Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Low On-State Impedance of 50 Ohms Typ at V_{CC} = 9 V**
- **Individual Switch Controls**
- **Extremely Low Input Current**

TLC4016M . . . J OR N PACKAGE
TLC4016I . . . D OR N PACKAGE
(TOP VIEW)



description

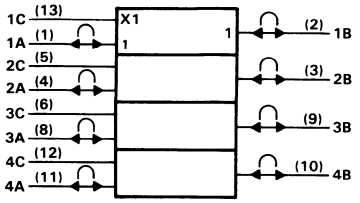
The TLC4016 is a silicon-gate CMOS quadruple analog switch integrated circuit designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 12 volts peak to be transmitted in either direction.

Each switch section has its own enable input control. A high-level voltage applied to this control terminal turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

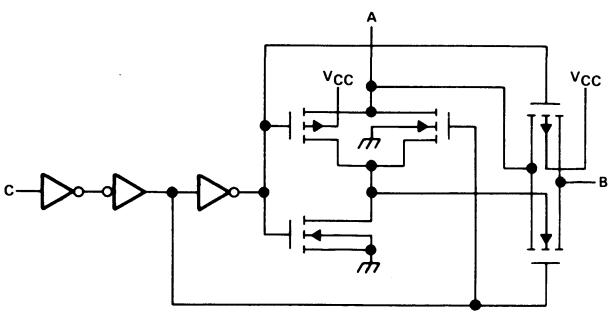
The TLC4016M is characterized for operation from −55°C to 125°C, and the TLC4016I is characterized from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range (see Note 1) . . . . . −0.5 V to 15 V
Control-input diode current ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
I/O port diode current ($V_I < 0$ or $V_{I/O} > V_{CC}$) . . . . . ±20 mA
On-state switch current ($V_{I/O}$ = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 875 mW
Operating free-air temperature, T_A: TLC4016M . . . . . −55°C to 125°C
TLC4016I . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N packages . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. For operation above 25°C free-air temperature, see Dissipation Derating Table.

DISSIPATION DERATING TABLE

Package	Maximum Power Dissipation			Derating Factor
	25°C	85°C	125°C	
D	950 mW	494 mW		7.6 mW/°C
J	1025 mW	533 mW	205 mW	8.2 mW/°C
N	875 mW	455 mW	175 mW	7.0 mW/°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		2†	5	12	V
I/O port voltage, $V_{I/O}$		0		V_{CC}	V
High-level input voltage, V_{IH}	V_{CC} = 2 V	1.5		V_{CC}	V
	V_{CC} = 4.5 V	3.15		V_{CC}	
	V_{CC} = 9 V	6.3		V_{CC}	
	V_{CC} = 12 V	8.4		V_{CC}	
Low-level input voltage, V_{IL}	V_{CC} = 2 V	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	
	V_{CC} = 9 V	0		1.8	
	V_{CC} = 12 V	0		2.4	
Input rise time, t_r	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Input fall time, t_f	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Operating free-air temperature, T_A	TLC4066M	−55		125	°C
	TLC4066I	−40		85	

†With supply voltages at or near 2 volts, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	V_{CC}	TLC4016M			TLC4016I			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
r_{Son}	On-state switch resistance		I_S = 1 mA, V_A = 0 to V_{CC}, See Figure 1	4.5 V		100	220		100	200	Ω
				9 V		50	120		50	105	
				12 V		30	100		30	85	
			I_S = 1 mA, V_A = 0 or V_{CC}, See Figure 1	2 V		120	240		120	215	
				4.5 V		50	120		50	100	
				9 V		35	80		35	75	
				12 V		20	70		20	60	
	On-state switch resistance matching		V_A = 0 to V_{CC}, See Figure 1	4.5 V		10	20		10	20	Ω
				9 V		5	15		5	15	
				12 V		5	15		5	15	
I_I	Control input current		V_I = 0 or V_{CC}	2 V to 6 V			±1			±1	μA
			V_I = 0 or V_{CC}, T_A = 25°C				±0.1			±0.1	
I_{Soff}	Off-state switch leakage current		V_S = ±V_{CC}, See Figure 2	5.5 V		±10	±600		±10	±600	nA
				9 V		±15	±800		±15	±800	
				12 V		±20	±1000		±20	±1000	
I_{Son}	On-state switch leakage current		V_A = 0 or V_{CC}, See Figure 3	5.5 V		±10	±150		±10	±150	nA
				9 V		±15	±200		±15	±200	
				12 V		±20	±300		±20	±300	
I_{CC}	Supply current		V_I = 0 or V_{CC}, I_O = 0	5.5 V		2	40		2	20	μA
				9 V		8	160		8	80	
				12 V		16	320		16	160	
C_i	Input capacitance	A or B		2 V to 12 V		15			15		pF
		C				5	10		5	10	
C_f	Feedthrough capacitance	A to B	V_I = 0	2 V to 12 V		5			5		pF

†All typical values are at T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TLC4016M			TLC4016I			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Propagation delay time, A to B or B to A	See Figure 4	2 V		25	75		25	62	ns
			4.5 V		5	15		5	13	
			9 V		4	14		4	12	
			12 V		3	13		3	11	
t_{on}	Switch turn-on time	R_L = 1 kΩ, See Figures 5 and 6	2 V		32	150		32	125	ns
			4.5 V		8	30		8	25	
			9 V		6	18		6	15	
			12 V		5	15		5	13	
t_{off}	Switch turn-off time	R_L = 1 kΩ, See Figures 5 and 6	2 V		45	252		45	210	ns
			4.5 V		15	54		15	45	
			9 V		10	48		10	40	
			12 V		8	45		8	38	
f_{co}	Switch cutoff frequency (channel loss = 3 dB)		4.5 V		100			100		MHz
			9 V		120			120		
$V_{OCF(PP)}$	Control feedthrough voltage to any switch, peak to peak	See Figure 7	4.5 V			180			180	mV
	Frequency at which crosstalk attenuation between any two switches equals 50 dB	See Figure 8	4.5 V		1			1		MHz

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

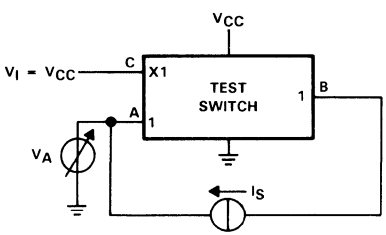
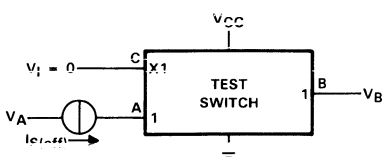


FIGURE 1. ON-STATE RESISTANCE TEST CIRCUIT



$I_S = V_A - V_B$
CONDITION 1: V_A = 0, V_B = V_{CC}
CONDITION 2: V_A = V_{CC}, V_B = 0

FIGURE 2. OFF-STATE SWITCH LEAKAGE CURRENT TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION

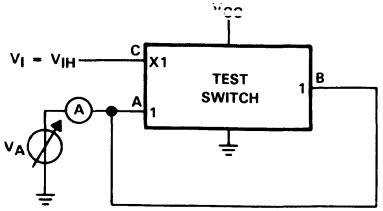
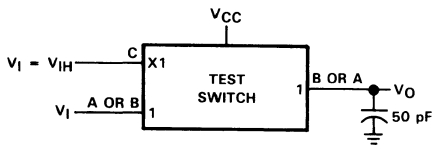
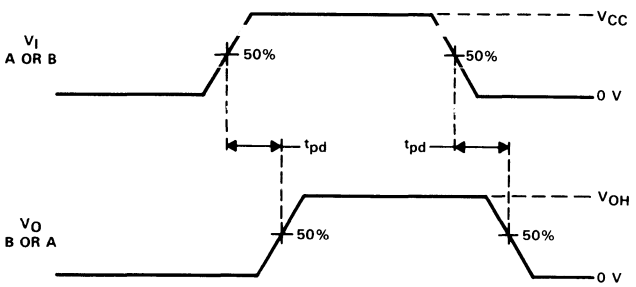


FIGURE 3. ON-STATE SWITCH LEAKAGE CURRENT TEST CIRCUIT



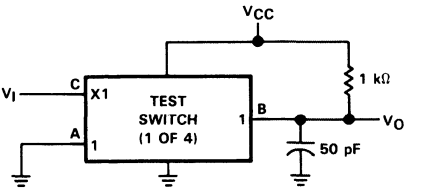
TEST CIRCUIT



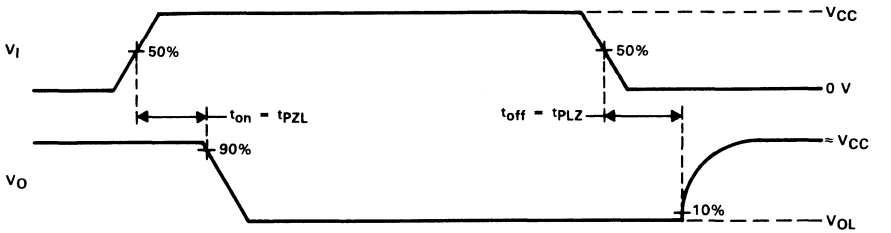
VOLTAGE WAVEFORMS

FIGURE 4. PROPAGATION DELAY TIME, SIGNAL INPUT TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



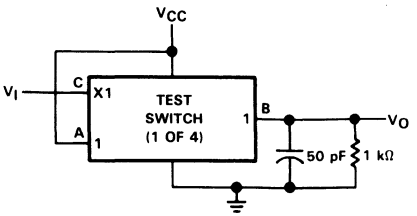
TEST CIRCUIT



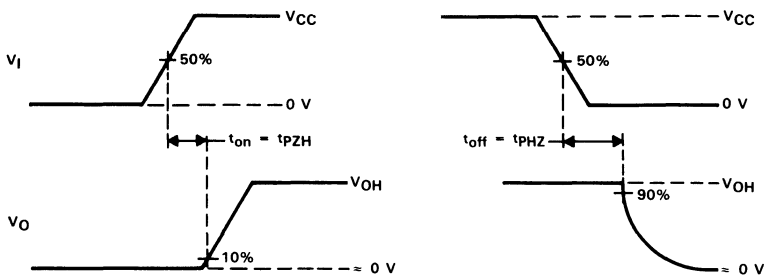
VOLTAGE WAVEFORMS

FIGURE 5. SWITCHING TIME (t_{PZL}, t_{PLZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



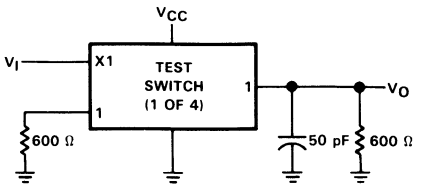
TEST CIRCUIT



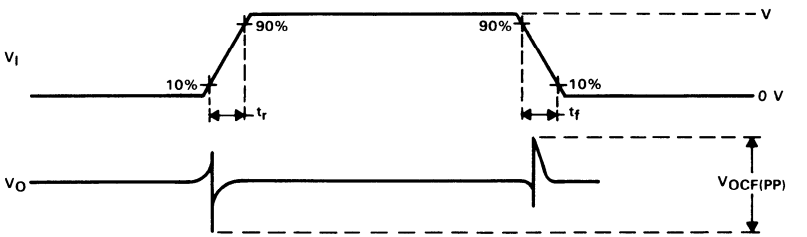
VOLTAGE WAVEFORMS

FIGURE 6. SWITCHING TIME (t_{PZH}, t_{PHZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION

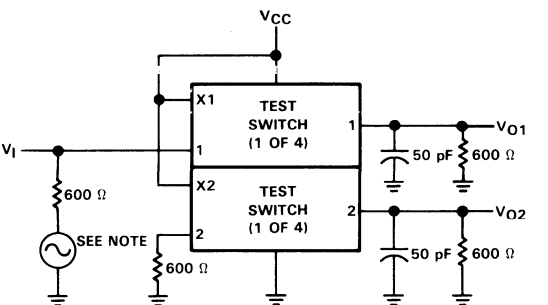


TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 7. CONTROL FEEDTHROUGH VOLTAGE



NOTE: ADJUST f for $a_X = \frac{V_{O2}}{V_{O1}} = 50$ dB.

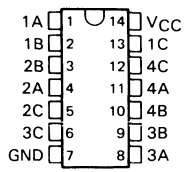
FIGURE 8. CROSSTALK BETWEEN ANY TWO SWITCHES, TEST CIRCUIT

TLC4066M, TLC4066I
SILICON-GATE CMOS QUADRUPLE BILATERAL ANALOG SWITCH

D2922, JANUARY 1986

- **High Degree of Linearity**
- **High On-Off Output Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Low On-State Impedance . . .Typically 30 Ohms at V_{CC} = 12 V**
- **Individual Switch Controls**
- **Extremely Low Input Current**
- **Functionally Interchangeable with National Semiconductor MM54/74HC4066, Motorola MC54/74HC4066, and RCA CD4066A**

TLC4066M . . . J OR N PACKAGE
TLC4066I . . . D OR N PACKAGE
(TOP VIEW)



description

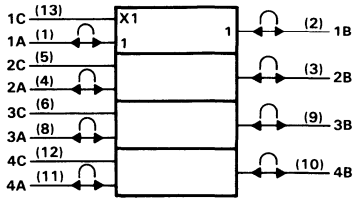
The TLC4066 is a silicon-gate CMOS quadruple analog switch integrated circuit designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 12 volts peak to be transmitted in either direction.

Each switch section has its own enable input control. A high-level voltage applied to this control terminal turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

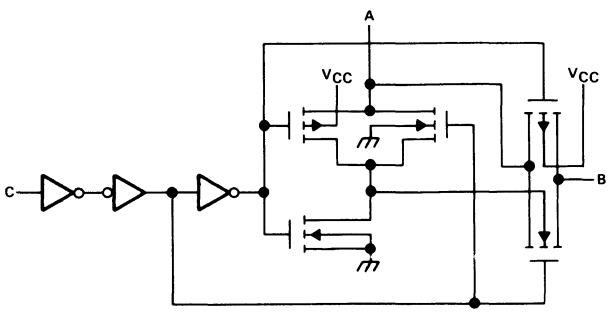
The TLC4066M is characterized for operation from −55°C to 125°C. The TLC4066I is characterized from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range (see Note 1) . . . . . −0.5 V to 15 V
Control-input diode current ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
I/O port diode current ($V_I < 0$ or $V_{I/O} > V_{CC}$) . . . . . ±20 mA
On-state switch current ($V_{I/O} = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 875 mW
Operating free-air temperature, T_A: TLC4066M . . . . . −55°C to 125°C
TLC4066I . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N packages . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. For operation above 25°C free-air temperature, see Dissipation Derating Table.

DISSIPATION DERATING TABLE

Package	Maximum Power Dissipation			Derating Factor
	25°C	85°C	125°C	
D	950 mW	494 mW		7.6 mW/°C
J	1025 mW	533 mW	205 mW	8.2 mW/°C
N	875 mW	455 mW	175 mW	7.0 mW/°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		2†	5	12	V
I/O port voltage, $V_{I/O}$		0		V_{CC}	V
High-level input voltage, V_{IH}	V_{CC} = 2 V	1.5		V_{CC}	V
	V_{CC} = 4.5 V	3.15		V_{CC}	
	V_{CC} = 9 V	6.3		V_{CC}	
	V_{CC} = 12 V	8.4		V_{CC}	
Low-level input voltage, V_{IL}	V_{CC} = 2 V	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	
	V_{CC} = 9 V	0		1.8	
	V_{CC} = 12 V	0		2.4	
Input rise time, t_r	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Input fall time, t_f	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Operating free-air temperature, T_A	TLC4066M	−55		125	°C
	TLC4066I	−40		85	

†With supply voltages at or near 2 volts, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	TLC4066M			TLC4066I			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
r_{Son}	On-state switch resistance		I_S = 1 mA, V_A = 0 to V_{CC}, See Figure 1	4.5 V		100	220		100	200	Ω
				9 V		50	110		50	105	
				12 V		30	90		30	85	
			I_S = 1 mA, V_A = 0 or V_{CC}, See Figure 1	2 V		120	240		120	215	
				4.5 V		50	120		50	100	
				9 V		35	80		35	75	
				12 V		20	70		20	60	
	On-state switch resistance matching		V_A = 0 to V_{CC}, See Figure 1	4.5 V		10	20		10	20	Ω
				9 V		5	15		5	15	
				12 V		5	15		5	15	
I_I	Control input current		V_I = 0 or V_{CC}	2 V or 6 V			±1			±1	μA
I_{Soff}	Off-state switch leakage current		V_S = ±V_{CC}, See Figure 2	5.5 V		±10	±600		±10	±600	nA
				9 V		±15	±800		±15	±800	
				12 V		±20	±1000		±20	±1000	
I_{Son}	On-state switch leakage current		V_A = 0 or V_{CC}, See Figure 3	5.5 V		±10	±150		±10	±150	nA
				9 V		±15	±200		±15	±200	
				12 V		±20	±300		±20	±300	
I_{CC}	Supply current		V_I = 0 or V_{CC}, I_O = 0	5.5 V		2	40		2	20	μA
				9 V		8	160		8	80	
				12 V		16	320		16	160	
C_i	Input capacitance	A or B		2 V to 12 V		15			15		pF
		C				5	10		5	10	
C_f	Feedthrough capacitance	A to B	V_I = 0	2 V to 12 V		5			5		pF

†All typical values are at T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TLC4066M			TLC4066I			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Propagation delay time, A to B or B to A	See Figure 4	2 V		25	75		15	30	ns
			4.5 V		5	15		5	13	
			9 V		4	12		4	10	
			12 V		3	13		3	11	
t_{on}	Switch turn-on time	R_L = 1 kΩ, See Figures 5 and 6	2 V		32	150		32	125	ns
			4.5 V		8	30		8	25	
			9 V		6	18		6	15	
			12 V		5	15		5	13	
t_{off}	Switch turn-off time	R_L = 1 kΩ, See Figures 5 and 6	2 V		45	252		45	210	ns
			4.5 V		15	54		15	45	
			9 V		10	48		10	40	
			12 V		8	45		8	38	
f_{co}	Switch cutoff frequency (channel loss = 3 dB)		4.5 V		100			100		MHz
			9 V		120			120		
$V_{OCF(PP)}$	Control feedthrough voltage to any switch, peak to peak	See Figure 7	4.5 V			180			180	mV
	Frequency at which crosstalk attenuation between any two switches equals 50 dB	See Figure 8	4.5 V		1			1		MHz

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

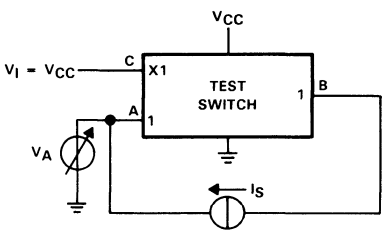
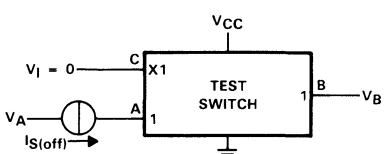


FIGURE 1. ON-STATE RESISTANCE TEST CIRCUIT



$V_S = V_A - V_B$
CONDITION 1: V_A = 0, $V_B = V_{CC}$
CONDITION 2: $V_A = V_{CC}$, V_B = 0

FIGURE 2. OFF-STATE SWITCH LEAKAGE CURRENT TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION

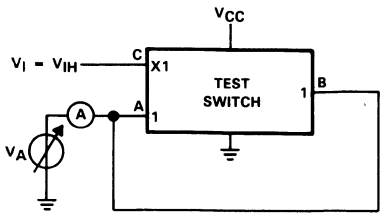
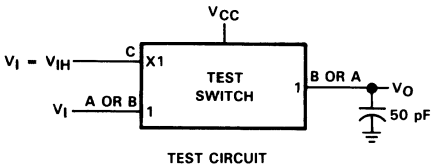
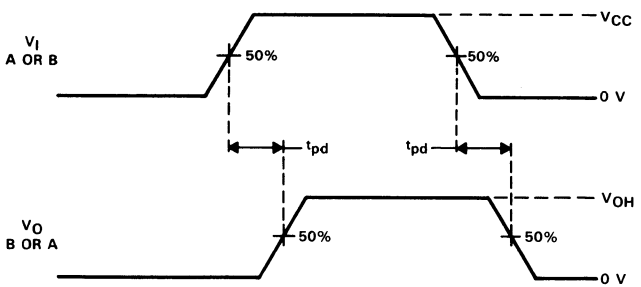


FIGURE 3. ON-STATE SWITCH LEAKAGE CURRENT TEST CIRCUIT



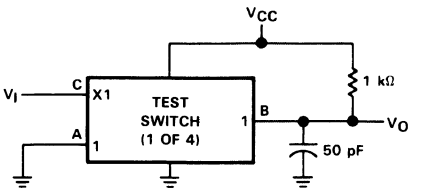
TEST CIRCUIT



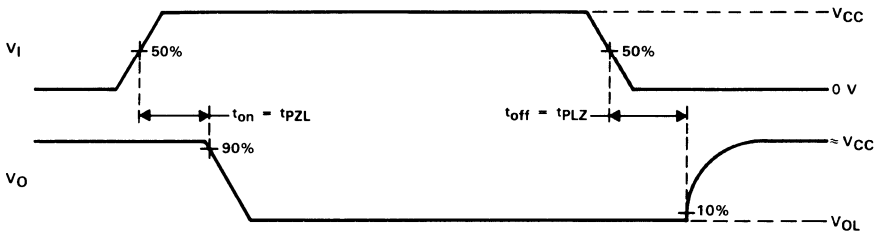
VOLTAGE WAVEFORMS

FIGURE 4. PROPAGATION DELAY TIME, SIGNAL INPUT TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



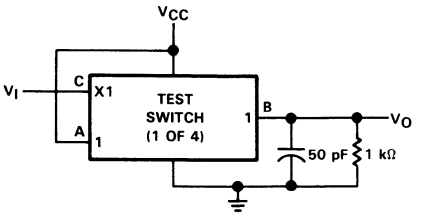
TEST CIRCUIT



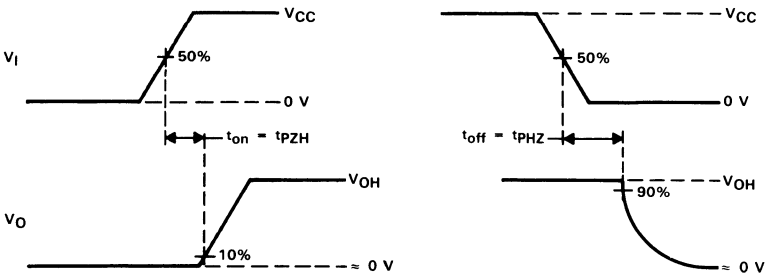
VOLTAGE WAVEFORMS

FIGURE 5. SWITCHING TIME (t_{PZL}, t_{PLZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



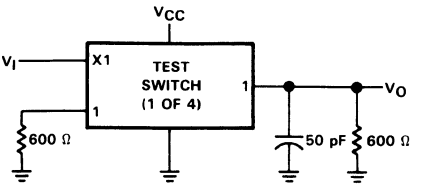
TEST CIRCUIT



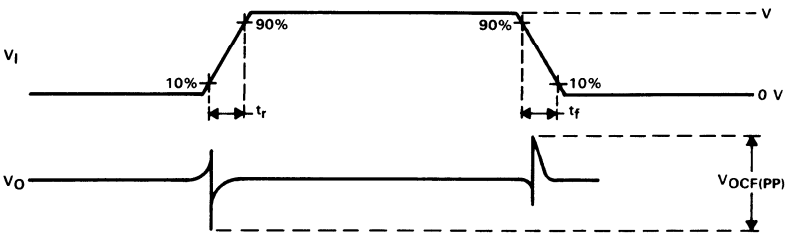
VOLTAGE WAVEFORMS

FIGURE 6. SWITCHING TIME (t_{PZH}, t_{PHZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION

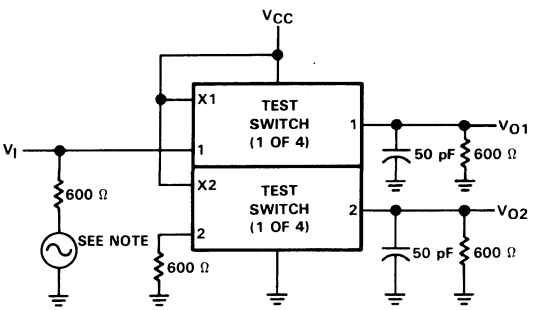


TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 7. CONTROL FEEDTHROUGH VOLTAGE



NOTE: ADJUST f for $a_X = \frac{V_{O2}}{V_{O1}} = 50$ dB.

FIGURE 8. CROSSTALK BETWEEN ANY TWO SWITCHES, TEST CIRCUIT

Data Acquisition

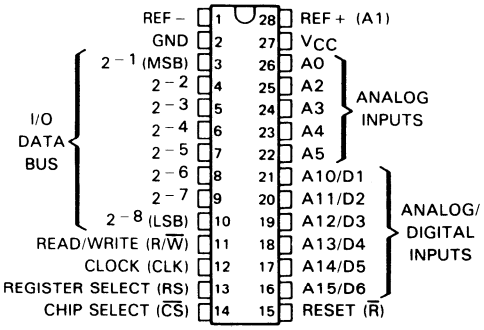
7

TLC532AM, TLC532AI, TLC533AM, TLC533AI
LinCMOS™ 8-BIT ANALOG-TO-DIGITAL PERIPHERALS WITH 5 ANALOG AND 6 DUAL-PURPOSE INPUTS

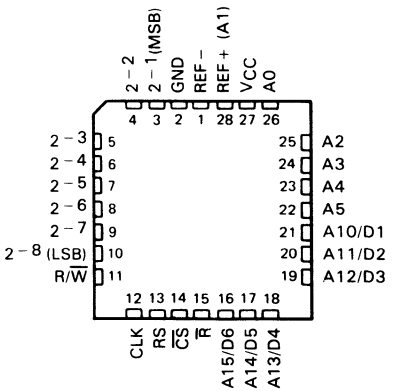
D2819, NOVEMBER 1983—REVISED SEPTEMBER 1986

- LinCMOS™ Technology
- 8-Bit Resolution
- Total Unadjusted Error . . . ±0.5 LSB Max
- Ratiometric Conversion
- Access Plus Conversion Time:
  TLC532A . . . 15 μs Max
  TLC533A . . . 30 μs Max
- 3-State, Bidirectional I/O Data Bus
- 5 Analog and 6 Dual-Purpose Inputs
- On-Chip 12-Channel Analog Multiplexer
- Three On-Chip 16-Bit Data Registers
- Software Compatible with Larger TL530 and TL531 (21-Input Versions)
- On-Chip Sample-and-Hold Circuit
- Single 5-V Supply Operation
- Low Power Consumption . . . 6.5 mW Typ
- Improved Direct Replacements for Texas Instruments TL532 and TL533, National Semiconductor ADC0829, and Motorola MC14442

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



description

The TLC532A and TLC533A are monolithic LinCMOS™ peripheral integrated circuits each designed to interface a microprocessor for analog data acquisition. These devices are complete peripheral data acquisition systems on a single chip and can convert analog signals to digital data from up to 11 external analog terminals. Each device features operation from a single 5-volt supply. Each contains a 12-channel analog multiplexer, an 8-bit ratiometric analog-to-digital (A/D) converter, a sample-and-hold, three 16-bit registers, and microprocessor-compatible control circuitry. Additional features include a built-in self-test, six multipurpose (analog or digital) inputs, five external analog inputs, and an 8-pin input/output (I/O) data port. The three on-chip data registers store the control data, the conversion results, and the input digital data that can be accesssed via the microprocessor data bus in two 8-bit bytes (most-significant byte first). In this manner, a microprocessor can access up to 11 external analog inputs or 6 digital signals and the positive reference voltage that may be used for self-test.

FUNCTION TABLE

ADDRESS/CONTROL					DESCRIPTION
R/W	RS	CS	R	CLK	
X	X	X	L†		Reset
L	H	L	H	↓	Write bus data to control register
H	L	L	H	↑	Read data from analog conversion register
H	H	L	H	↑	Read data from ditigal data register
X	X	H	H	X	No response

H = High-level, L = Low-level, X = Irrelevant
↓ = High-to-low transition, ↑ = Low-to-high transition
†For proper operation, Reset must be low for at least three clock cycles.

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description (continued)

The A/D conversion uses the successive-approximation technique and switched-capacitor circuitry. This method eliminates the possibility of missing codes, nonmonotonicity, and a need for zero or full-scale adjustment. Any one of 11 analog inputs (or self-test) can be converted to an 8-bit digital word and stored in 10 microseconds (TLC532A) or 20 microseconds (TLC533A) after instructions from the microprocessor have been recognized. The on-chip sample-and-hold functions automatically to minimize errors due to noise on the analog inputs. Furthermore, differential high-impedance reference inputs are available to help isolate the analog circuitry from the logic and supply noises while easing ratiometric conversion and scaling.

The TLC532AM and TLC533AM are available in both the N and FN plastic packages and are characterized for operation from −55 °C to 125 °C. The TLC532AI and TLC533AI are characterized for operation from −40 °C to 85 °C.

functional description

The TLC532A and TLC533A provide direct interface to a microprocessor-based system. Control of the TLC532A and TLC533A is handled via the 8-line TTL-compatible 3-state data bus, the three control inputs (Read/Write, Register Select, and Chip Select), and the Clock input. Each device contains three 16-bit internal registers. These registers are the control register, the analog conversion data register, and the digital data register.

A high level at the Read/Write input and a low level at the Chip Select input set the device to output data on the 8-line data bus for the processor to read. A low level at the Read/Write input and a low level at the Chip Select input set the device to receive instructions into the internal control register on the 8-line data bus from the processor. When the device is in the read mode and the Register Select input is low, the processor will read the data contained in the analog conversion data register. However, when the Register Select input is high, the processor reads the data contained in the digital data register.

The control register is a write-only register into which the microprocessor writes command instructions for the device to start A/D conversion and to select the analog channel to be converted. The analog conversion data register is a read-only register that contains the current converter status and most recent conversion results. The digital data register is also a read-only register that holds the digital input logic levels from the six dual-purpose inputs.

Internally each device contains a byte pointer that selects the appropriate byte during two cycles of the Clock input in a normal 16-bit microprocessor instruction. The internal pointer will automatically point to the most-significant (MS) byte after the first complete clock cycle any time that the Chip Select is at the high level for at least one clock cycle. This causes the device to treat the next signal on the 8-line data bus as the MS byte. A low level at the Chip Select input activates the inputs and outputs and an internal function decoder. However, no data is transferred until the Clock goes high. The internal byte pointer first points to the MS byte of the selected register during the first clock cycle. After the first clock cycle in which the MS byte is accessed, the internal pointer switches to the LS byte and remains there for as long as Chip Select is low. The MS byte of any register may be accessed by either an 8-bit or a 16-bit microprocessor instruction; however, the LS byte may only be accessed by a 16-bit microprocessor instruction.

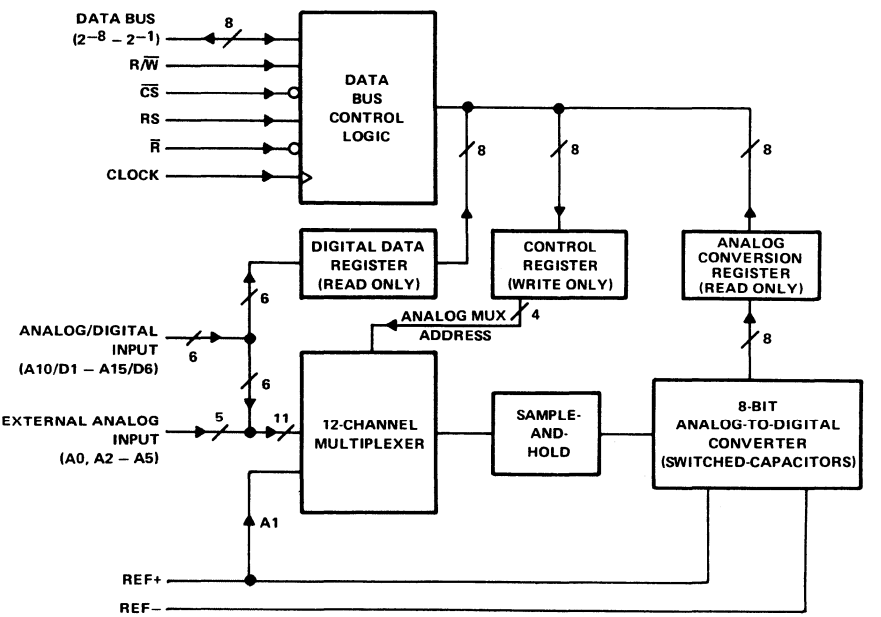
Normally, a two-byte word is written into or read from the controlling processor, but a single byte can be read by the processor by proper manipulation of the Chip Select input. This can be used to read conversion status from the analog conversion data register or the digital multipurpose input levels from the digital data register. The format and content of each two-byte word is shown in Figures 1 through 3.

functional description (continued)

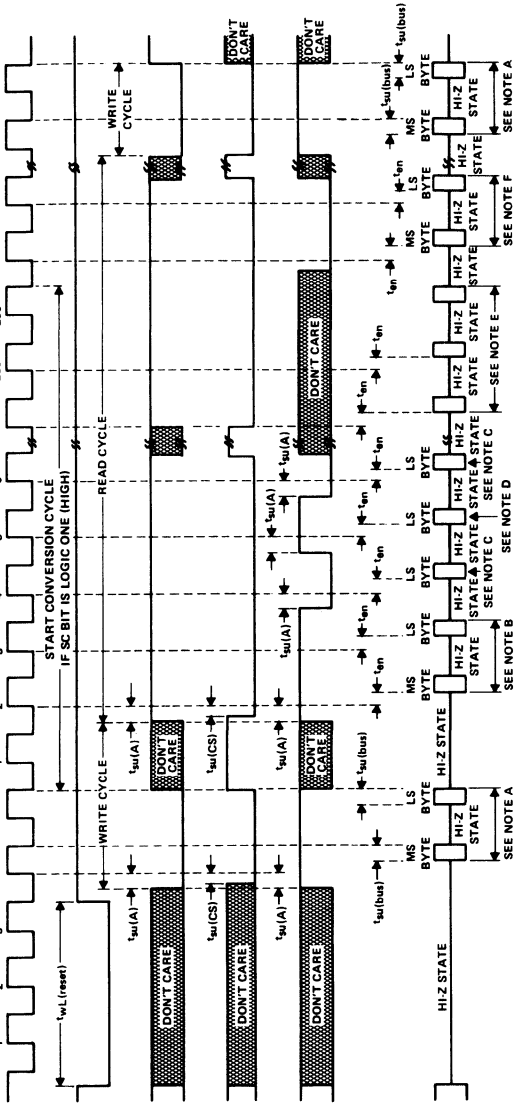
A conversion cycle is started after a two-byte instruction is written into the control register and the start conversion (SC) bit is a logic high. This two-byte instruction also selects the input analog channel to be converted. The status (EOC) bit in the analog conversion data register is reset and it remains reset until the conversion is completed, at that time the status bit is then set again. After conversion, the results are loaded into the analog conversion data register. These results remain in the analog conversion data register until the next conversion cylce is completed. If a new conversion command is entered into the control register while the conversion cycle is in progress, the on-going conversion will be aborted and a new channel acquisition cycle will immediately begin.

The Reset input allows the device to be externally forced to a known state. When a low level is applied to the Reset input for a minimum of three clock periods, the start conversion bit is cleared. The A/D converter is then idled and all the outputs are placed in the high-impedance off-state. However, the content of the analog conversion data register is not affected by the Reset input going to a low level.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.

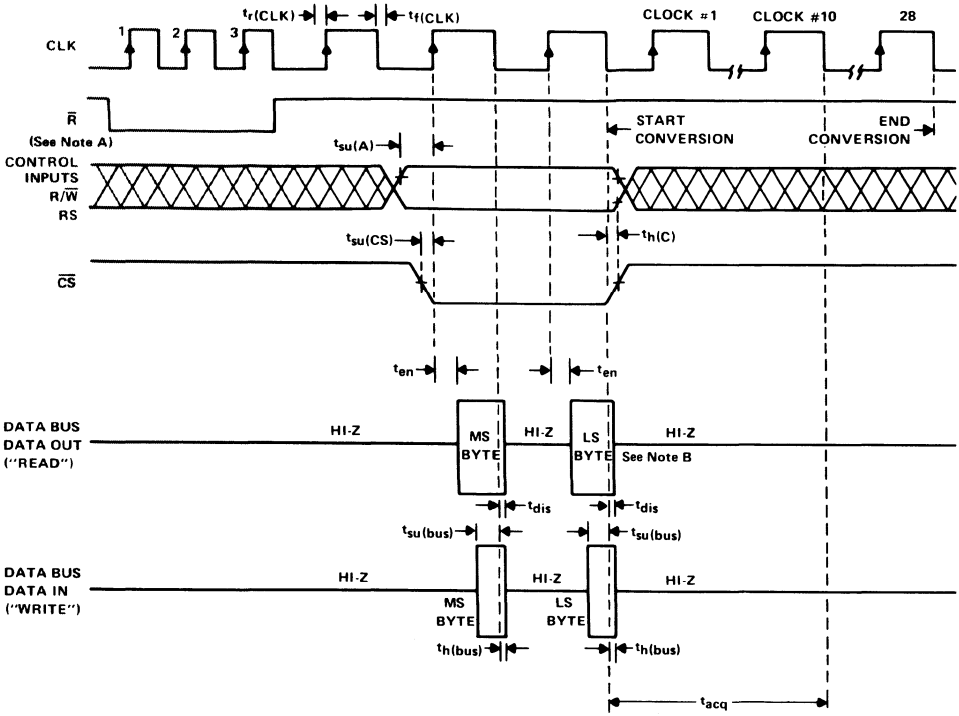


typical operating sequence



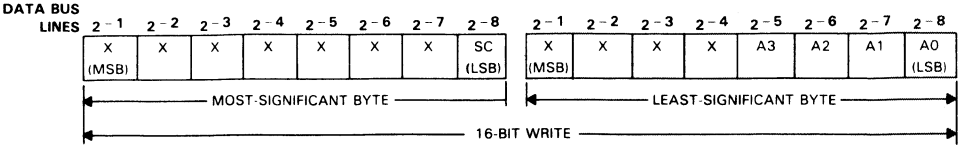
NOTES: A. This is a 16-bit input instruction from the microprocessor being sent to the control data register.
B. This is the 2-byte (16-bit) content of the digital data register being sent to the microprocessor.
C. This is the LS byte (8-bit) content of the analog conversion data register being sent to the microprocessor.
D. This is the LS byte (8-bit) content of the digital data register being sent to the microprocessor.
E. These are MS byte (8-bit), LS byte (8-bit), and LS byte (8-bit) content of the analog conversion data register or digital data register being sent to the microprocessor.
F. This is the 2-byte (16-bit) content of the analog conversion data register being sent to the microprocessor.

read or write cycle time sequence



NOTES: A. The reset pulse (R̄ low) is required only during power-up.

B. The most-significant byte output of Data Out occurs when CLK is high. When CLK is low, Data Out is in the high-impedance (off) state. When CLK goes high again, the least-significant byte is placed on the data bus. At this point, the least-significant byte will remain on the bus for as long as CLK is kept high.



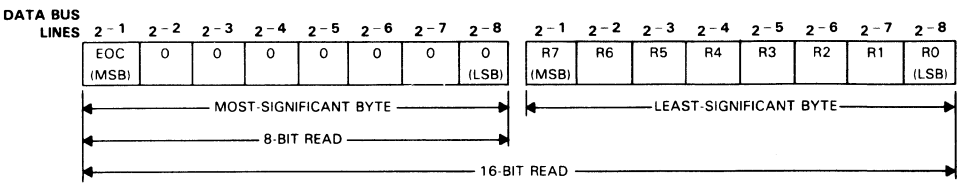
Unused Bits (X) – The MS byte bits 2^{-1} through 2^{-7} and LS byte bits 2^{-1} through 2^{-4} of the control register are not used internally.

Start Conversion (SC) – When the SC bit in the MS byte is set to a logical 1 (high level), analog-to-digital conversion of the specified analog channel will begin immediately after the completion of the control register write.

Analog Multiplex Address (A0-A3) – These four address bits are decoded by the analog multiplexer and used to select the appropriate analog channel as shown below:

Hexadecimal Address (A3 = MSB)	Channel Select
0	A0
1	REF+ (A1)
2-5	A2-A5
6-9 (not used)	
A-F	A10-A15

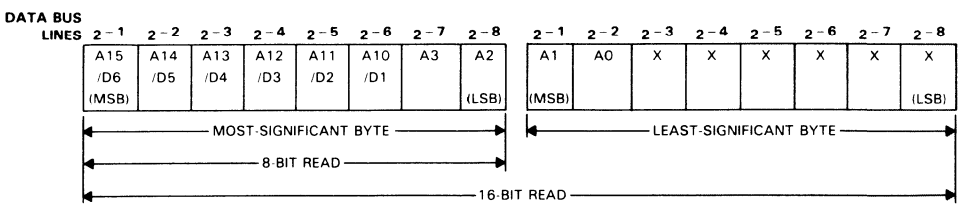
FIGURE 1. CONTROL REGISTER TWO-BYTE WRITE WORD FORMAT AND CONTENT



A/D Status (EOC) – The A/D status end-of-conversion (EOC) bit is set whenever an analog-to-digital conversion is successfully completed by the A/D converter. The status bit is cleared by a 16-bit write from the microprocessor to the control register. The remainder of the bits in the MS byte of the analog conversion data register are always reset to logical 0 to simplify microprocessor interrogation of the A/D converter status.

A/D Result (R0-R7) – The LS byte of the analog conversion data register contains the result of the analog-to-digital conversion. Result bit R7 is the MSB and the converter follows the standard convention of assigning a code of all ones (11111111) to a full-scale analog voltage. There are no special overflow or underflow indications.

FIGURE 2. ANALOG CONVERSION DATA REGISTER ONE-BYTE AND TWO-BYTE READ WORD FORMAT AND CONTENT



Shared Digital Port (A10/D1-A15/D6) – The voltage present on these pins is interpreted as a digital signal and the corresponding states are read from these bits. A digital value will be given for each pin even if some or all of these pins are being used as analog inputs.

Analog Multiplexer Address (A0-A3) – The address of the selected analog channel presently addressed is given by these bits.

Unused Bits (X) – LS byte bits 2^{-3} through 2^{-8} of the digital data register are not used.

FIGURE 3. DIGITAL DATA REGISTER ONE-BYTE AND TWO-BYTE READ WORD FORMAT AND CONTENT

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 V to 6.5 V
Input voltage range: Positive reference voltage . . . . . V_{REF-} to V_{CC} + 0.3 V
Negative reference voltage . . . . . −0.3 V to V_{REF+}
All other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Input current, I_I (any input) . . . . . ±10 mA
Total input current, (all inputs) . . . . . ±20 mA
Operating free-air temperature range: TLC532AM, TLC533AM . . . . . −55°C to 125°C
TLC532AI, TLC533AI . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C
Case temperature for 10 seconds: FN package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

		TLC532A			TLC533A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)		2.5	V_{CC}	$V_{CC}+0.1$	2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 2)		−0.1	0	2.5	−0.1	0	2.5	V
Differential reference voltage, $V_{REF+} - V_{REF-}$		1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
High-level input voltage, V_{IH}	Clock input	$V_{CC}-0.8$			$V_{CC}-0.8$			V
	All other digital inputs	2			2			
Low-level input voltage, V_{IL}	Any digital input			0.8			0.8	V
Clock frequency, f_{CLK}		0.1	2	2.048	0.1	1.048	1.06	MHz
CS setup time, $t_{su(CS)}$		75			100			ns
Address (R/W and RS) setup time, $t_{su(A)}$		100			145			ns
Data bus input setup time, $t_{su(bus)}$		140			185			ns
Control (R/W, RS, and CS) hold time, $t_{h(C)}$		10			20			ns
Data bus input hold time, $t_{h(bus)}$		15			20			ns
Pulse duration of control during read, $t_{w(C)}$		305			575			ns
Pulse duration, reset low, $t_{wL(reset)}$		3			3			Clock Cycles
Pulse duration of clock high, $t_{wH(CLK)}$		230			440			ns
Pulse duration of clock low, $t_{wL(CLK)}$		200			410			ns
Clock rise time, $t_{r(CLK)}$				15			25	ns
Clock fall time, $t_{f(CLK)}$				16			30	ns
Operating free-air temperature, T_A	TLC__AM	−55		125	−55		125	°C
	TLC__AI	−40		85	−40		85	

NOTE 2: Analog input voltages greater than or equal to that applied to the REF+ terminal convert to all ones (11111111), while input voltages equal to or less than that applied to the REF− terminal convert to all zeros (00000000). For proper operation, the positive reference voltage, V_{REF+}, must be at least 1-volt greater than the negative reference voltage, V_{REF-}. In addition, unadjusted errors may increase as the differential reference voltage, $V_{REF+} - V_{REF-}$, falls below 4.75 volts.

electrical characteristics over recommended operating free-air temperature range, V_{REF+} = V_{CC}, V_{REF-} at ground, f_{CLK} = 2 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −1.6 mA	2.4			V
V_{OL}	low-level output voltage		I_{OL} = 1.6 mA			0.4	V
I_{IH}	High-level input current	Any digital or Clock input	V_{IH} = 5.5 V			10	μA
		Any control input				1	
I_{IL}	Low-level input current	Any digital or Clock input	V_{IL} = 0			−10	μA
		Any control input				−1	
I_{OZ}	Off-state (high impedance-state) output current		$V_O = V_{CC}$			10	μA
			V_O = 0			−10	
I_I	Analog input current (see Note 3)		V_I = 0 to V_{CC}			±500	nA
	Leakage current between selected channel and all other analog channels		V_I = 0 to V_{CC}, Clock input at 0 V			±400	nA
C_i	Input capacitance	Digital pins 3 thru 10			4	30	pF
		Any other input pin			2	15	
$I_{CC} + I_{REF+}$	Supply current plus reference current		V_{CC} = V_{REF+} = 5.5 V, Outputs open		1.5	3	mA
I_{CC}	Supply current		V_{CC} = 5.5 V		1.4	2	mA

NOTE 3: Analog input current is an average of the current flowing into a selected analog channel input during one full conversion cycle.

operating characteristics over recommended operating free-air temperature range, V_{REF+} = V_{CC}, V_{REF-} at ground, f_{CLK} = 2 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Linearity error		See Note 4			±0.5	LSB
	Zero error		See Note 5			±0.5	LSB
	Full-scale error		See Note 5			±0.5	LSB
	Total unadjusted error		See Note 6			±0.5	LSB
	Absolute accuracy error		See Note 7			±1	LSB
t_{conv}	Conversion time (including channel acquisition time)				30		Clock Cycles
t_{acq}	Channel acquisition time prior to starting conversion				10		Clock Cycles
t_{en}	Data output enable time (see Note 8)		C_L = 50 pF, R_L = 3 kΩ,			250	ns
t_{dis}	Data output disable time		C_L = 50 pF, R_L = 3 kΩ	10			ns
$t_{r(bus)}$	Data bus output rise time	High-impedance to high-level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		Low to high-level				300	
$t_{f(bus)}$	Data bus output fall time	High-impedance to low-level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		High to low-level				300	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 4. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
5. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
6. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
7. Absolute accuracy error is the maximum difference between an analog value and the nominal midstep value within any step. This includes all errors including inherent quantization error, which is the ±0.5 LSB uncertainty caused by the A/D converters finite resolution.
8. If chip-select setup time, $t_{su(CS)}$, is less than 0.14 microseconds, the effective data output enable time, t_{en}, may extend such that $t_{su(CS)} + t_{en}$ is equal to a maximum of 0.475 microseconds.

electrical characteristics over recommended ranges V_{CC}, V_{REF+}, and operating free-air temperature, V_{REF-} at ground, f_{CLK} = 1.048 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −1.6 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 1.6 mA			0.4	V
I_{IH}	High-level input current	Any digital or Clock input	V_{IH} = 5.5 V			10	μA
		Any control input				1	
I_{IL}	Low-level input current	Any digital or Clock input	V_{IL} = 0			−10	μA
		Any control input				−1	
I_{OZ}	Off-state (high impedance-state) output current		$V_O = V_{CC}$			10	μA
			V_O = 0			−10	
I_I	Analog input current (see Note 3)		V_I = 0 to V_{CC}			±500	nA
	Leakage current between selected channel and all other analog channels		V_I = 0 to V_{CC}, Clock input at 0 V			±400	nA
C_i	Input capacitance	Digital pins 3 thru 10			4	30	pF
		Any other input pin			2	15	
$I_{CC} + I_{REF+}$	Supply current plus reference current		$V_{CC} = V_{REF+}$ = 5.5 V, Outputs open		1.3	3	mA
I_{CC}	Supply current		V_{CC} = 5.5 V		1.2	2	mA

NOTE 3: Analog input current is an average of the current flowing into a selected analog channel input during one full conversion cycle.

operating characteristics over recommended ranges V_{CC}, V_{REF+}, and operating free-air temperature, V_{REF-} at ground, f_{clock} = 1.048 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Linearity error		See Note 4			±0.5	LSB
	Zero error		See Note 5			±0.5	LSB
	Full-scale error		See Note 5			±0.5	LSB
	Total unadjusted error		See Note 6			±0.5	LSB
	Absolute accuracy error		See Note 7			±1	LSB
t_{conv}	Conversion time (including channel acquisition time)				30		Clock Cycles
t_{acq}	Channel acquisition time prior to starting conversion				10		Clock Cycles
t_{en}	Data output enable time (see Note 8)		C_L = 50 pF, R_L = 3 kΩ,			335	ns
t_{dis}	Data output disable time		C_L = 50 pF, R_L = 3 kΩ	10			ns
$t_{r(bus)}$	Data bus output rise time	High-impedance to high-level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		Low to high-level				300	
$t_{f(bus)}$	Data bus output fall time	High-impedance to low-level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		High to low-level				300	

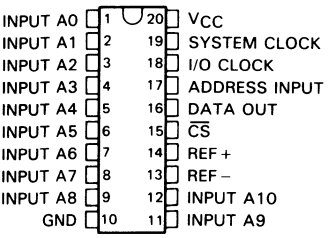
†Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 4. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
5. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
6. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
7. Absolute accuracy error is the maximum difference between an analog value and the nominal midstep value within any step. This includes all errors including inherent quantization error, which is the ±0.5 LSB uncertainty caused by the A/D converters finite resolution.
8. If chip-select setup time, $t_{su(CS)}$, is less than 0.14 microseconds, the effective data output enable time, t_{en}, may extend such that $t_{su(CS)} + t_{en}$ is equal to a maximum of 0.475 microseconds.

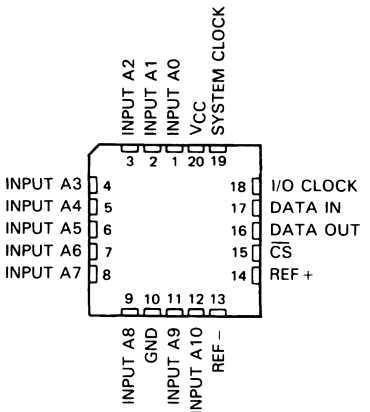
- **LinCMOS™ Technology**
- **8-Bit Resolution A/D Converter**
- **Microprocessor Peripheral or Stand-Alone Operation**
- **On-Chip 12-Channel Analog Multiplexer**
- **Built-In Self-Test Mode**
- **Software-Controllable Sample and Hold**
- **Total Unadjusted Error . . . ±0.5 LSB Max**
- **TLC541 is Direct Replacement for Motorola MC145040 and National Semiconductor ADC0811. TLC540 is Capable of Higher Speed**
- **Pinout and Control Signals Compatible with TLC1540 Family of 10-Bit A/D Converters**

TYPICAL PERFORMANCE	TLC540	TLC541
Channel Acquisition Sample Time	2 μs	3.6 μs
Conversion Time	9 μs	17 μs
Samples per Second	75 × 10^3	40 × 10^3
Power Dissipation	6 mW	6 mW

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



description

The TLC540 and TLC541 are LinCMOS™ A/D peripherals built around an 8-bit switched-capacitor successive-approximation A/D converter. They are designed for serial interface to a microprocessor or peripheral via a three-state output with up to four control inputs [including independent System Clock, I/O Clock, Chip Select ($\overline{CS}$), and Address Input]. A 4-megahertz system clock for the TLC540 and a 2.1-megahertz system clock for the TLC541 with a design that includes simultaneous read/write operation allow high-speed data transfers and sample rates of up to 75,180 samples per second for the TLC540 and 40,000 samples per second for the TLC541. In addition to the high-speed converter and versatile control logic, there is an on-chip 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal "self-test" voltage, and a sample-and-hold that can operate automatically or under microprocessor control. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The converters incorporated in the TLC540 and TLC541 feature dproofifferential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A switched-capacitor design allows guaranteed low-error (±0.5 LSB) conversion in 9 microseconds for the TLC540 and 17 microseconds for the TLC541 over the full operating temperature range.

The TLC540 and the TLC541 are available in both the N and FN plastic packages. The M-suffix versions are characterized for operation from −55°C to 125°C. The I-suffix versions are characterized for operation from −40°C to 85°C.

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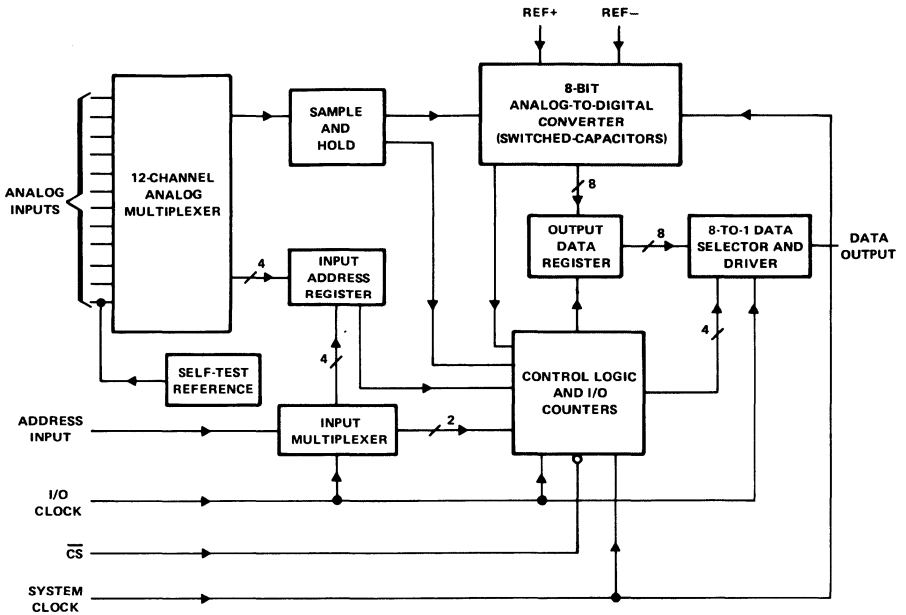
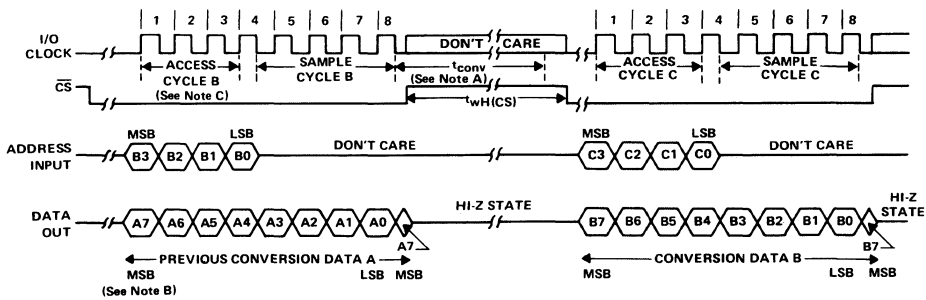
functional block diagram



operating sequence



NOTES: A. The conversion cycle, which requires 36 System Clock periods, is initiated on the 8th falling edge of the I/O Clock after $\overline{CS}$ goes low for the channel whose address exists in memory at that time. If $\overline{CS}$ is kept low during conversion, the I/O Clock must remain low for at least 36 System Clock cycles to allow conversion to be completed.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6-A0) will be clocked out on the first seven I/O Clock falling edges.

C. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three System Clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range (any input) . . . . . −0.3 V to V_{CC} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} + 0.3 V
Peak input current range (any input) . . . . . ±10 mA
Peak total input current (all inputs) . . . . . ±30 mA
Operating free-air temperature range: TLC540I, TLC541I . . . . . −40°C to 85°C
TLC540M, TLC541M . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to digital ground with REF− and GND wired together (unless otherwise noted).

recommended operating conditions

			TLC540			TLC541			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)			2.5	V_{CC}	$V_{CC}+0.1$	2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 2)			−0.1	0	2.5	0.1	0	2.5	V
Differential reference voltage, $V_{REF+} - V_{REF-}$ (see Note 2)			1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}			2			2			V
Low-level control input voltage, V_{IL}					0.8			0.8	V
Setup time, address bits at data input before I/O CLK↑, $t_{su(A)}$			200			400			ns
Hold time, address bits after I/O CLK↑, $t_{h(A)}$			0			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			3			3			System clock cycles
$\overline{CS}$ high during conversion, $t_{wH(CS)}$			36			36			System clock cycles
Input/Output clock frequency, $f_{CLK(I/O)}$			0		2.048	0		1.1	MHz
System clock frequency, $f_{CLK(SYS)}$			$f_{CLK(I/O)}$		4	$f_{CLK(I/O)}$		2.1	MHz
System clock high, $t_{wH(SYS)}$			110			210			ns
System clock low, $t_{wL(SYS)}$			100			190			ns
Input/Output clock high, $t_{wH(I/O)}$			200			404			ns
Input/Output clock low, $t_{wL(I/O)}$			200			404			ns
Clock transition time (see Note 4)	System	$f_{CLK(SYS)} \le 1048$ kHz			30			30	ns
		$f_{CLK(SYS)} > 1048$ kHz			20			20	
	I/O	$f_{CLK(I/O)} \le 525$ kHz			100			100	ns
		$f_{CLK(I/O)} > 525$ kHz			40			40	
Operating free-air temperature, T_A		TLC540M, TLC541M	−55		125	−55		125	°C
		TLC540I, TLC541I	−40		85	−40		85	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all "1"s (11111111), while input voltages less than that applied to REF− convert as all "0"s (00000000). For proper operation, REF+ voltage must be at least 1 volt higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 volts.

3. To minimize errors caused by noise at the chip select input, the internal circuitry waits for three System Clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in an address until the minimum chip select setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 microseconds for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 2.048 MHz for TLC540 or $f_{CLK(I/O)}$ = 1.1 MHz for TLC541

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 16)		V_{CC} = 4.75 V, I_{OH} = 360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, I_{OL} = 1.6 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC}, $\overline{CS}$ at V_{CC}			10	μA
			V_O = 0, $\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		V_I = V_{CC}		0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0		−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V		1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V		0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}		−0.4	−1	
I_{CC} + I_{REF}	Supply and reference current		V_{REF+} = V_{CC}, $\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs			7	55	pF
		Control inputs			5	15	

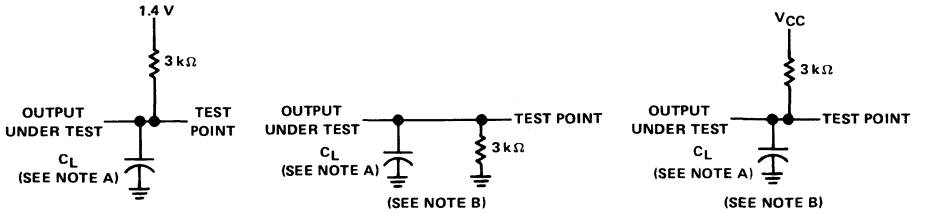
†All typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{REF+} = 4.75$ V to 5.5 V, $f_{CLK(I/O)} = 2.048$ MHz for TLC540 or 1.1 MHz for TLC541, $f_{CLK(SYS)} = 4$ MHz for TLC540 or 2.1 MHz for TLC541.

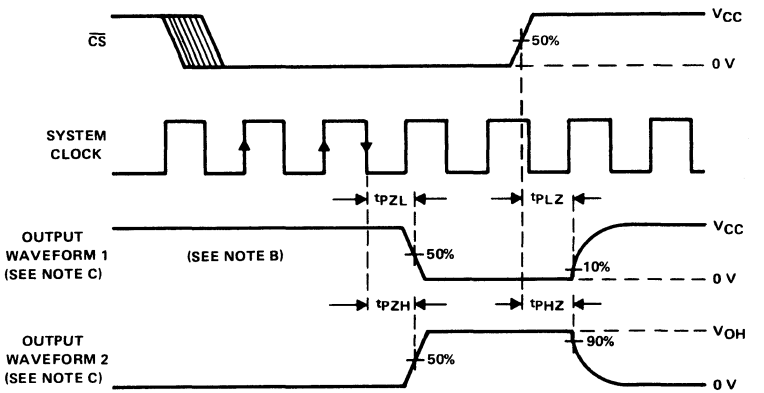
	PARAMETER	TEST CONDITIONS	TLC540			TLC541			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Linearity error	See Note 5			±0.5			±0.5	LSB
	Zero error	See Notes 2 and 6			±0.5			±0.5	LSB
	Full-scale error	See Notes 2 and 6			±0.5			±0.5	LSB
	Total unadjusted error	See Note 7			±0.5			±0.5	LSB
	Self-test output code	Input A11 address = 1011 (See Note 8)	01111101 (125)		10000011 (131)	01111101 (125)		10000011 (131)	
t_{conv}	Conversion time	See Operating Sequence			9			17	μs
	Total access and conversion time	See Operating Sequence			13.3			25	μs
t_{acq}	Channel acquisition time (sample cycle)	See Operating Sequence			4			4	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓		10			10			ns
t_d	Delay time, I/O clock↓ to data output valid	See Parameter Measurement Information			300			400	ns
t_{en}	Output enable time				150			150	ns
t_{dis}	Output disable time				150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

NOTES: 2. Analog input voltages greater than that applied to REF+ convert to all "1"s (11111111), while input voltages less than that applied to REF− convert to all"0"s (00000000). For proper operation, REF+ voltage must be at least 1 volt higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 volts.
5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The A11 analog input signal is internally generated and is used for test purposes.

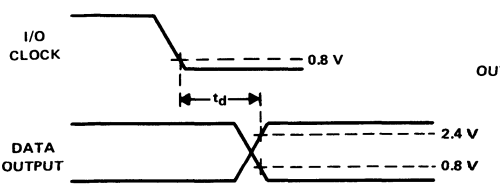
PARAMETER MEASUREMENT INFORMATION



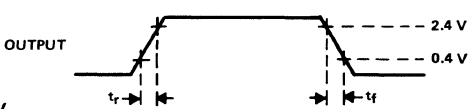
LOAD CIRCUIT FOR t_d, t_r, AND t_f | LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ} | LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME



VOLTAGE WAVEFORM FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC540 and 100 pF for TLC541.
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

principles of operation

The TLC540 and TLC541 are each complete data acquisition systems on a single chip. They include such functions as analog multiplexer, sample-and-hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs [two clocks, chip select ($\overline{CS}$), and address]. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. With judicious interface timing, with TLC540 a conversion can be completed in 9 microseconds, while complete input-conversion-output cycles can be repeated every 13 microseconds. With TLC541 a conversion can be completed in 17 microseconds, while complete input-conversion-output cycles are repeated every 25 microseconds. Furthermore, this fast conversion can be executed on any of 11 inputs or its built-in "self-test," and in any order desired by the controlling processor.

The System and I/O Clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the System Clock input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O Clock. The System Clock will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the Data Output pin is in a three-state condition and the Address Input and I/O Clock pins are disabled. This feature allows each of these pins, with the exception of the $\overline{CS}$ pin, to share a control logic point with their counterpart pins on additional A/D devices when additional TLC540/541 devices are used. In this way, the above feature serves to minimize the required control logic pins when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the System Clock after a low $\overline{CS}$ transition, before the low transition is recognized. This technique is used to protect the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result will automatically appear on the Data Out pin.
2. A new positive-logic multiplexer address is shifted in on the first four rising edges of the I/O Clock. The MSB of the address is shifted in first. The negative edges of these four I/O clock pulses shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample-and-hold begins sampling the newly addressed analog input after the fourth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three clock cycles are then applied to the I/O pin and the sixth, seventh, and eighth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final eighth clock cycle is applied to the I/O Clock pin. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 36 System Clock cycles. After this final I/O Clock cycle, $\overline{CS}$ must go high or the I/O Clock must remain low for at least 36 System Clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. Also, if $\overline{CS}$ is taken high it must remain high until the end of the conversion. Otherwise, a valid falling edge of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 System Clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

principles of operation (continued)

It is possible to connect the System and I/O Clock pins together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. When $\overline{CS}$ is recognized by the device to be at a low level, the common clock signal is used as an I/O Clock. When $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used to drive the "conversion crunching" circuitry.
2. The device will recognize a $\overline{CS}$ low transition only when the $\overline{CS}$ input changes and subsequently the System Clock pin receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles will not shift in the address because a low $\overline{CS}$ must be recognized before the I/O Clock can shift in an analog channel address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the sixth I/O Clock pulse that has been recognized by the device, so that a $\overline{CS}$ low level will be recognized upon the lowering of the eighth I/O Clock signal that is recognized by the device. Otherwise, additional common clock cycles will be recognized as I/O Clock pulses and will shift in an erroneous address.

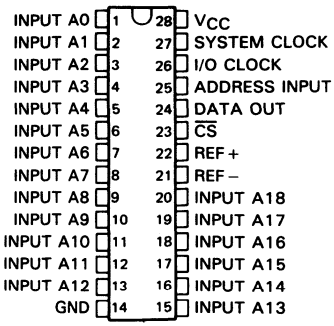
For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample-and-hold begins sampling upon the negative edge of the fourth I/O Clock cycle, the hold function is not initiated until the negative edge of the eighth I/O Clock cycle. Thus, the control circuitry can leave the I/O Clock signal in its high state during the eighth I/O Clock cycle until the moment at which the analog signal must be converted. The TLC540/TLC541 will continue sampling the analog input until the eighth falling edge of the I/O Clock. The control circuitry or software will then immediately lower the I/O Clock signal and hold the analog signal at the desired point in time and start conversion.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.

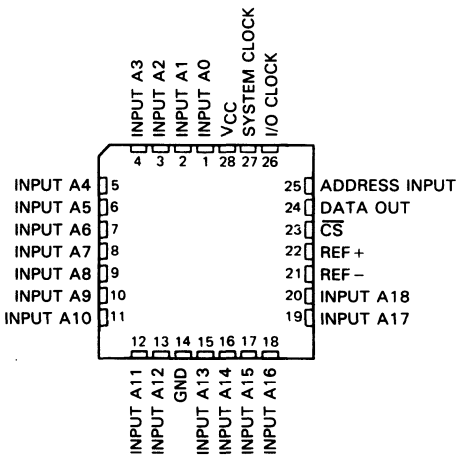
- LinCMOS™ Technology
- 8-Bit Resolution A/D Converter
- Microprocessor Peripheral or Stand-Alone Operation
- On-Chip 20-Channel Analog Multiplexer
- Built-In Self-Test Mode
- Software-Controllable Sample and Hold
- Total Unadjusted Error . . . ±0.5 LSB Max
- Timing and Control Signals Compatible with 8-Bit TLC540 and 10-Bit TLC1540 A/D Converter Families

TYPICAL PERFORMANCE	TL545	TL546
Channel Acquisition Time	1.5 μs	2.7 μs
Conversion Time	9 μs	17 μs
Sampling Rate	76 × 10^3	40 × 10^3
Power Dissipation	6 mW	6 mW

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



description

The TLC545 and TLC546 are LinCMOS™ A/D peripherals built around an 8-bit switched-capacitor successive-approximation A/D converter. They are designed for serial interface to a microprocessor or peripheral via a 3-state output with up to four control inputs [including independent System Clock, I/O Clock, Chip Select ($\overline{CS}$), and Address Input]. A 4-MHz system clock for the TLC545 and a 2.1-MHz system clock for the TLC546 with a design that includes simultaneous read/write operation allowing high-speed data transfers and sample rates of up to 76,923 samples per second for the TLC545, and 40,000 samples per second for the TLC546. In addition to the high-speed converter and versatile control logic, there is an on-chip 20-channel analog multiplexer that can be used to sample any one of 19 inputs or an internal "self-test" voltage, and a sample-and-hold that can operate automatically or under microprocessor control.

The converters incorporated in the TLC545 and TLC546 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched-capacitor design allows low-error (±0.5 LSB)

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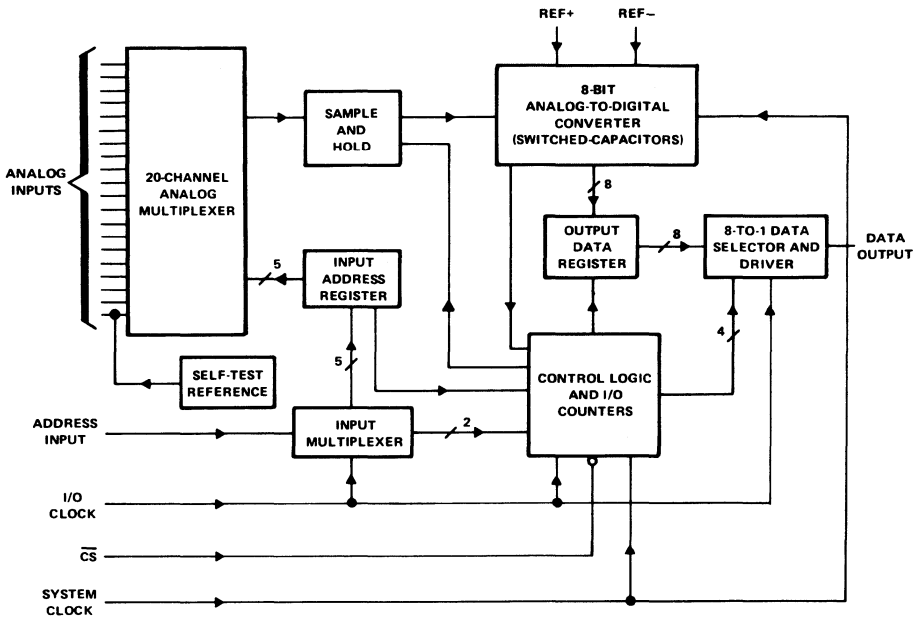
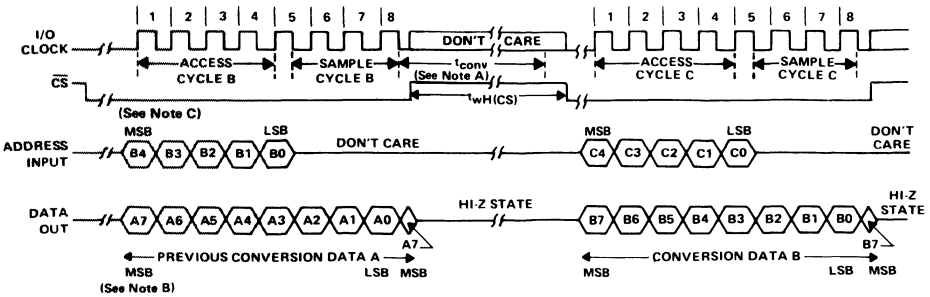
conversion in 9 μs for the TLC545, and 17 μs for the TLC546, over the full operating temperature range. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The TLC545M and the TLC546M are characterized for operation from −55°C to 125°C. The TLC545I and the TLC546I are characterized for operation from −40°C to 85°C. The TLC545C and the TLC546C are characterized for operation from 0°C to 70°C.

functional block diagram



operating sequence



NOTES: A. The conversion cycle, which requires 36 system clock periods, is initiated with the 8th I/O clock↓ after CS↓ for the channel whose address exists in memory at that time.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6-A0) will be clocked out on the first seven I/O clock falling edges.

C. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three system clock cycles (or less) after a chip select transition before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range (any input) . . . . . −0.3 V to V_{CC} +0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} +0.3 V
Peak input current range (any input) . . . . . ±10 mA
Peak total input current (all inputs) . . . . . ±30 mA
Operating free-air temperature range: TLC545M, TLC546M . . . . . −55°C to 125°C
TLC545I, TLC546I . . . . . −40°C to 85°C
TLC545C, TLC546C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

			TLC545			TLC546			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 3)			0	V_{CC}	$V_{CC}+0.1$	0	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{ref-} (see Note 2)			−0.1	0	V_{CC}	−0.1	0	V_{CC}	V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)			0	V_{CC}	$V_{CC}+0.2$	0	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}			2			2			V
Low-level control input voltage, V_{IL}					0.8			0.8	V
Setup time, address bits at data input before I/O CLK↑, $t_{su(A)}$			200			400			ns
Address hold time, t_h			0			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			3			3			System clock cycles
Chip select high during conversion, $t_{wH(CS)}$			36			36			System clock cycles
Input/Output clock frequency, $f_{CLK(I/O)}$			0		2.048	0		1.1	MHz
System clock frequency, $f_{CLK(SYS)}$			$f_{CLK(I/O)}$		4	$f_{CLK(I/O)}$		2.1	MHz
System clock high, $t_{wH(SYS)}$			110			210			ns
System clock low, $t_{wL(SYS)}$			100			190			ns
Input/Output clock high, $t_{wH(I/O)}$			200			404			ns
Input/Output clock low, $t_{wL(I/O)}$			200			404			ns
Clock transition time (see Note 4)	System	$f_{CLK(SYS)} \le 1048$ kHz			30			30	ns
		$f_{CLK(SYS)} > 1048$ kHz			20			20	
	I/O	$f_{CLK(I/O)} \le 525$ kHz			100			100	ns
		$f_{CLK(I/O)} > 525$ kHz			40			40	
Operating free-air temperature, T_A		TLC545M, TLC546M	−55		125	−55		125	°C
		TLC545I, TLC546I	−40		85	−40		85	
		TLC545C, TLC546C	0		70	0		70	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all "1"s (11111111), while input voltages less than that applied to REF− convert as all "0"s (00000000). As the differential reference voltage decreases below 4.75 V, the total unadjusted error tends to increase.

3. To minimize errors caused by noise at the Chip Select input, the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge or rising edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip select setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, V_{CC} = V_{ref+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 2.048 MHz for TLC545 or $f_{CLK(I/O)}$ = 1.1 MHz for TLC546

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 24)		V_{CC} = 4.75 V,	I_{OH} = −360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC},	$\overline{CS}$ at V_{CC}			10	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		V_I = V_{CC}			0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0			−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V			0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}			−0.4	−1	
I_{CC} + I_{ref}	Supply and reference current		V_{ref+} = V_{CC},	$\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

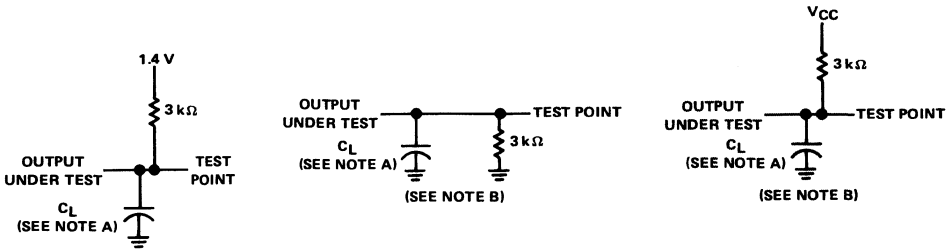
†All typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, V_{CC} = V_{ref+} = 4.75 V to 5.5 V, $f_{CLK(I/O)}$ = 2.048 MHz for TLC545 or 1.1 MHz for TLC546, $f_{CLK(SYS)}$ = 4 MHz for TLC545 or 2.1 MHz for TLC546

	PARAMETER	TEST CONDITIONS	TLC545			TLC546			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Linearity error	See Note 5			±0.5			±0.5	LSB
	Zero error	See Note 6			±0.5			±0.5	LSB
	Full-scale error	See Note 6			±0.5			±0.5	LSB
	Total unadjusted error	See Note 7			±0.5			±0.5	LSB
	Self-test output code	Input A19 address = 10011 (See Note 8)	01111101 (125)		10000011 (131)	01111101 (125)		10000011 (131)	
t_{conv}	Conversion time	See Operating Sequence			9			17	μs
	Total access and conversion time	See Operating Sequence			13			25	μs
t_{acq}	Channel acquisition time (sample cycle)	See Operating Sequence			3			3	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓		10			10			ns
t_d	Delay time, I/O clock↓ to data output valid	See Parameter Measurement Information			300			400	ns
t_{en}	Output enable time				150			150	ns
t_{dis}	Output disable time				150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

NOTES: 5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero Error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The A19 analog input signal is internally generated and is used for test purposes.

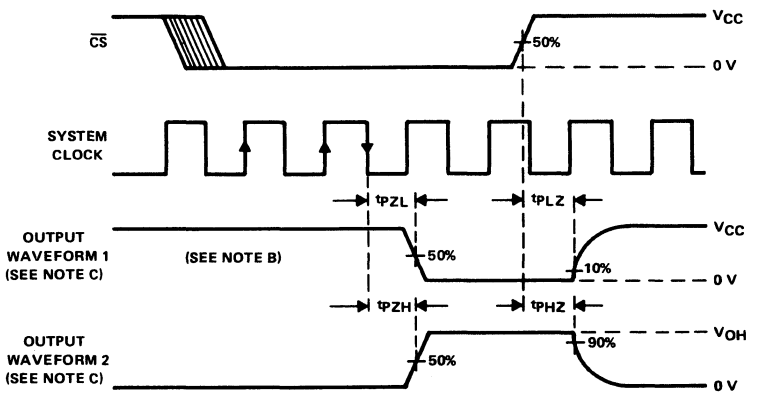
PARAMETER MEASUREMENT INFORMATION



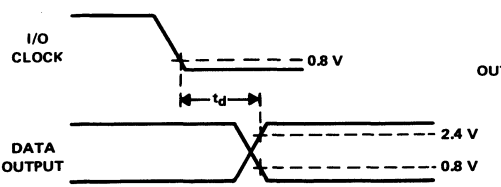
LOAD CIRCUIT FOR t_d, t_r, AND t_f

LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}

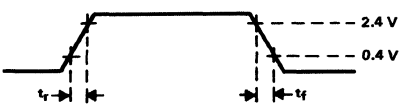
LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME



VOLTAGE WAVEFORM FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC545 and 100 pF for TLC546
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

principles of operation

The TLC545 and TLC546 are both complete data acquisition systems on single chips. Each includes such functions as system clock, sample-and-hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs; Chip Select ($\overline{CS}$), Address Input, I/O clock, and System clock. These control inputs and a TTL-compatible 3-state output facilitate serial communications with a microprocessor or microcomputer. The TLC545 and TLC546 can complete conversions in a maximum of 9 and 17 μs respectively, while complete input-conversion-output cycles can be repeated at a maximum of 13 and 25 μs, respectively.

The System and I/O clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the System clock input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O clock. The System clock will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the Data Output pin is in a high-impedance condition, and the Address Input and I/O Clock pins are disabled. This feature allows each of these pins, with the exception of the $\overline{CS}$, to share a control logic point with their counterpart pins on additional A/D devices when additional TLC545/TLC546 devices are used. Thus, the above feature serves to minimize the required control logic pins when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the System clock after a $\overline{CS}$ transition before the transition is recognized. The MSB of the previous conversion result will automatically appear on the Data Out pin.
2. A new positive-logic multiplexer address is shifted in on the first five rising edges of the I/O clock. The MSB of the address is shifted in first. The negative edges of these five I/O clocks shift out the 2nd, 3rd, 4th, 5th, and 6th most significant bits of the previous conversion result. The on-chip sample-and hold begins sampling the newly addressed analog input after the 5th falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Two clock cycles are then applied to the I/O pin and the 7th and 8th conversion bits are shifted out on the negative edges of these clock cycles.
4. The final 8th clock cycle is applied to the I/O clock pin. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 36 system clock cycles. After this final I/O clock cycle, $\overline{CS}$ must go high or the I/O clock must remain low for at least 36 system clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O Clock line. If glitches occur on the I/O Clock line, the I/O sequence between the microprocessor/controller and the device will lose synchronization. Also, if $\overline{CS}$ is taken high, it must remain high until the end of conversion. Otherwise, a valid falling edge of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 system clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

principles of operation (continued)

It is possible to connect the system and I/O clocks together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

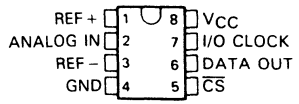
1. When $\overline{CS}$ is recognized by the device to be at a low level, the common clock signal is used as an I/O clock. When the $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used to drive the "conversion crunching" circuitry.
2. The device will recognize a $\overline{CS}$ transition only when the $\overline{CS}$ input changes and subsequently the system clock pin receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles will not shift in the address because a low $\overline{CS}$ must be recognized before the I/O clock can shift in an analog channel address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the 6th I/O clock, which has been recognized by the device, so that a $\overline{CS}$ low level will be recognized upon the lowering of the 8th I/O clock signal recognized by the device. Otherwise, additional common clock cycles will be recognized as I/O clocks and will shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample-and-hold begins sampling upon the negative edge of the 5th I/O clock cycle, the hold function is not initiated until the negative edge of the 8th I/O clock cycle. Thus, the control circuitry can leave the I/O clock signal in its high state during the 8th I/O clock cycle, until the moment at which the analog signal must be converted. The TLC545/546 will continue sampling the analog input until the 8th falling edge of the I/O clock. The control circuitry or software must then immediately lower the I/O clock signal to initiate the hold function at the desired point in time and to start conversion.

Detailed information on interfacing to most popular microprocesors is readily available from the factory.

- LinCMOS™ Technology
- Microprocessor Peripheral or Stand-Alone Operation
- 8-Bit Resolution A/D Converter
- Differential Reference Input Voltages
- Conversion Time . . . 17 μs Max
- Total Access and Conversion Cycles Per Second
  TLC548 . . . up to 45,500
  TLC549 . . . up to 40,000
- On-Chip Software-Controllable Sample-and-Hold
- Total Unadjusted Error . . . ±0.5 LSB Max
- 4-MHz Typical Internal System Clock
- Wide Supply Range . . . 3 V to 6 V
- Low Power Consumption . . . 6 mW Typ
- Ideal for Cost-Effective, High-Performance Applications Including Battery-Operated Portable Instrumentation
- Pinout and Control Signals Compatible with the TLC540 and TLC545 8-Bit A/D Converters and with the TLC1540 10-Bit A/D Converter

TLC548M, TLC549M . . . D OR P PACKAGE
TLC548I, TLC549I . . . D OR P PACKAGE
TLC548C, TLC549C . . . D PACKAGE
(TOP VIEW)



description

The TLC548 and TLC549 are LinCMOS™ A/D peripheral integrated circuits built around an 8-bit switched-capacitor successive-approximation ADC. They are designed for serial interface with a microprocessor or peripheral through a 3-state data output and an analog input. The TLC548 and TLC549 use only the Input/Output Clock (I/O Clock) input along with the Chip Select ($\overline{CS}$) input for data control. The maximum I/O clock input frequency of the TLC548 is guaranteed up to 2.048 megahertz, and the I/O clock input frequency of the TLC549 is guaranteed to 1.1 megahertz. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

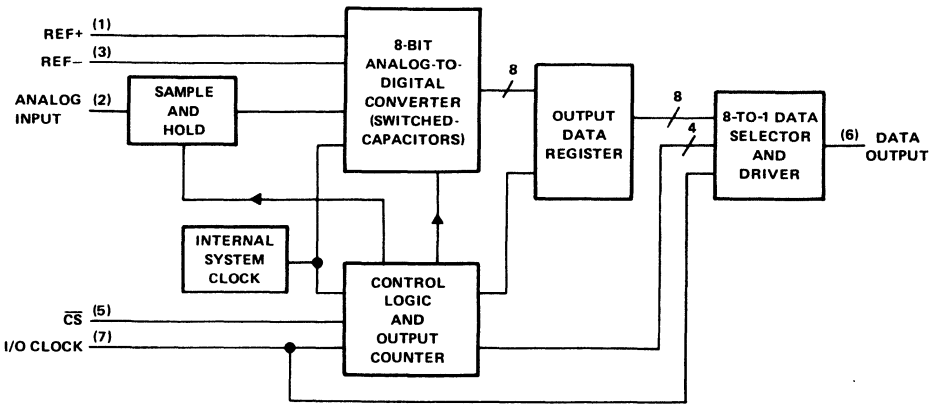
Operation of the TLC548 and the TLC549 is very similar to that of the more complex TLC540 and TLC541 devices; however, the TLC548 and TLC549 provide an on-chip system clock that operates typically at 4 megahertz and requires no external components. The on-chip system clock allows internal device operation to proceed independently of serial input/output data timing and permits manipulation of the TLC548 and TLC549 as desired for a wide range of software and hardware requirements. The I/O Clock together with the internal system clock allow high-speed data transfer and conversion rates of 45,500 conversions per second for the TLC548, and 40,000 conversions per second for the TLC549.

Additional TLC548 and TLC549 features include versatile control logic, an on-chip sample-and-hold circuit that can operate automatically or under microprocessor control, and a high-speed converter with differential high-impedance reference voltage inputs that ease ratiometric conversion, scaling, and circuit isolation from logic and supply noises. Design of the totally switched-capacitor successive-approximation converter circuit allows conversion with a maximum total error of ±0.5 least significant bit (LSB) in less than 17 microseconds.

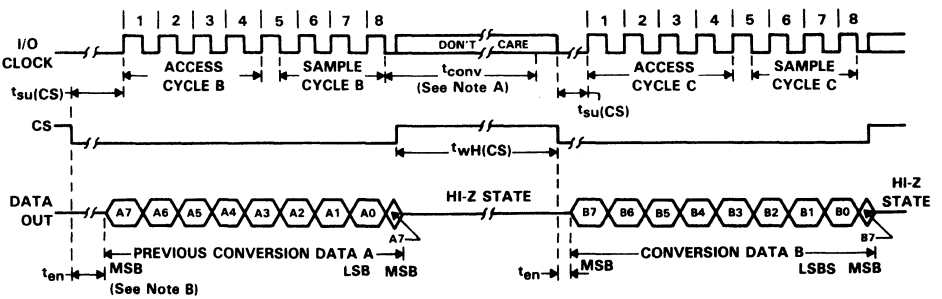
The TLC548M and TLC549M are available in the D or P plastic package and are characterized for operation over the temperature range of −55°C to 125°C. The TLC548I and TLC549I are characterized for operation from −40°C to 85°C. The TLC548C and TLC549C are characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments.

functional block diagram



operating sequence



NOTES: A. The conversion cycle, which requires 36 internal system clock periods (17 μs maximum), is initiated with the 8th I/O clock pulse trailing edge after $\overline{CS}$ goes low for the channel whose address exists in memory at the time.

B. The most significant bit (A7) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6-A0) will be clocked out on the first seven I/O clock falling edges. B7-B0 will follow in the same manner.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range at any input . . . . . −0.3 V to V_{CC} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} + 0.3 V
Peak input current range (any input) . . . . . ±10 mA
Peak total input current range (all inputs) . . . . . ±30 mA
Operating free-air temperature range (see Note 2): TLC548M, TLC549M . . . . . −55°C to 125°C
TLC548I, TLC549I . . . . . −40°C to 85°C
TLC548C, TLC549C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal with the REF− and GND terminal pins connected together, unless otherwise noted.
2. The D package is not guaranteed below −40°C.

recommended operating conditions

		TLC548			TLC549			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		3	5	6	3	5	6	V
Positive reference voltage, V_{REF+} (see Note 3)		2.5	V_{CC}	V_{CC}+0.1	2.5	V_{CC}	V_{CC}+0.1	V
Negative reference voltage, V_{REF-} (see Note 3)		−0.1	0	2.5	−0.1	0	2.5	V
Differential reference voltage, V_{REF+}, V_{REF-} (see Note 3)		1	V_{CC}	V_{CC}+0.2	1	V_{CC}	V_{CC}+0.2	V
Analog input voltage (see Note 3)		0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH} (for V_{CC} = 4.75 V to 5.5 V)		2			2			V
Low-level control input voltage, V_{IL} (for V_{CC} = 4.75 V to 5.5 V)				0.8			0.8	V
Input/output clock frequency, $f_{CLK(I/O)}$ (for V_{CC} = 4.75 V to 5.5 V)		0		2.048	0		1.1	MHz
Input/output clock high, $t_{wH(I/O)}$ (for V_{CC} = 4.75 V to 5.5 V)		200			404			ns
Input/output clock low, $t_{wL(I/O)}$ (for V_{CC} = 4.75 V to 5.5 V)		200			404			ns
Input/output clock transition time, $t_{t(I/O)}$ (see Note 4) (for V_{CC} = 4.75 V to 5.5 V)				100			100	ns
Duration of $\overline{CS}$ input high state during conversion, $t_{wH(CS)}$ (for V_{CC} = 4.75 V to 5.5 V)		17			17			μs
Setup time, $\overline{CS}$ low before first I/O clock, $t_{su(CS)}$ (for V_{CC} = 4.75 V to 5.5 V) (see Note 5)		1.4			1.4			μs
Operating free-air temperature, T_A	TLC548M, TLC549M	−55		125	−55		125	°C
	TLC548I, TLC549I	−40		85	−40		85	
	TLC548C, TLC549C	0		70	0		70	

NOTES: 3. Analog input voltages greater than that applied to REF+ convert to all ones (11111111), while input voltages less than that applied to REF− convert to all zeros (00000000). For proper operation, the positive reference voltage V_{REF+}, must be at least 1 volt greater than the negative reference voltage V_{REF-}. In additon, unadjusted errors may increase as the differential reference voltage $V_{REF+} - V_{REF-}$ falls below 4.75 V.
4. This is the time required for the input/output clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μs for remote data acquisition applications in which the sensor and the ADC are placed several feet away from the controlling microprocessor.
5. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and one falling edge of internal system clock after $\overline{CS}$↓ before responding to control input signals. This $\overline{CS}$ set-up time is given by the t_{en} and $t_{su(CS)}$ specifications.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 2.048 MHz for TLC548 or 1.1 MHz for TLC549

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.75 V, I_{OH} = −360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, I_{OL} = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC}, $\overline{CS}$ at V_{CC}			10	V
			V_O = 0, $\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current, control inputs		V_I = V_{CC}		0.005	2.5	μA
I_{IL}	Low-level input current, control inputs		V_I = 0		−0.005	−2.5	μA
$I_{I(on)}$	Analog channel on-state input current, during sample cycle		Analog input at V_{CC}		0.4	1	μA
			Analog input at 0 V		−0.4	−1	
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V		1.8	2.5	mA
$I_{CC}+I_{REF}$	Supply and reference current		V_{REF+} = V_{CC}		1.9	3	mA
C_i	Input capacitance	Analog inputs			7	55	pF
		Control inputs			5	15	

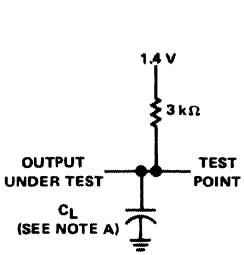
operating characteritics over recommended operating free-air temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 2.048 MHz for TLC548 or 1.1 MHz for TLC549

PARAMETER		TEST CONDITIONS	TLC548			TLC549			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
	Linearity error	See Note 6			±0.5			±0.5	LSB
	Zero error	See Note 7			±0.5			±0.5	LSB
	Full-scale error	See Note 7			±0.5			±0.5	LSB
	Total unadjusted error	See Note 8			±0.5			±0.5	LSB
t_{conv}	Conversion time	See Operating Sequence		8	17		12	17	μs
	Total access and conversion time	See Operating Sequence		12	22		19	25	μs
t_{acq}	Channel acquisition time (sample cycle)	See Operating Sequence			4			4	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓		10			10			ns
t_d	Delay time to data output valid	I/O clock↓			300			400	ns
t_{en}	Output enable time	See Parameter Measurement Information			1.4			1.4	μs
t_{dis}	Output disable time				150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

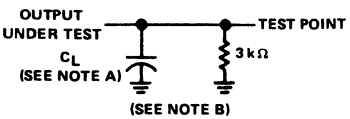
†All typicals are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 6. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
7. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
8. Total unadjusted error is the sum of linearity, zero, and full-scale errors.

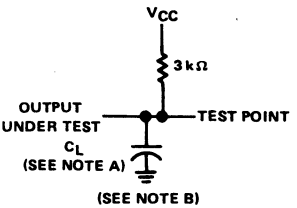
PARAMETER MEASUREMENT INFORMATION



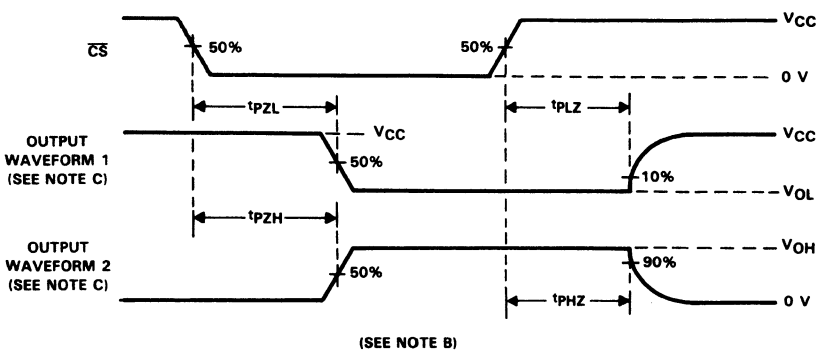
LOAD CIRCUIT FOR t_d, t_r, AND t_f



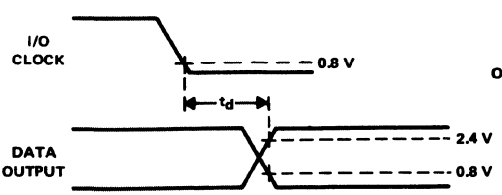
LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}



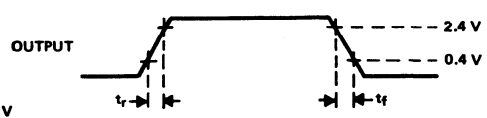
LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME



VOLTAGE WAVEFORM FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC548 and 100 pF for TLC549; C_L includes jig capacitance.
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

PRINCIPLES OF OPERATION

The TLC548 and TLC549 are each complete data acquisition systems on a single chip. Each contains an internal system clock, sample-and-hold, 8-bit A/D converter, data register, and control logic circuitry. For flexibility and access speed, there are two control inputs: I/O Clock and Chip Select ($\overline{CS}$). These control inputs and a TTL-compatible three-state output facilitate serial communications with a microprocessor or minicomputer. A conversion can be completed in 17 microseconds or less, while complete input-conversion-output cycles can be repeated in 22 microseconds for the TLC548 and in 25 microseconds for the TLC549.

The internal system clock and I/O clock are used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Due to this independence and the internal generation of the system clock, the control hardware and software need only be concerned with reading the previous conversion result and starting the conversion by using the I/O clock. In this manner, the internal system clock drives the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the data output pin is in a high-impedance condition and the I/O clock pin is disabled. This $\overline{CS}$ control function allows the I/O Clock pin to share the same control logic point with its counterpart pin when additional TLC548 and TLC549 devices are used. This also serves to minimize the required control logic pins when using multiple TLC548 and TLC549 devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the internal system clock after a $\overline{CS}\downarrow$ before the transition is recognized. However, upon a $\overline{CS}$ rising edge, DATA OUT will go to a high-impedance state within the t_{dis} specification even though the rest of the IC's circuitry will not recognize the transition until the $t_{su(CS)}$ specification has elapsed. This technique is used to protect the device against noise when used in a noisy environment. The most significant bit (MSB) of the previous conversion result will initially appear on the DATA OUT pin when $\overline{CS}$ goes low.
2. The falling edges of the first four I/O clock cycles shift out the 2nd, 3rd, 4th, and 5th most significant bits of the previous conversion result. The on-chip sample-and-hold begins sampling the analog input after the 4th high-to-low transition of the I/O Clock. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three more I/O clock cycles are then applied to the I/O pin and the 6th, 7th, and 8th conversion bits are shifted out on the falling edges of these clock cycles.
4. The final, (the 8th), clock cycle is applied to the I/O clock pin. The on-chip sample-and-hold begins the hold function upon the high-to-low transition of this clock cycle. The hold function will continue for the next four internal system clock cycles, after which the holding function terminates and the conversion is performed during the next 32 system clock cycles, giving a total of 36 cycles. After the 8th I/O clock cycle, $\overline{CS}$ must go high or the I/O clock must remain low for at least 36 internal system clock cycles to allow for the completion of the hold and conversion functions. $\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O Clock line. If glitches occur on the I/O Clock line, the I/O sequence between the microprocessor/controller and the device will lose synchronization. If $\overline{CS}$ is taken high, it must remain high until the end of conversion. Otherwise, a valid high-to-low transition of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 internal system clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

PRINCIPLES OF OPERATION

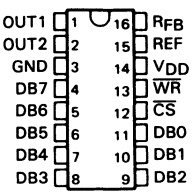
For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample-and-hold begins sampling upon the high-to-low transition of the 4th I/O clock cycle, the hold function does not begin until the high-to-low transition of the 8th I/O clock cycle, which should occur at the moment when the analog signal must be converted. The TLC548 and TLC549 will continue sampling the analog input until the high-to-low transition of the 8th I/O clock pulse. The control circuitry or software will then immediately lower the I/O clock signal and start the holding function to hold the analog signal at the desired point in time and start conversion.

Detailed information on interfacing to the most popular microprocessor is readily available from Texas Instruments.

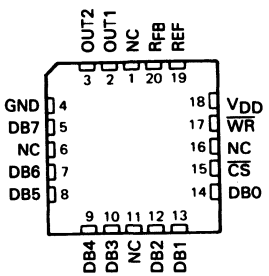
- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonic over the Entire A/D Conversion Range**
- **Segmented High-Order Bits Ensure Low-Glitch Output**
- **Designed to be Interchangeable with Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320**

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	½ LSB Max
Power dissipation at V_{DD} = 5 V	5 mW Max
Settling time	100 ns Max
Propagation delay	80 ns Max

D OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TLC7524 is an Advanced LinCMOS™ 8-bit digital-to-analog converter (DAC) designed for easy interface to most popular microprocessors.

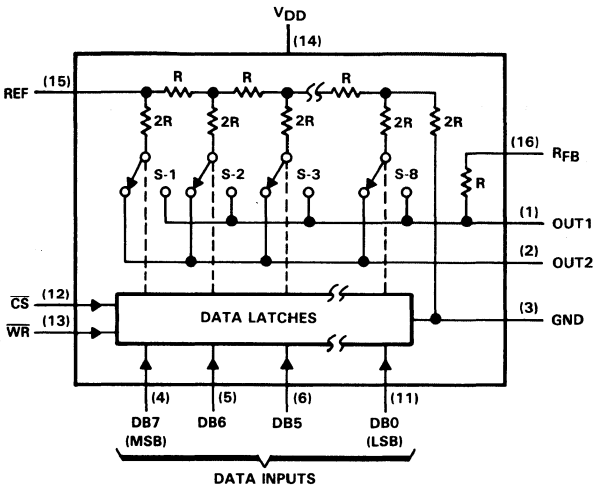
The TLC7524 is an 8-bit multiplying DAC with input latches and with a load cycle similar to the "write" cycle of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most-significant bits, which produce the highest glitch impulse. The TLC7524 provides accuracy to ½ LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5 milliwatts typically.

Featuring operation from a 5-V to 15-V single supply, the TLC7524 interfaces easily to most microprocessor buses or output ports. Excellent multiplying (2 or 4 quadrant) makes the TLC7524 an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

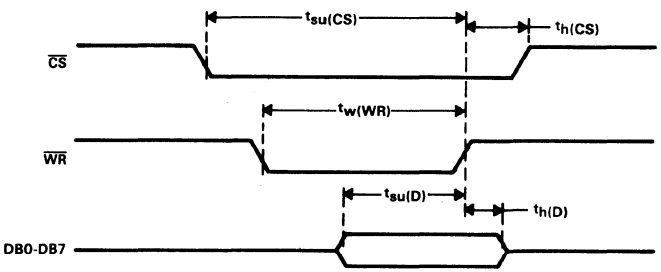
The TLC7524I is characterized for operation from −25°C to 85°C, and the TLC7524C is characterized for operation from 0°C to 70°C.

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} . . . . . −0.3 V to 16.5 V
Digital input voltage, V_I . . . . . −0.3 V to V_{DD} +0.3 V
Reference voltage, V_{ref} . . . . . ±25 V
Peak digital input current, I_I . . . . . 10 μA
Operating free-air temperature range: TLC7524I . . . . . −25°C to 85°C
TLC7524C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

recommended operating conditions

		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V_{ref}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input voltage, V_{IL}				0.8			1.5	V
CS setup time, $t_{su(CS)}$		40			40			ns
CS hold time, $t_{h(CS)}$		0			0			ns
Data bus input setup time, $t_{su(D)}$		25			25			ns
Data bus input hold time, $t_{h(D)}$		10			10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		40			40			ns
Operating free-air temperature, T_A	TLC7524I	−25		85	−25		85	°C
	TLC7524C	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range, V_{ref} = ±10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{IH}	High-level input current		$V_I = V_{DD}$			10			10	μA
I_{IL}	Low-level input current		V_I = 0			−10			−10	μA
I_{lkg}	Output leakage current	OUT1	DB0-DB7 at 0 V, $\overline{WR}$, $\overline{CS}$ at 0 V, V_{ref} = ±10 V			±400			±200	nA
		OUT2	DB0-DB7 at V_{DD}, $\overline{WR}$, $\overline{CS}$ at 0 V, V_{ref} = ±10 V			±400			±200	
I_{DD}	Supply current	Quiescent	DB0-DB7 at V_{IH}min or V_{IL}max			1			2	mA
		Standby	DB0-DB7 at 0 V or V_{DD}			500			500	μA
k_{SVS}	Supply voltage sensitivity, $\Delta gain/\Delta V_{DD}$		ΔV_{DD} = ±10%		0.01	0.16		0.005	0.04	%FSR/%
C_i	Input capacitance, DB0-DB7, $\overline{WR}$, $\overline{CS}$		V_I = 0			5			5	pF
C_o	Output capacitance	OUT1	DB0-DB7 at 0 V,			30			30	pF
		OUT2	$\overline{WR}$ and $\overline{CS}$ at 0 V			120			120	
C_o	Output capacitance	OUT1	DB0-DB7 at V_{DD},			120			120	pF
		OUT2	$\overline{WR}$ and $\overline{CS}$ at 0 V			30			30	
	Reference input impedance (Pin 15 to GND)			5		20	5		20	kΩ

operating characteristics over recommended operating free-air temperature range, V_{ref} = ±10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Linearity error				±0.5			±0.5	LSB
Gain error	See Note 1			±2.5			±2.5	LSB
Settling time (to ½ LSB)	See Note 2			100			100	ns
Propagation delay from digital input to 90% of final analog output current	See Note 2			80			80	ns
Feedthrough at OUT1 or OUT2	V_{ref} = ±10 V (100-kHz sinewave) $\overline{WR}$ and $\overline{CS}$ at 0 V, DB0-DB7 at 0 V			0.5			0.5	%FSR
Temperature coefficient of gain	T_A = 25°C to MAX		±0.004			±0.001		%FSR/°C

†Typical values at T_A = 25°C.

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
2. OUT1 load = 100 Ω, C_{ext} = 13 pF, $\overline{WR}$ at 0 V, $\overline{CS}$ at 0 V, DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.

principles of operation

The TLC7524 is an 8-bit multiplying D/A converter consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded and these decoded bits, through a modification in the R-2R ladder, control three equally weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 1. With all digital inputs low, the entire reference current, I_{ref}, is switched to OUT2. The current source I/256 represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30 pF maximum) appears at OUT2 and the on-state switch capacitance (120 pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 1. Analysis of the circuit for all digital inputs high is similar to Figure 1; however, in this case, I_{ref} would be switched to OUT1.

Interfacing the TLC7524 D/A converter to a microprocessor is accomplished via the data bus and the $\overline{CS}$ and $\overline{WR}$ control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the TLC7524 analog output responds to the data activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs are latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The TLC7524 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

principles of operation (continued)

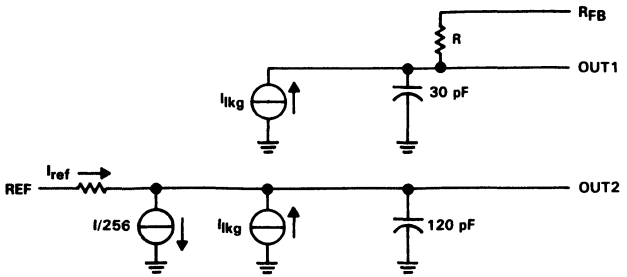


FIGURE 1. TLC7524 EQUIVALENT CIRCUIT WITH ALL DIGITAL INPUTS LOW

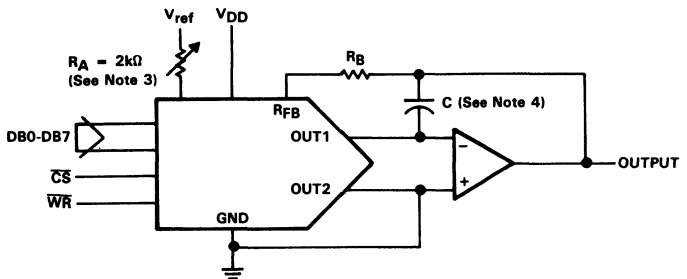


FIGURE 2. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

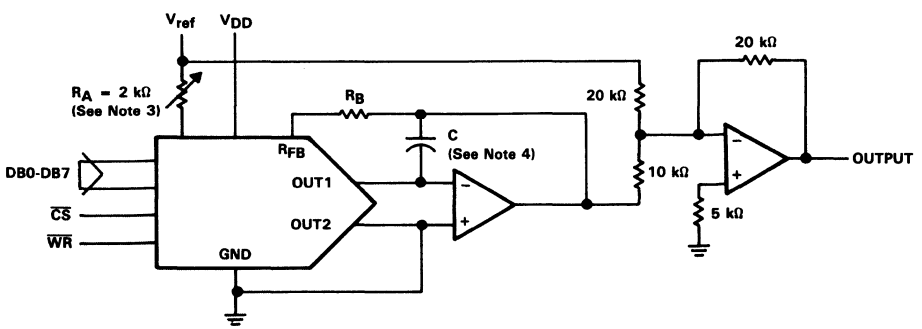


FIGURE 3. BIPOLAR OPERATION (4-QUADRANT OPERATION)

NOTES: 3. R_A and R_B used only if gain adjustment is required.
4. C phase compensation (10-15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

principles of operation (continued)

TABLE 1. UNIPOLAR BINARY CODE

DIGITAL INPUT (SEE NOTE 5) MSB LSB	ANALOG OUTPUT
11111111	$-V_{ref}$ (255/256)
10000001	$-V_{ref}$ (129/256)
10000000	$-V_{ref}$ (128/256) = $-V_{ref}/2$
01111111	$-V_{ref}$ (127/256)
00000001	$-V_{ref}$ (1/256)
00000000	0

TABLE 2. BIPOLAR (OFFSET BINARY) CODE

DIGITAL INPUT (SEE NOTE 6) MSB LSB	ANALOG OUTPUT
11111111	V_{ref} (127/128)
10000001	V_{ref} (1/128)
10000000	0
01111111	$-V_{ref}$ (1/128)
00000001	$-V_{ref}$ (127/128)
00000000	$-V_{ref}$

NOTES: 5. LSB = 1/256 (V_{ref}).
6. LSB = 1/128 (V_{ref}).

microprocessor interfaces

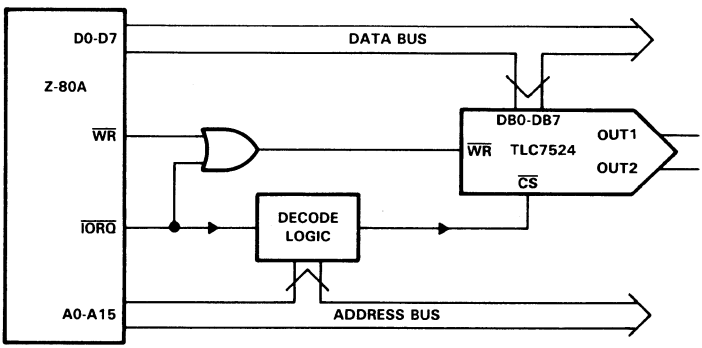


FIGURE 4. TLC7524—Z-80A INTERFACE

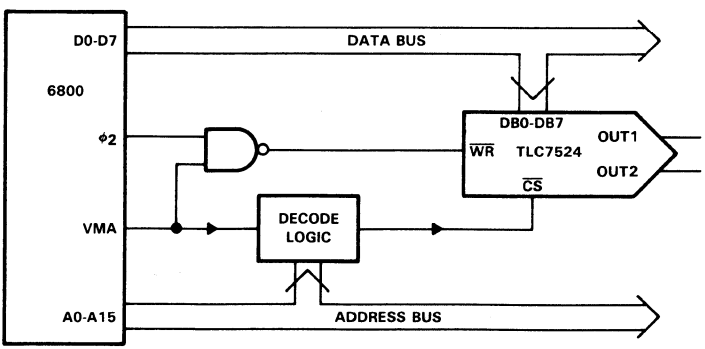


FIGURE 5. TLC7524—6800 INTERFACE

microprocessor interfaces (continued)

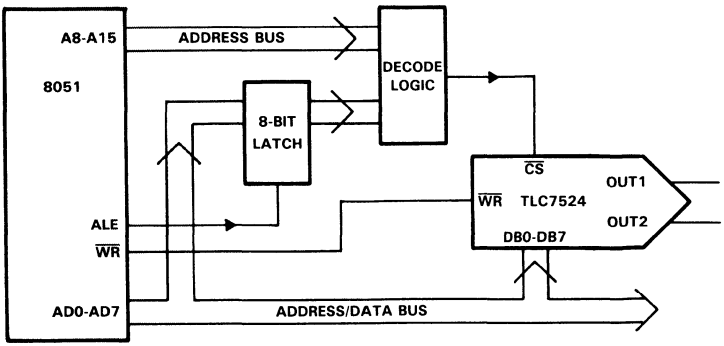
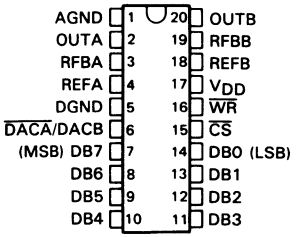


FIGURE 6. TLC7524–8051 INTERFACE

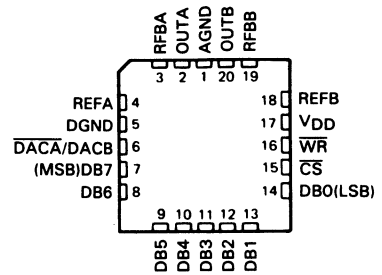
- **ADVANCED LinCMOS™ Silicon-Gate Technology**
- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Guaranteed Monotonicity**
- **Designed to be Interchangeable with Analog Devices AD7528 and PMI PM-7528**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320**

DW OR N PACKAGE
(TOP VIEW)



KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 bits
Linearity Error	1/2 LSB
Power Dissipation at V_{DD} = 5 V	5 mW
Settling Time at V_{DD} = 5 V	100 ns
Propagation Delay at V_{DD} = 5 V	80 ns

FN PACKAGE
(TOP VIEW)



description

The TLC7528 is a dual 8-bit digital-to-analog converter designed with separate on-chip data latches and featuring excellent DAC-to-DAC matching. Data is transferred to either of the two DAC data latches via a common 8-bit input port. Control input DACA/DACB determines which DAC is to be loaded. The "load" cycle of the TLC7528 is similar to the "write" cycle of a random-access memory, allowing easy interface to most popular microprocessor busses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

The TLC7528 operates from a 5-volt to 15-volt power supply and dissipates less than 15 mW (typical). Excellent 2- or 4-quadrant multiplying makes the TLC7528 a sound choice for many microprocessor-controlled gain-setting and signal-control applications.

The TLC7528I is characterized for operation from −25 to 85°C. The TLC7528C is characterized for operation from 0°C to 70°C.

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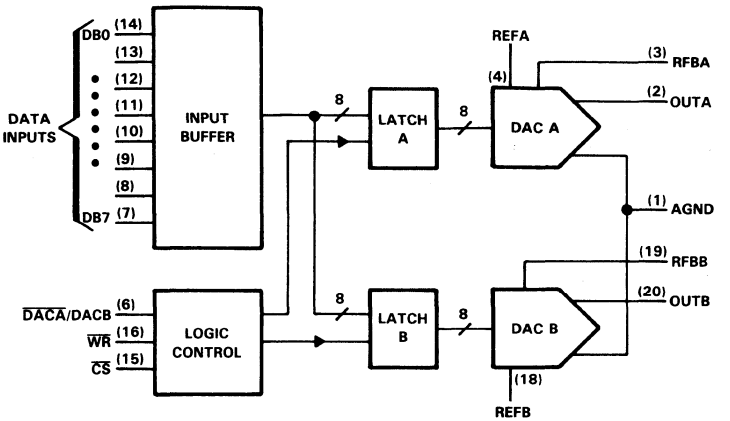
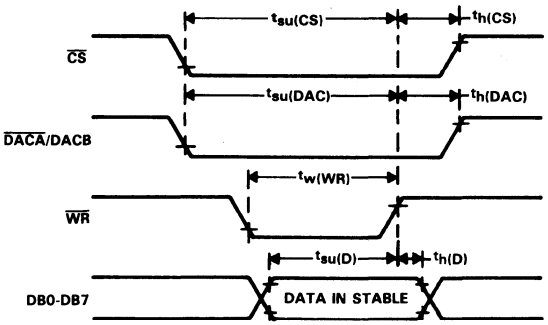
functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (to AGND or DGND) . . . . . −0.3 V to 16.5 V
Voltage between AGND and DGND . . . . . ±V_{DD}
Input voltage, V_I (to DGND) . . . . . −0.3 V to V_{DD} + 0.3
Reference voltage, V_{refA} or V_{refB} (to AGND) . . . . . ±25 V
Output voltage, V_{OA} or V_{OB} (to AGND) . . . . . ±25 V
Peak input current . . . . . 10 μA
Operating free-air temperature range: TLC7528I . . . . . −25°C to 85°C
TLC7528C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

recommended operating conditions

		V_{DD} = 4.75 V to 5.25 V			V_{DD} = 14.5 V to 15.5 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Reference voltage, V_{refA} or V_{refB}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input voltage, V_{IL}				0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$		50			50			ns
$\overline{CS}$ hold time, $t_{h(CS)}$		0			0			ns
DAC select setup time, $t_{su(DAC)}$		50			50			ns
DAC select hold time, $t_{h(DAC)}$		10			10			ns
Data bus input setup time $t_{su(D)}$		25			25			ns
Data bus input hold time $t_{h(D)}$		0			0			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		50			50			ns
Operating free-air temperature, T_A	TLC7528I	−25		85	−25		85	°C
	TLC7528C	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{IH}	High-level input current		V_I = V_{DD}			10			10	μA
I_{IL}	Low-level input current		V_I = 0 V			−10			−10	μA
	Reference input impedance (Pin 15 to GND)			5	12	20	5	12	20	kΩ
I_{lkg}	Output leakage current	OUTA	DACA data latch loaded with 00000000, V_{refA} = ±10 V			±400			±200	nA
		OUTB	DACB data latch loaded with 00000000, V_{refB} = ±10 V			±400			±200	
	Input resistance match (REFA to REFB)					±1%			±1%	
	DC supply sensitivity, Δ gain/Δ V_{DD}		ΔV$_{DD}$ = ±10%			0.04			0.02	%/%
I_{DD}	Supply current (quiescent)		DB0-DB7 at V_{IH}min or V_{IL}max			1			1	mA
I_{DD}	Supply current (standby)		DB0-DB7 at 0 V or V_{DD}			0.5			0.5	mA
C_i	Input capacitance	DB0-DB7				10			10	pF
		$\overline{WR}$, $\overline{CS}$ $\overline{DACA}$/DACB				15			15	
C_o	Output capacitance, (OUTA, OUTB)		DAC data latches loaded with 00000000			50			50	pF
			DAC data latches loaded with 11111111			120			120	

†All typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Linearity error					±1/2			±1/2	LSB
Settling time (to 1/2 LSB)		See Note 1			100			100	ns
Gain error		See Note 2			2.5			2.5	LSB
AC feedthrough	REFA to OUTA	See Note 3			−65			−65	dB
	REFB to OUTB				−65			−65	
Temperature coefficient of gain		See Note 4			0.007			0.0035	%FSR/°C
Propagation delay (from digital input to 90% of final analog output current)		See Note 5			80			80	ns
Channel-to-channel isolation	REFA to OUTB	See Note 6		77			77		dB
	REFB to OUTA	See Note 7		77			77		
Digital-to-analog glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C		160			440		nVs
Digital crosstalk glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C		30			60		nVs
Harmonic distortion		V_i = 6 V rms, f = 1 kHz, T_A = 25°C		−85			−85		dB

NOTES: 1. OUTA, OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
2. Gain error is measured using an internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
3. V_{ref} = 20 V peak-to-peak, 100-kHz sine wave; DAC data latches loaded with 00000000.
4. Temperature coefficient of gain measured from 0°C to 25°C or from 25°C to 70°C.
5. V_{refA} = V_{refB} = 10 V; OUTA/OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
6. Both DAC latches loaded with 11111111; V_{refA} = 20 V peak-to-peak, 100-kHz sine wave; V_{refB} = 0; T_A = 25°C.
7. Both DAC latches loaded with 11111111; V_{refB} = 20 V peak-to-peak, 100-kHz sine wave; V_{refA} = 0; T_A = 25°C.

principles of operation

The TLC7528 contains two identical 8-bit multiplying D/A converters, DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA with all digital inputs low is shown in Figure 1.

Figure 2 shows the DACA equivalent circuit. A similar equivalent circuit can be drawn for DACB. Both DACs share the analog ground pin 1 (AGND). With all digital inputs high, the entire reference current flows to OUTA. A small leakage current (I_{lkg}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. C_O is due to the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_O is 50 pF to 120 pF maximum. The equivalent output resistance r_O varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

Interfacing the TLC7528 to a microprocessor is accomplished via the data bus, $\overline{CS}$, $\overline{WR}$, and $\overline{DACA}$/DACB control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the TLC7528 analog output, specified by the $\overline{DACA}$/DACB control line, responds to the activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs is latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The digital inputs of the TLC7528 provide TTL compatibility when operated from a supply voltage of 5 V. The TLC7528 may be operated with any supply voltage in the range from 5 V to 15 V, however, input logic levels are not TTL compatible above 5 V.

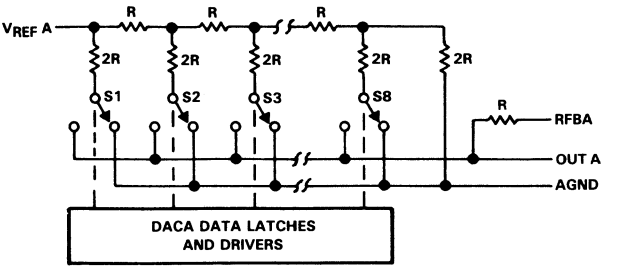


FIGURE 1. SIMPLIFIED FUNCTIONAL CIRCUIT FOR DACA

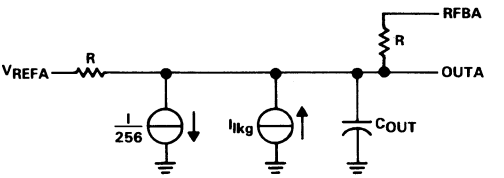


FIGURE 2. TLC7528 EQUIVALENT CIRCUIT, DACA LATCH LOADED WITH 11111111.

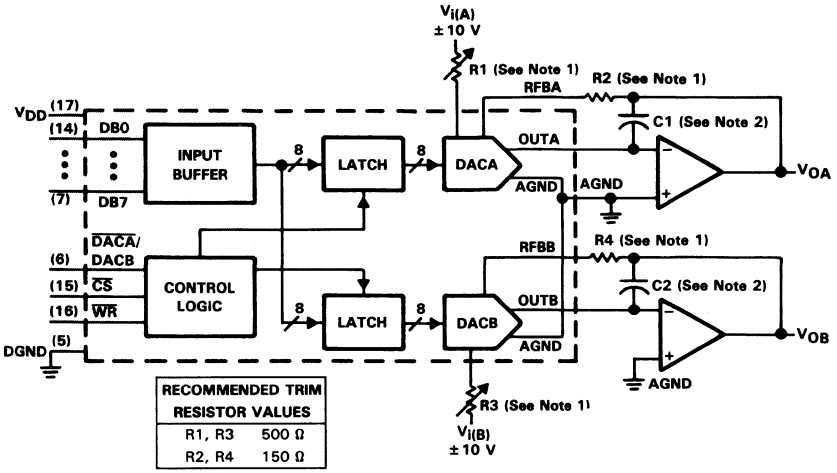
MODE SELECTION TABLE

$\overline{DACA}$/DACB	$\overline{CS}$	$\overline{WR}$	DACA	DACB
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = low level, H = high level, X = don't care

TYPICAL APPLICATION DATA

The TLC7528 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 3 and 4. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

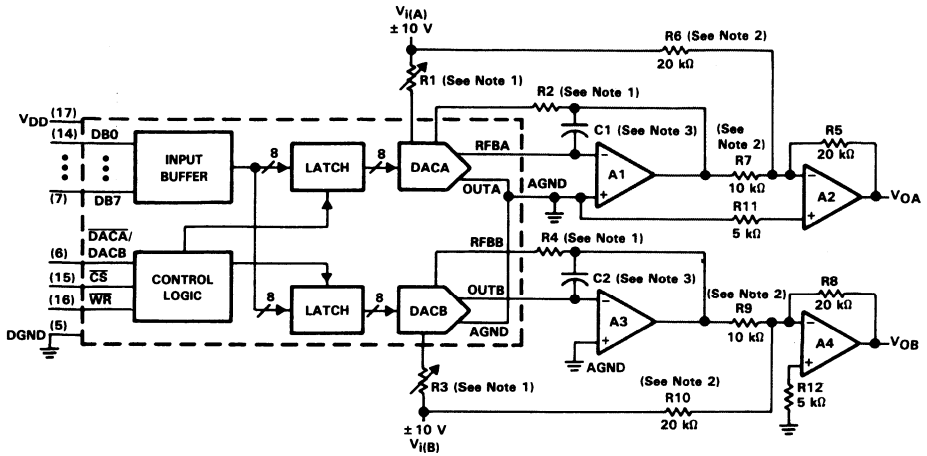


RECOMMENDED TRIM RESISTOR VALUES	
R1, R3	500 Ω
R2, R4	150 Ω

NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.
2. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

FIGURE 3. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

TYPICAL APPLICATION DATA



NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table in Figure 5 for recommended values. Adjust R1 for V_{OA} = 0 V with code 10000000 in DACA latch. Adjust R3 for V_{OB} = 0 V with 10000000 in DACB latch.
2. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
3. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

FIGURE 4. BIPOLAR OPERATION (4-QUADRANT OPERATION)

TABLE 1. UNIPOLAR BINARY CODE

DAC LATCH CONTENTS MSB LSB†	ANALOG OUTPUT
11111111	$-V_i$ (255/256)
10000001	$-V_i$ (129/256)
10000000	$-V_i$ (128/256) = $-V_i/2$
01111111	$-V_i$ (127/256)
00000001	$-V_i$ (1/256)
00000000	$-V_i$ (0/256) = 0

† 1 LSB = $(2^{-8})V_i$

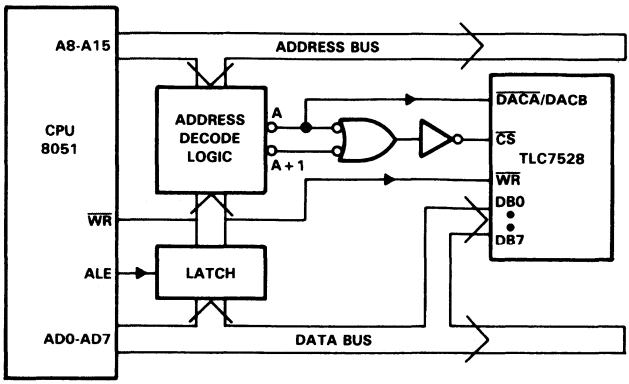
TABLE 2. BIPOLAR (OFFSET BINARY) CODE

DAC LATCH CONTENTS MSB LSB‡	ANALOG OUTPUT
11111111	V_i (127/128)
10000001	V_i (1/128)
10000000	0 V
01111111	$-V_i$ (1/128)
00000001	$-V_i$ (127/128)
00000000	$-V_i$ (128/128)

‡ 1 LSB = $(2^{-7})V_i$

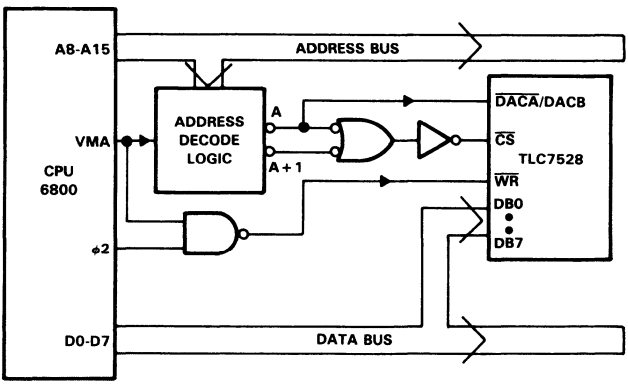
TYPICAL APPLICATION DATA

microprocessor interface information



NOTE: A = decoded address for TLC7528 DACA.
A+1 = decoded address for TLC7528 DACB.

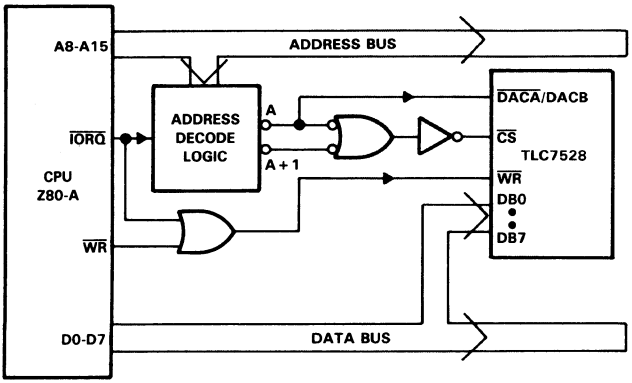
FIGURE 5. TLC7528 – INTEL 8051 INTERFACE



NOTE: A = decoded address for TLC7528 DACA.
A+1 = decoded address for TLC7528 DACB.

FIGURE 6. TLC7528 – 6800 INTERFACE

TYPICAL APPLICATION DATA



NOTE: A = decoded address for TLC7528 DACA.
A + 1 = decoded address for TLC7528 DACB.

FIGURE 7. TLC7528 TO Z80-A INTERFACE

programmable window detector

The programmable window comparator shown in Figure 8 will determine if voltage applied to the DAC feedback resistors are within the limits programmed into the TLC7528 data latches. Input signal range depends on the reference and polarity, that is, the test input range is 0 to $-V_{ref}$. The DACA and DACB data latches are programmed with the upper and lower test limits. A signal within the programmed limits will drive the output high.

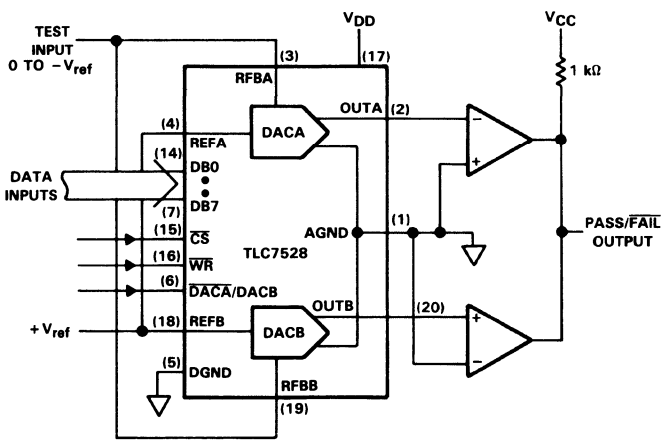


FIGURE 8. DIGITALLY PROGRAMMABLE WINDOW COMPARATOR (UPPER- AND LOWER-LIMIT TESTER)

TYPICAL APPLICATION DATA

digitally controlled signal attenuator

Figure 9 shows the TLC7528 configured as a two-channel programmable attenuator. Applications include stereo audio and telephone signal level control. Table 3 shows input codes vs attenuation for a 0 to 15.5 dB range.

Attentuation db = $-20 \log_{10} D/256$, D = digital input code

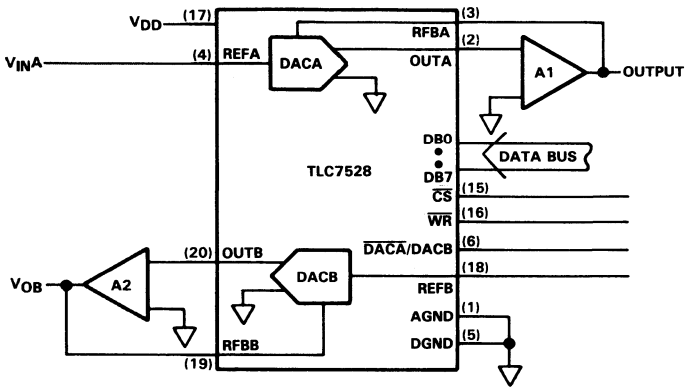


FIGURE 9. DIGITALLY CONTROLLED DUAL TELEPHONE ATTENUATOR

TABLE 3. ATTENUATION vs DACA, DACB CODE

ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL	ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL
0	11111111	255	8.0	01100110	102
0.5	11110010	242	8.5	01100000	96
1.0	11100100	228	9.0	01011011	91
1.5	11010111	215	9.5	01010110	86
2.0	11001011	203	10.0	01010001	81
2.5	11000000	192	10.5	01001100	76
3.0	10110101	181	11.0	01001000	72
3.5	10101011	171	11.5	01000100	68
4.0	10100010	162	12.0	01000000	64
4.5	10011000	152	12.5	00111101	61
5.0	10010000	144	13.0	00111001	57
5.5	10001000	136	13.5	00110110	54
6.0	10000000	128	14.0	00110011	51
6.5	01111001	121	14.5	00110000	48
7.0	01110010	114	15.0	00101110	46
7.5	01101100	108	15.5	00101011	43

TYPICAL APPLICATION DATA

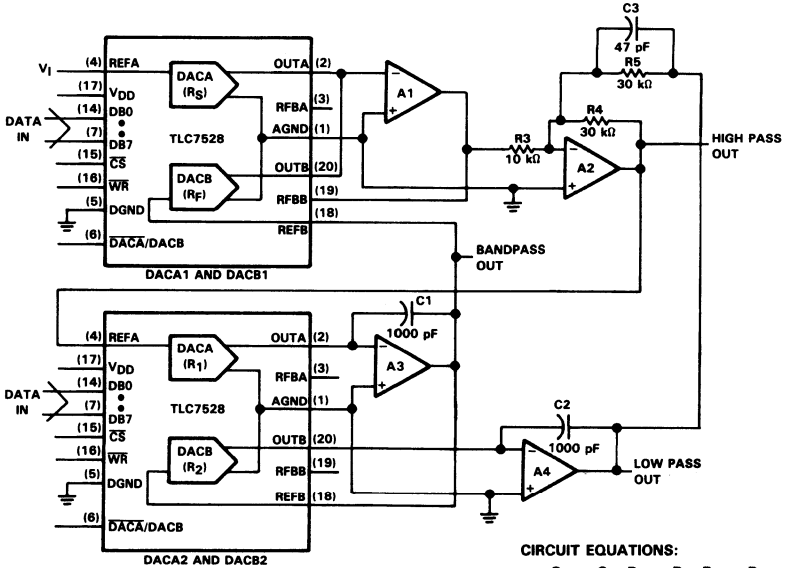
programmable state-variable filter

This programmable state-variable or universal filter configuration provides low-pass, high-pass, and band-pass outputs, and is suitable for applications in which microprocessor control of filter parameters is required.

As shown in Figure 10, DACA1 and DACB1 control the gain and Q of the filter while DACA2 and DACB2 control the cutoff frequency. Both halves of the DACA2 and DACB2 must track accurately in order for the cutoff-frequency equation to be true. With the TLC7528, this is easily achieved.

$$f_C = \frac{1}{2\pi\ R1\ C1}$$

The programmable range for the cutoff or center frequency is 0 to 15 kHz with a Q ranging from 0.3 to 4.5. This defines the limits of the component values.



CIRCUIT EQUATIONS:

$C_1 = C_2,\ R_1 = R_2,\ R_4 = R_5$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{fb(DACB1)}}$$

$$A_o = -\frac{R_F}{R_S}$$

NOTES: A. Op-amps A1, A2, A3, and A4 are TL287.

B. C3 compensates for the op-amp gain-bandwidth limitations.

C. DAC equivalent resistance equals $\frac{256 \times (\text{DAC ladder resistance})}{\text{DAC digital code}}$

FIGURE 10. DIGITALLY CONTROLLED STATE-VARIABLE FILTER

General Information 1

Thermal Information 2

Special Functions 5

Voltage Regulators 6

Data Acquisition 7

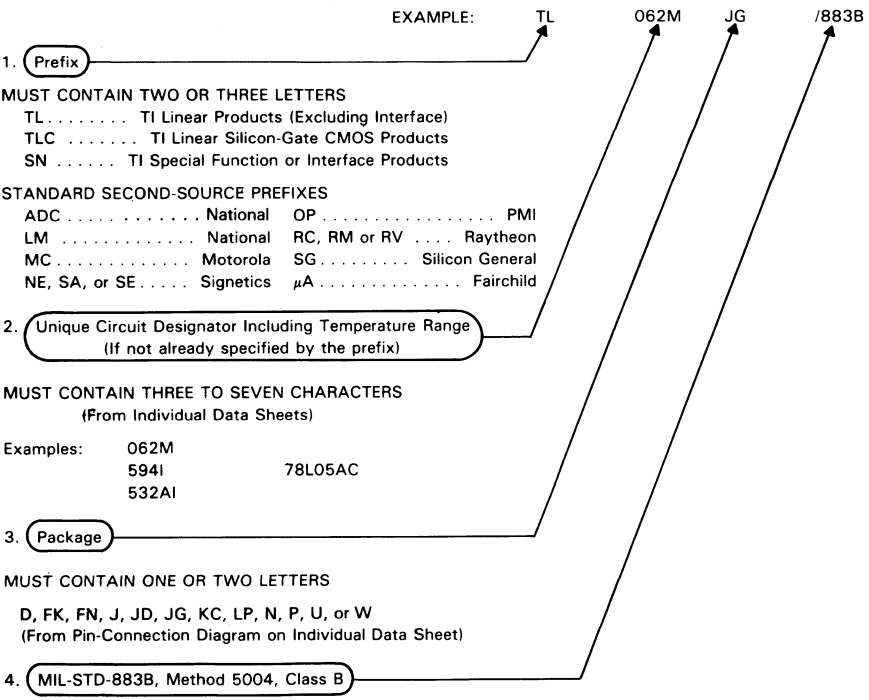
Appendix A

Appendix A

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as explained in the following example.



Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specififed by the customer (with possible additional costs), circuits will be shipped on the most practical carrier.

Dual-In-Line (D, J, JD, JG, N, P)
- —Slide Magazines
- —A-Channel Plastic Tubing
- —Barnes Carrier
- —Sectioned Cardboard Box
- —Individual Cardboard Box

Plug-In (LP)
- —Barnes Carrier
- —Sectional Cardboard Box
- —Individual Cardboard Box

Chip Carriers (FK, FN)
- —Anti-Static Plastic Tubing

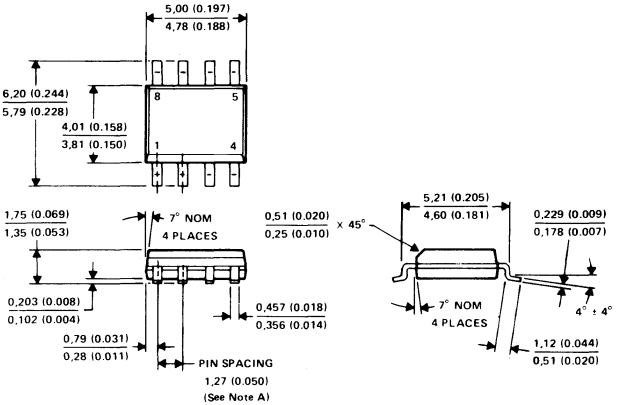
Flat (U, W)
- —Barnes Carrier
- —Milton Ross Carrier

TO-220AB (KC)
- —Sleeves

D plastic dual-in-line packages

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

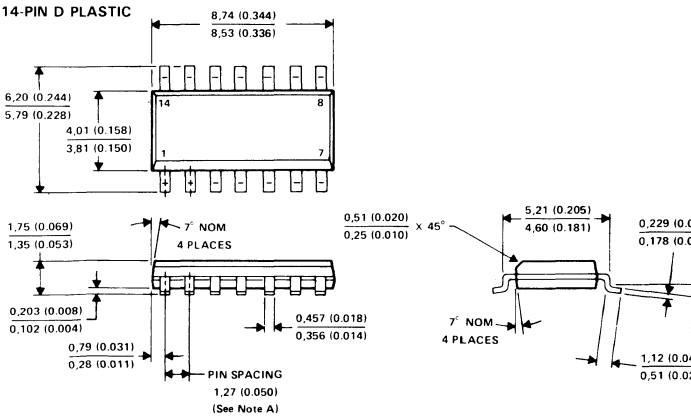
8-PIN D PLASTIC



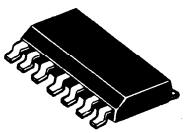
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOT TO SCALE

14-PIN D PLASTIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES



NOT TO SCALE

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

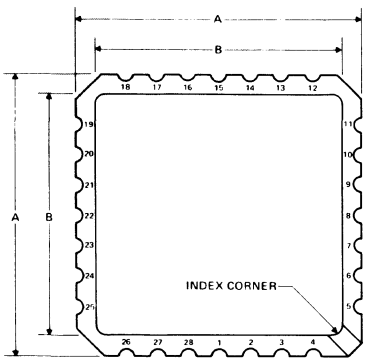
FK ceramic chip carrier package

This hermetically sealed chip carrier package has a ceramic base.
The FK package has a three-layer base with a metal lid and braze seal.

The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.

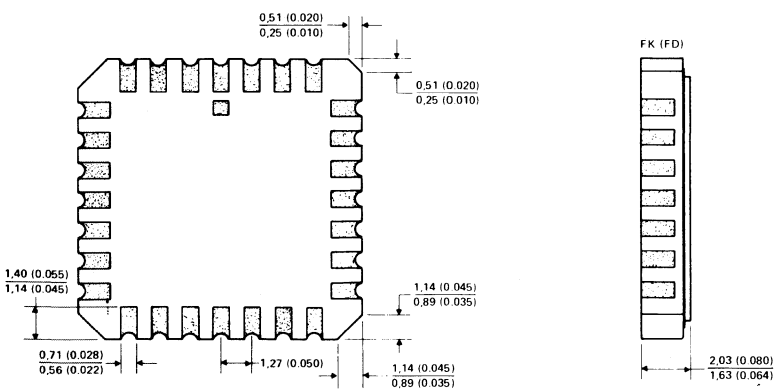
FK CERAMIC CHIP CARRIER PACKAGES
(28-terminal package shown)



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)

*All dimensions and notes for the specified JEDEC outline apply.



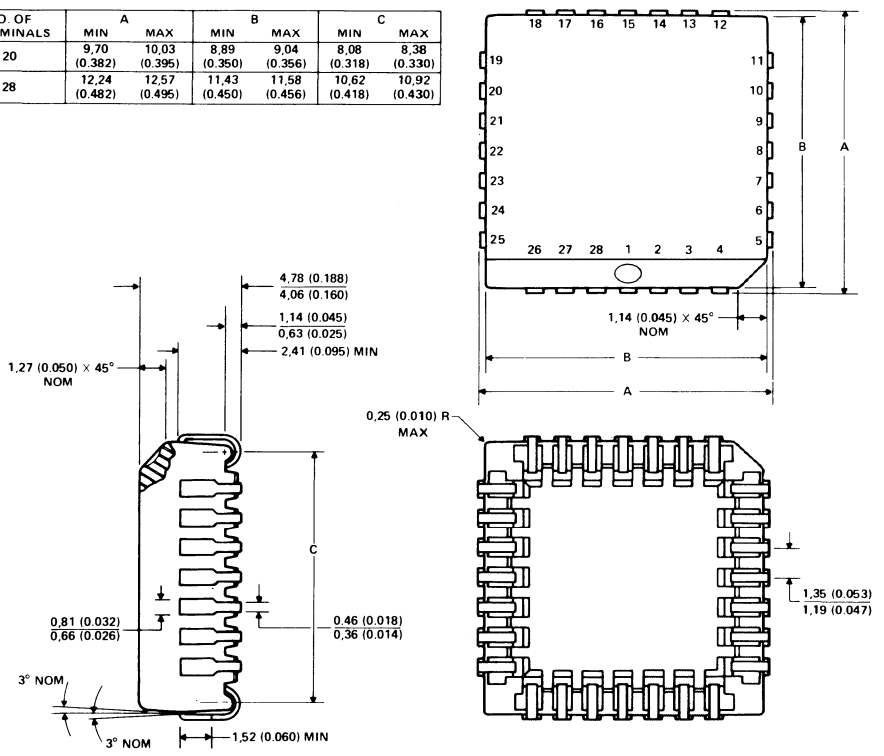
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

FN plastic chip carrier package

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN PLASTIC CHIP CARRIER PACKAGE
(28-terminal package shown)

NO. OF TERMINALS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
20	9,70 (0.382)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	8,08 (0.318)	8,38 (0.330)
28	12,24 (0.482)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,62 (0.418)	10,92 (0.430)



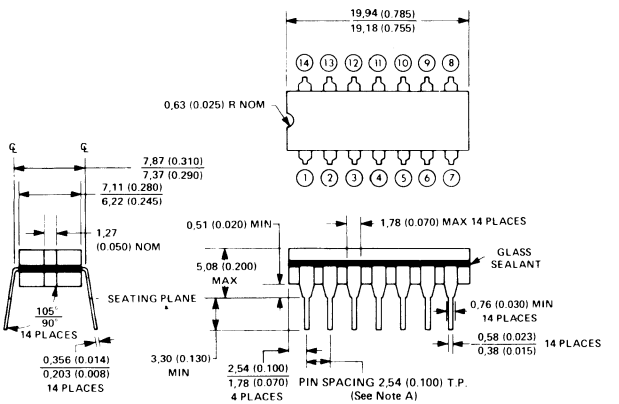
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

Appendix A

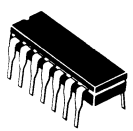
J ceramic dual-in-line packages

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldering assembly.

14-PIN J CERAMIC

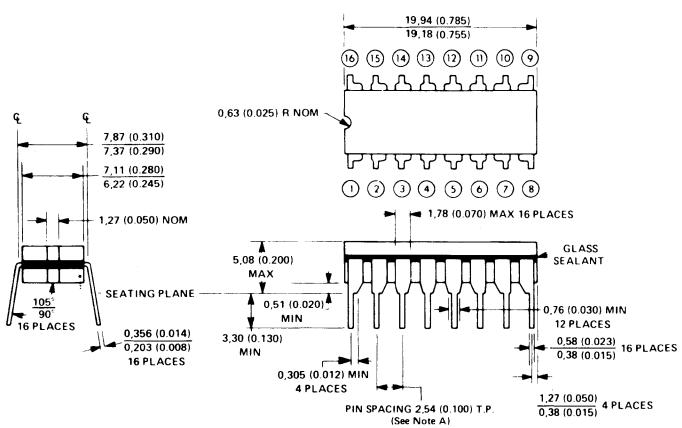


Falls Within JEDEC TO-116 and MO-001AA Dimensions
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

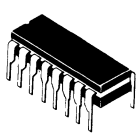


NOT TO SCALE

16-PIN J CERAMIC



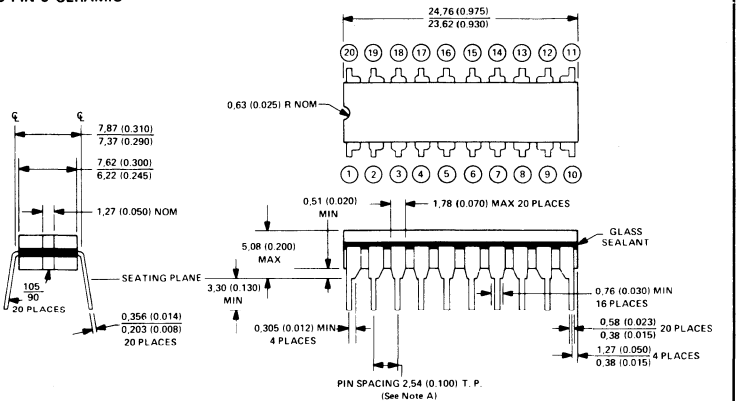
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

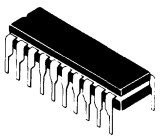


NOT TO SCALE

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

20-PIN J CERAMIC





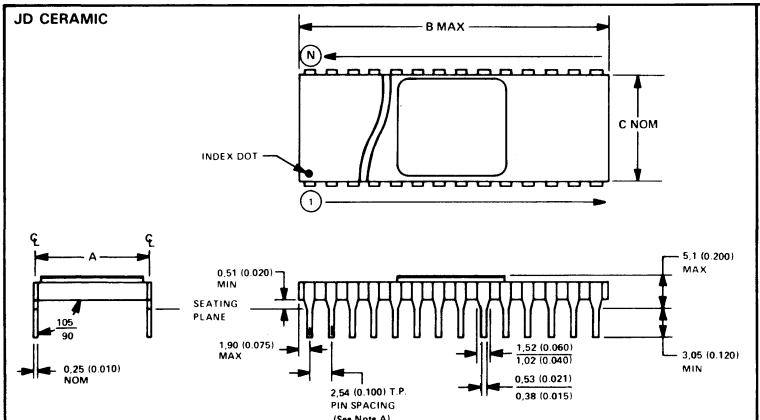
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

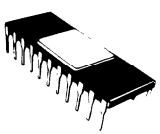
NOT TO SCALE

ceramic dual-in-line packages—side-braze (JD)

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.

JD CERAMIC





DIM \ PINS	28	40
A ± 0,25 (0.010)	15,24 (0.600)	15,24 (0.600)
B MAX	36,8 (1.45)	52,1 (2.05)
C NOM	15,0 (0.590)	15.0 (0.590)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

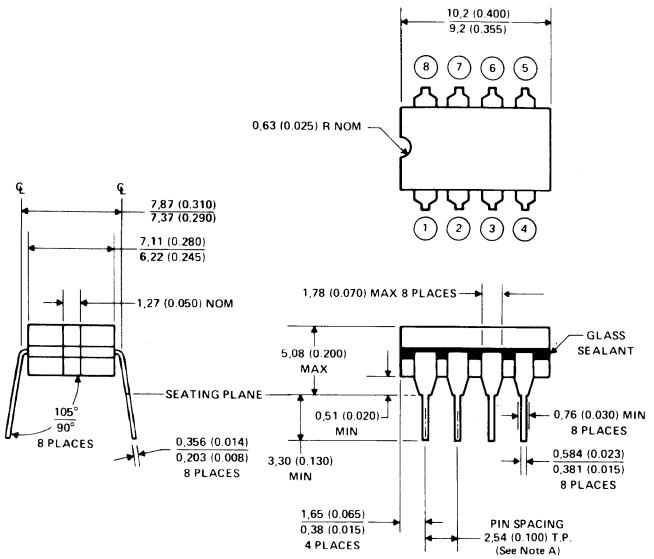
NOT TO SCALE

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

JG ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. The package is intended for insertion in mounting-hole rows 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering.

8-PIN JG CERAMIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

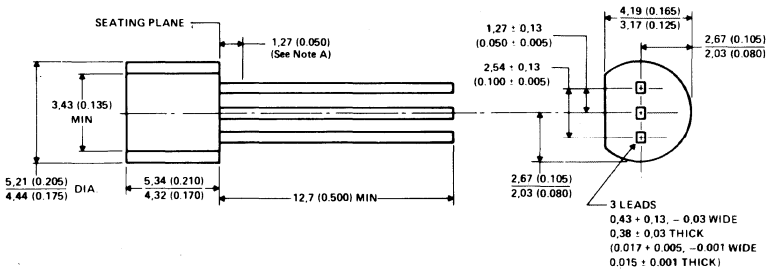
NOT TO SCALE

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

LP plastic package

These packages each consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

LP PLASTIC



Falls Within JEDEC TO-226AA Dimensions
(TO-226AA Replaces TO-92)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

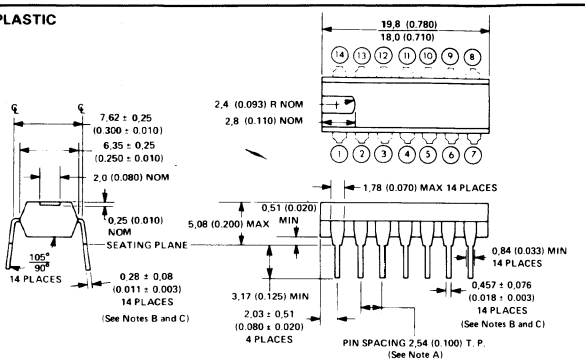
NOT TO SCALE

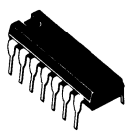
NOTE A: Lead dimensions are not controlled within this area.

N plastic dual-in-line package

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) or 15,24 (0.600) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

14-PIN N PLASTIC



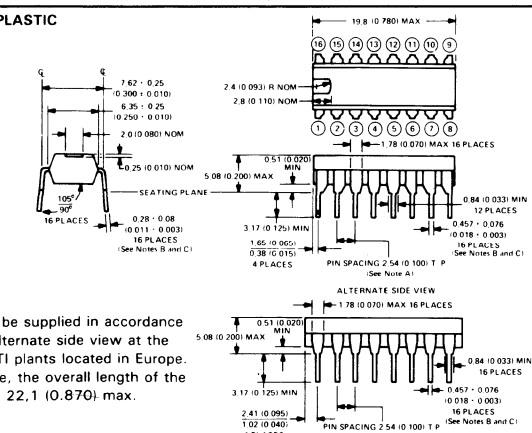


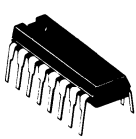
Falls Within JEDEC TO 116 and EIA MO 001AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOT TO SCALE

16-PIN N PLASTIC





ALTERNATE SIDE VIEW

Parts may be supplied in accordance with the alternate side view at the option of TI plants located in Europe. In this case, the overall length of the package is 22,1 (0.870) max.

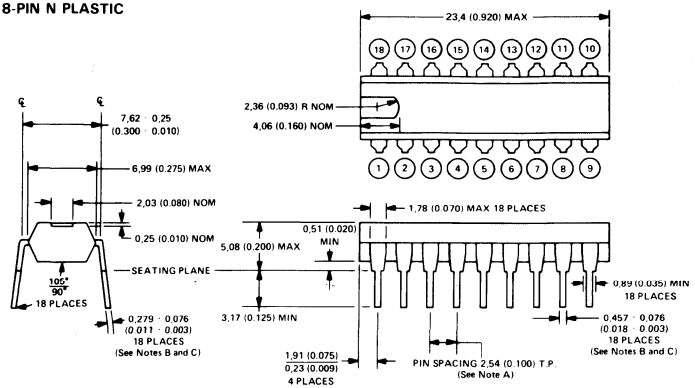
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

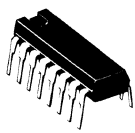
NOT TO SCALE

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line packages (continued)

18-PIN N PLASTIC

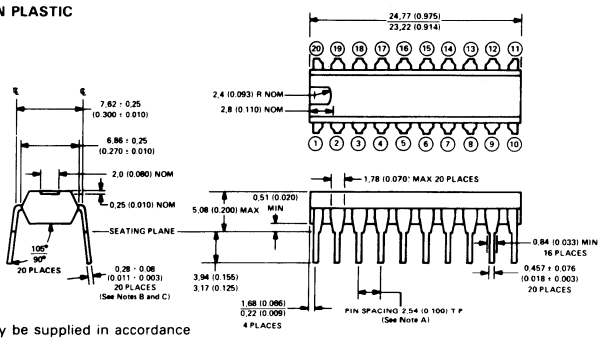


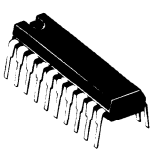


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

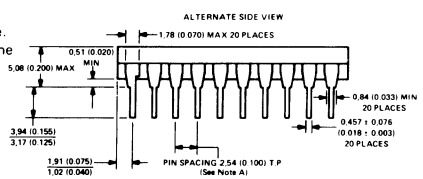
NOT TO SCALE

20-PIN N PLASTIC





Parts may be supplied in accordance with the alternate side view at the option of TI plants locatd in Europe. In this case, the overall length of the package is 26,7 (1.050) max.



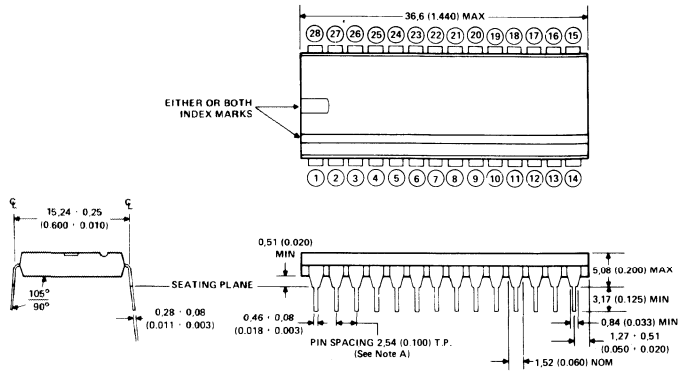
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

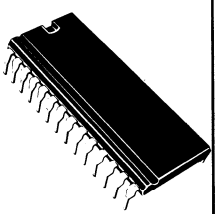
NOT TO SCALE

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic packages (continued)

28-PIN N PLASTIC

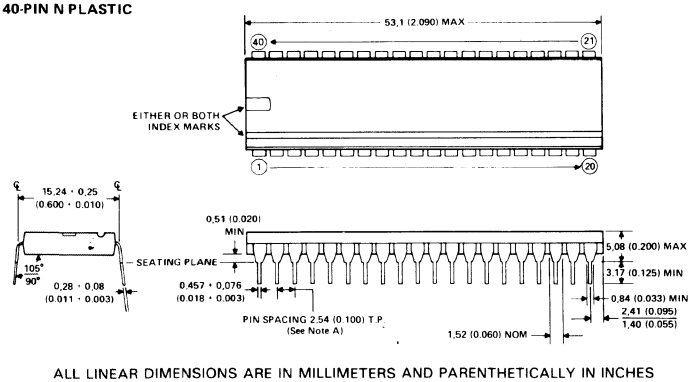


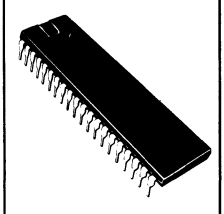


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOT TO SCALE

40-PIN N PLASTIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

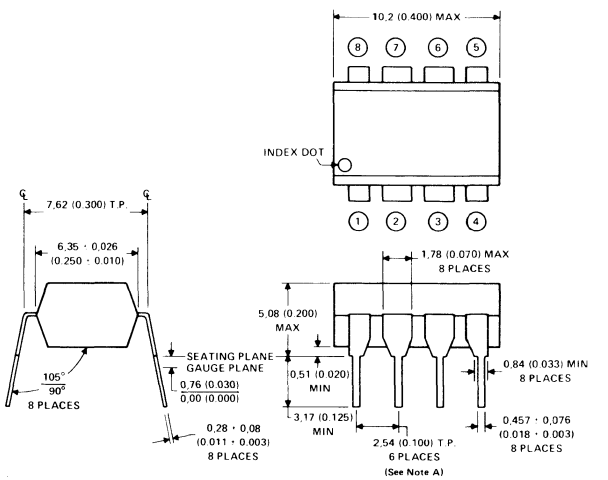
NOT TO SCALE

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

P dual-in-line plastic package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics remain stable when operated under high-humidity conditions. The package is intended for insertion in mounting hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldering assembly.

8-PIN P PLASTIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

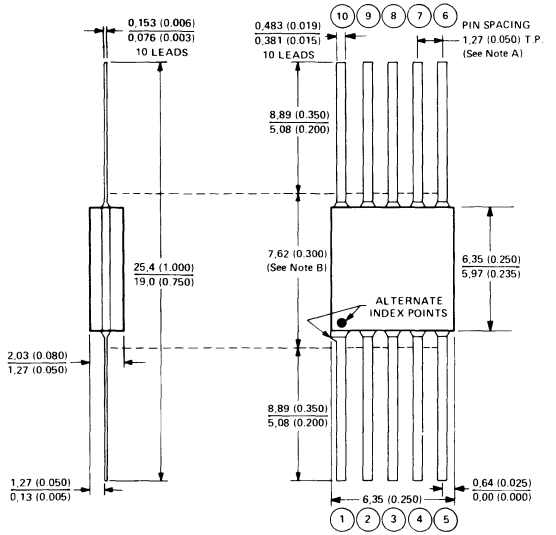
NOT TO SCALE

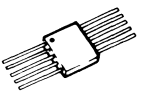
NOTE A: Each pin centerline is within 0,13 (0.005) radius of true position at the gauge plane with maximum material condition and unit installed.

U ceramic flat packages

This flat package consists of a ceramic base, ceramic cap, and lead frame. Circuit bars are alloy mounted. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

10-PIN U CERAMIC





Falls Within JEDEC MO-004AE Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

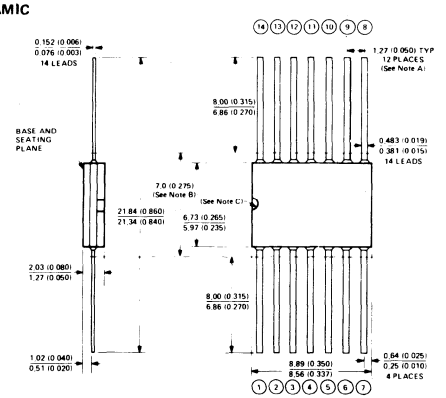
NOT TO SCALE

NOTES: A. Leads are within 0.005 radius of true position (TP) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.

W ceramic flat packages

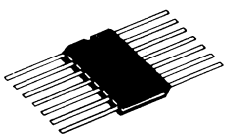
These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

14-PIN W CERAMIC



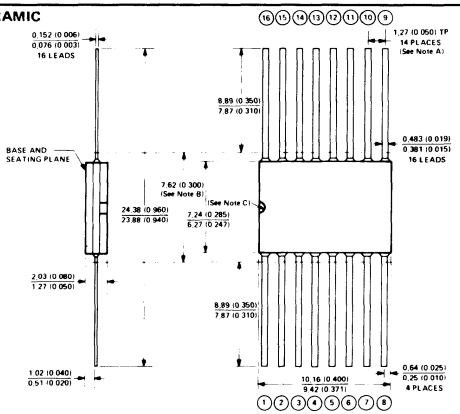
Falls Within JEDEC MO-004AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES



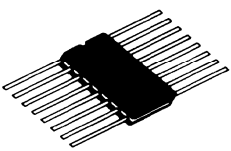
NOT TO SCALE

16-PIN W CERAMIC



Falls Within JEDEC MO-004AG Dimensions

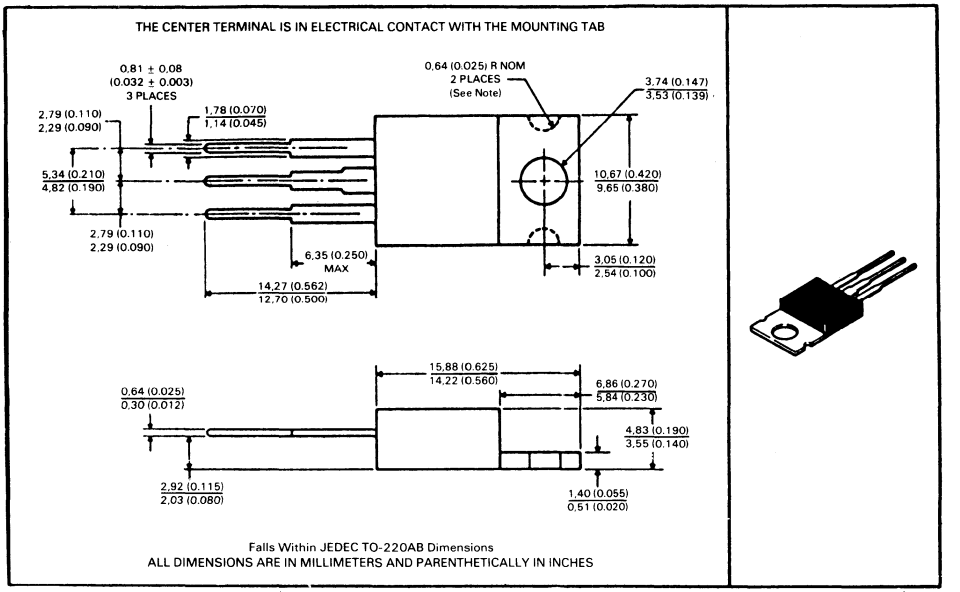
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES



NOT TO SCALE

NOTES: A. Leads are within 0,13 (0.005) radius of true position (TP) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.

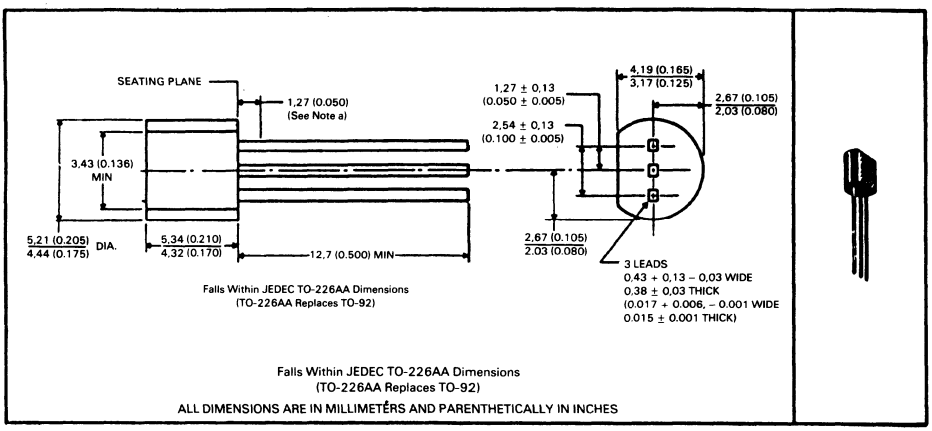
KC (TO-220AB) package



NOTE: Notches may or may not be present.

LP plastic package

This package is an encapsulation in a plastic compound specifically designed for this purpose. The package will withstand soldering temperatures without deformation. The package exhibits stable characteristics under high-humidity conditions and is capable of meeting MIL-STD-202C, Method 106B.



NOTE: a: Lead dimensions are not controlled in this area.